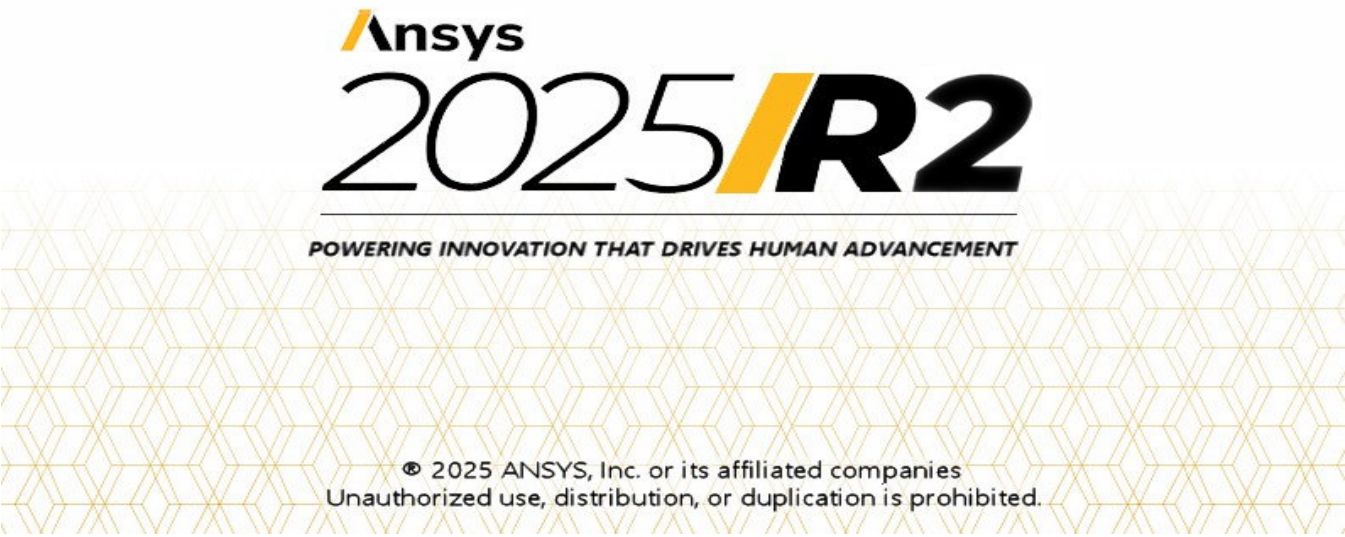

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Twin Builder® Components: Power Management ICs

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1 - Power Management ICs Library

The Power Management ICs library provides real components from manufacturers. It consists of the following types of components:

- High and Low Side Drivers
- High Side Switches
- Linear Regulators
- Low Side Switches
- Power Factor Correction
- PWM Controllers
- Three Phase Bridge Drivers

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High and Low Side Drivers

The High and Low Side Drivers consist of the following types of models:

- ADP3623
- ADP3624
- ADP3625
- ADP3629
- ADP3630
- ADP3631
- ADP3633
- ADP3634
- ADP3635
- EL7155
- EL7158
- IR2110
- IR2127
- IR2128
- IR21271
- LM2722
- LM2724A
- LM27222
- LM5100A
- LM5100B
- LM5100C
- LM5101A
- LM5101B
- LM5101C
- LM5102
- LM5104
- LM5105
- LM5106

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- LM5107
- LM5109A
- LM5109B
- LM5110
- LM5111
- LM5112
- LM5113
- LM5114
- RIC7113A4
- UCC27200A
- UCC27517

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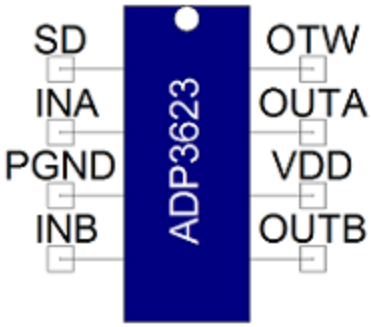
ADP3623: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *ADP362x/ADP363x* is a family of high current and dual high speed drivers, capable of driving two independent N-channel power MOSFETs. The family uses the industry-standard footprint but adds high speed switching performance and improved system reliability. The family has an internal temperature sensor and provides two levels of over-temperature protection, an over-temperature warning, and an over-temperature shutdown at extreme junction temperatures. The SD function, generated from a precise internal comparator, provides fast system enable or shutdown. This feature allows redundant overvoltage protection, complementing the protection inside the main controller device, or provides safe system shutdown in the event of an over-temperature warning. The wide input voltage range allows the driver to be compatible with both analog and digital PWM controllers. Digital power controllers are supplied from a low voltage supply, and the driver is supplied from a higher voltage supply. The *ADP362x/ADP363x* family adds UVLO and hysteresis functions, allowing safe startup and shutdown of the higher voltage supply

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when used with low voltage digital controllers. The device family is available in thermally enhanced SOIC_N_EP and MINI_SO_EP packaging to maximize high frequency and current switching in a small printed circuit board (PCB) area.

Inputs are modeled with voltage meters and resistances. The drivers outputs are modeled with ideal switches and resistances. The logic and delays are modeled with state machines.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	SD	Output Shutdown. When high, this pin disables normal operation, forcing OUTA and OUTB low.
2	INA	Inverting Input Pin for Channel A Gate Driver.
3	PGND	Ground. This pin should be closely connected to the source of the power MOSFET.
4	INB	Inverting Input Pin for Channel B Gate Driver.
5	OUTB	Output Pin for Channel B Gate Driver.
6	VDD	Power Supply Voltage. Bypass this pin to PGND with a ~1 µF to 5 µF ceramic capacitor.
7	OUTA	Output Pin for Channel A Gate Driver.
8	OTW	Overtemperature Warning Flag. Open drain, active low.

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Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

SUPPLY						
Supply Voltage Range		4.5		18	5	V
Supply Current	No switching, INA and INB disabled		1.2	3	1.2	mA
Standby Current			1.2	3	1.2	mA
UVLO						
Turn-On Threshold Voltage		3.8	4.2	4.5	4.2	V
Turn-Off Threshold Voltage		3.5	3.9	4.3	3.9	V
Hysteresis			0.3		0.3	V
DIGITAL INPUTS						
Input Voltage High		2			2	V
Input Voltage Low				0.8	0.8	V
Input Current	$0\ V < V_{IN} < V_{DD}$	-20		20	-20/20	uA
SD Threshold High		1.19	1.28	1.38	1.28	V
SD Threshold Low		0.95	1	1.05	1	V
SD Hysteresis			0.28		0.28	V
Internal Pull-up/Pull-Down Current			6		6	uA
OUTPUTS						
Output Resistance, Unbiased	VDD = PGND		80		80	kOhm
Peak Source Current			4		4	A
Peak Sink Current			-4		-4	A
SWITCHING TIME						

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OUTA, OUTB Rise Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Fall Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Rise Propagation Delay	C_{LOAD} = 2.2 nF		14	30	14	ns
OUTA, OUTB Rise Time Propagation Delay	C_{LOAD} = 2.2 nF		22	35	22	ns
SD Propaga-tion Delay Low			32	45	32	ns
SD Propaga-tion Delay High			48	75	48	ns
Delay Match-ing Between Channels			2			ns
OVERTEMPERATURE PROTECTION				NOT IMPLEMENTED		

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Example circuit :

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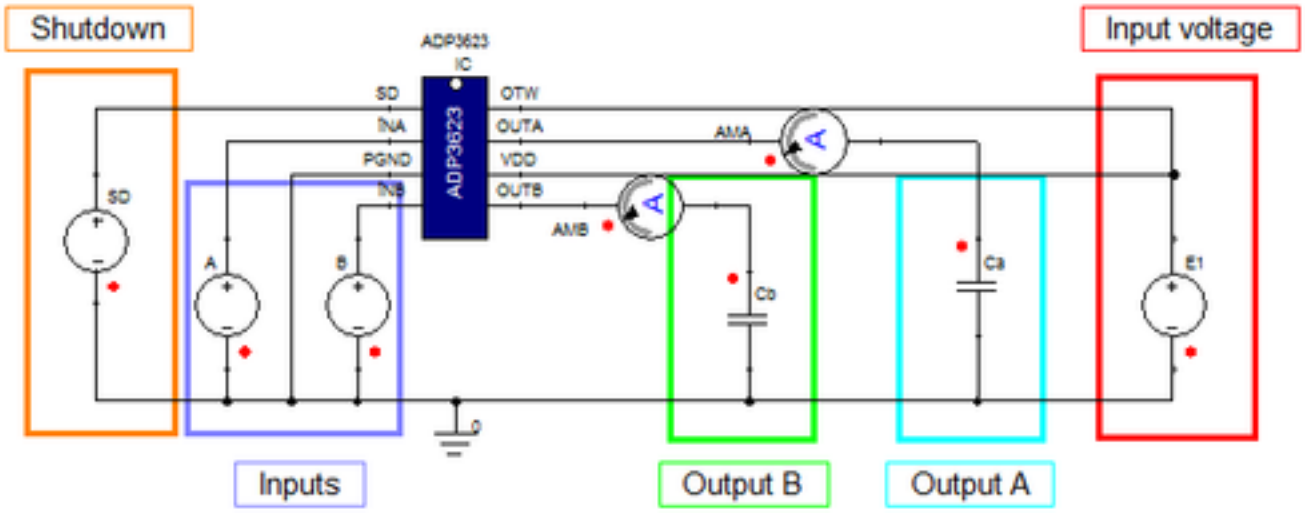
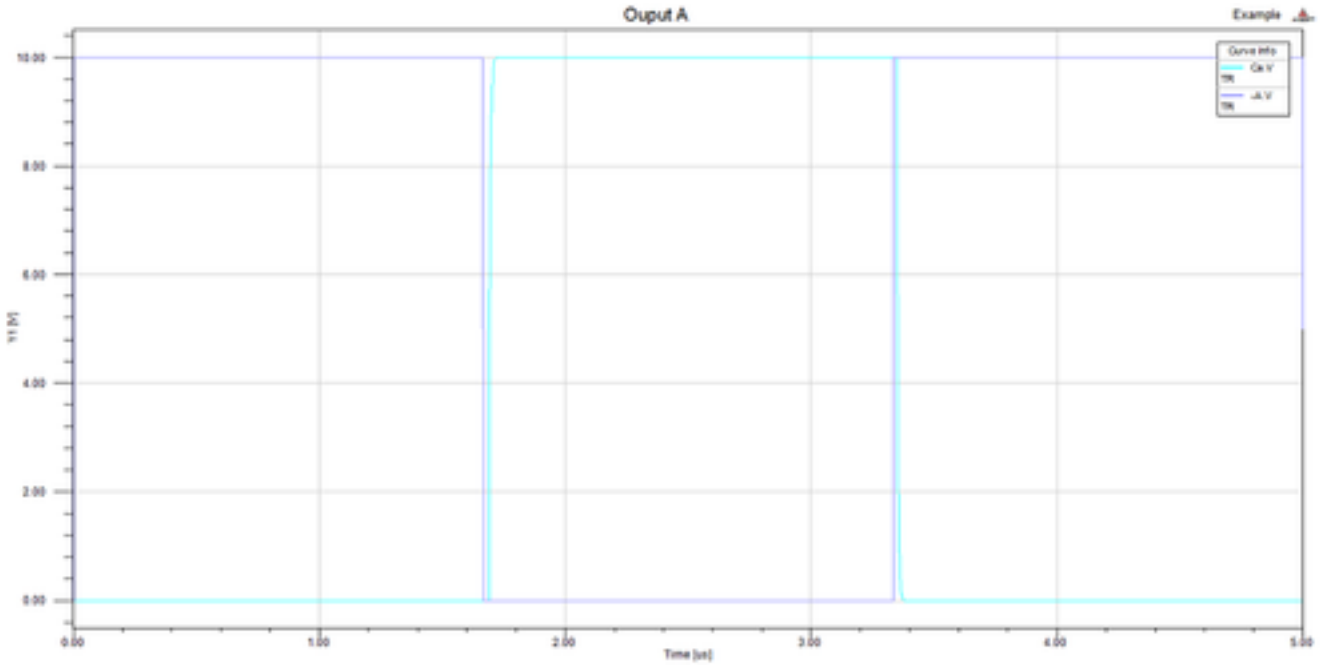


Figure 2. Example Circuit

Simulation results :



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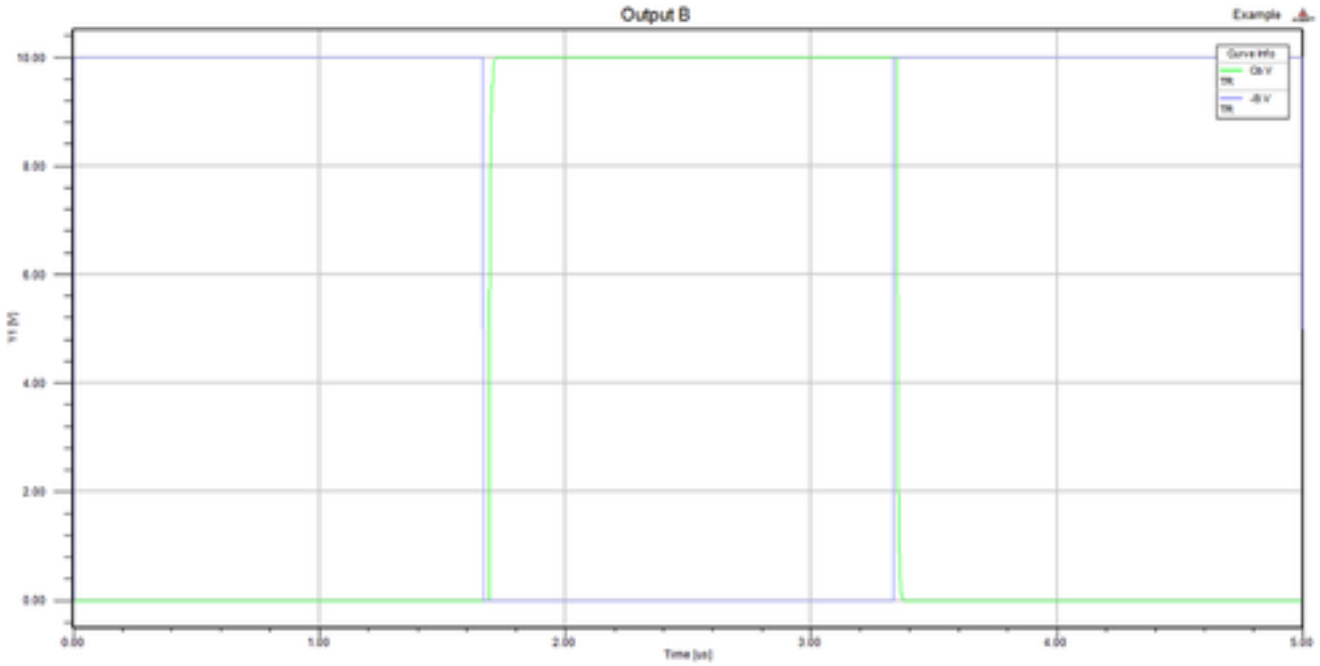

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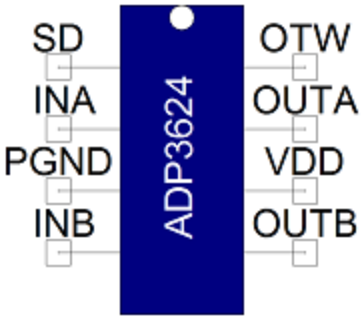
ADP3624: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *ADP362x/ADP363x* is a family of high current and dual high speed drivers, capable of driving two independent N-channel power MOSFETs. The family uses the industry-standard footprint but adds high speed switching performance and improved system reliability. The family has an internal temperature sensor and provides two levels of over-temperature protection, an over-temperature warning, and an over-temperature shutdown at extreme junction temperatures. The SD function, generated from a precise internal comparator, provides fast system enable or shutdown. This feature allows redundant overvoltage protection, complementing the protection inside the main controller device, or provides safe system shutdown in the event of an over-temperature warning. The wide input voltage range allows the driver to be compatible with both analog and digital PWM controllers. Digital power controllers are supplied from a low voltage supply, and the driver is supplied from a higher voltage supply. The *ADP362x/ADP363x* family adds UVLO and hysteresis functions, allowing safe startup and shutdown of the higher voltage supply

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when used with low voltage digital controllers. The device family is available in thermally enhanced SOIC_N_EP and MINI_SO_EP packaging to maximize high frequency and current switching in a small printed circuit board (PCB) area.

Inputs are modeled with voltage meters and resistances. The drivers outputs are modeled with ideal switches and resistances. The logic and delays are modeled with state machines.

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Table 1

PIN	NAME	FUNCTION
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2	INA	Inverted Input Pin for Channel A Gate Driver.
3	PGND	Ground. This pin should be closely connected to the source of the power MOSFET.
4	INB	Inverted Input Pin for Channel B Gate Driver.
5	OUTB	Output Pin for Channel B Gate Driver.
6	VDD	Power Supply Voltage. Bypass this pin to PGND with a ~1 µF to 5 µF ceramic capacitor.
7	OUTA	Output Pin for Channel A Gate Driver.
8	OTW	Overtemperature Warning Flag. Open drain, active low.

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

SUPPLY						
Supply Voltage Range		4.5		18	10	V
Supply Current	No switching, INA and INB disabled		1.2	3	1.2	mA
Standby Current			1.2	3	1.2	mA
UVLO						
Turn-On Threshold Voltage		3.8	4.2	4.5	4.2	V
Turn-Off Threshold Voltage		3.5	3.9	4.3	3.9	V
Hysteresis			0.3		0.3	V
DIGITAL INPUTS						
Input Voltage High		2			2	V
Input Voltage Low				0.8	0.8	V
Input Current	$0\ V < V_{IN} < V_{DD}$	-20		20	-20/20	uA
SD Threshold High		1.19	1.28	1.38	1.28	V
SD Threshold Low		0.95	1	1.05	1	V
SD Hysteresis			0.28		0.28	V
Internal Pull-up/Pull-Down Current			6		6	uA
OUTPUTS						
Output Resistance, Unbiased	VDD = PGND		80		80	kOhm
Peak Source Current			4		4	A
Peak Sink Current			-4		-4	A
SWITCHING TIME						

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OUTA, OUTB Rise Time	C_{LOAD} = 2.2 nF		10	25	10	ns
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OUTA, OUTB Rise Propagation Delay	C_{LOAD} = 2.2 nF		14	30	14	ns
OUTA, OUTB Rise Time Propagation Delay	C_{LOAD} = 2.2 nF		22	35	22	ns
SD Propaga-tion Delay Low			32	45	32	ns
SD Propaga-tion Delay High			48	75	48	ns
Delay Match-ing Between Channels			2			ns
OVERTEMPERATURE PROTECTION				NOT IMPLEMENTED		

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Example circuit :

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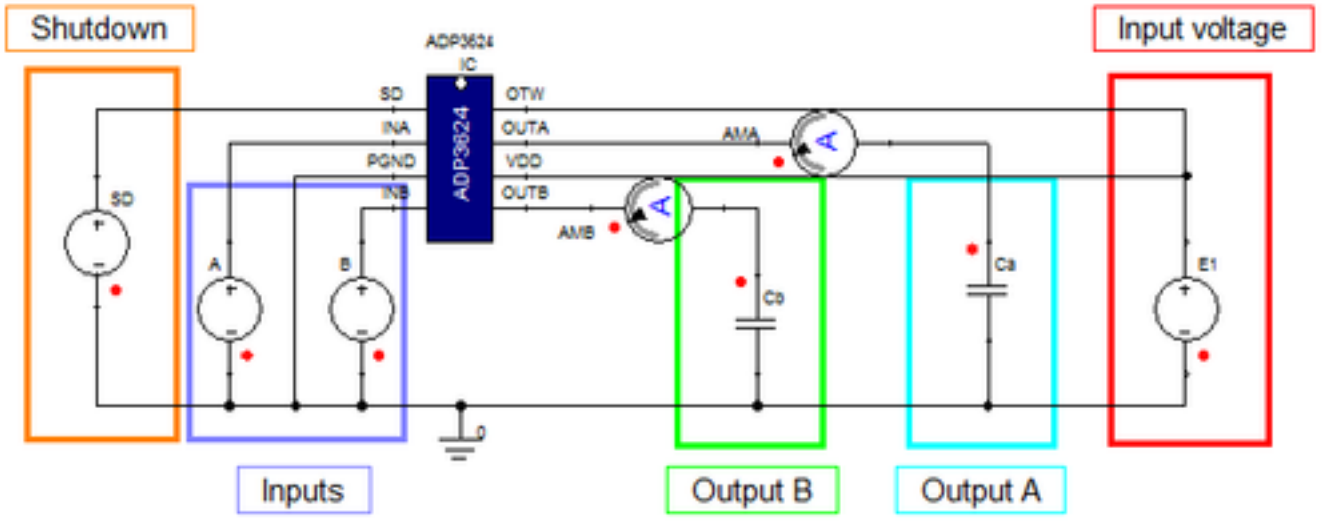
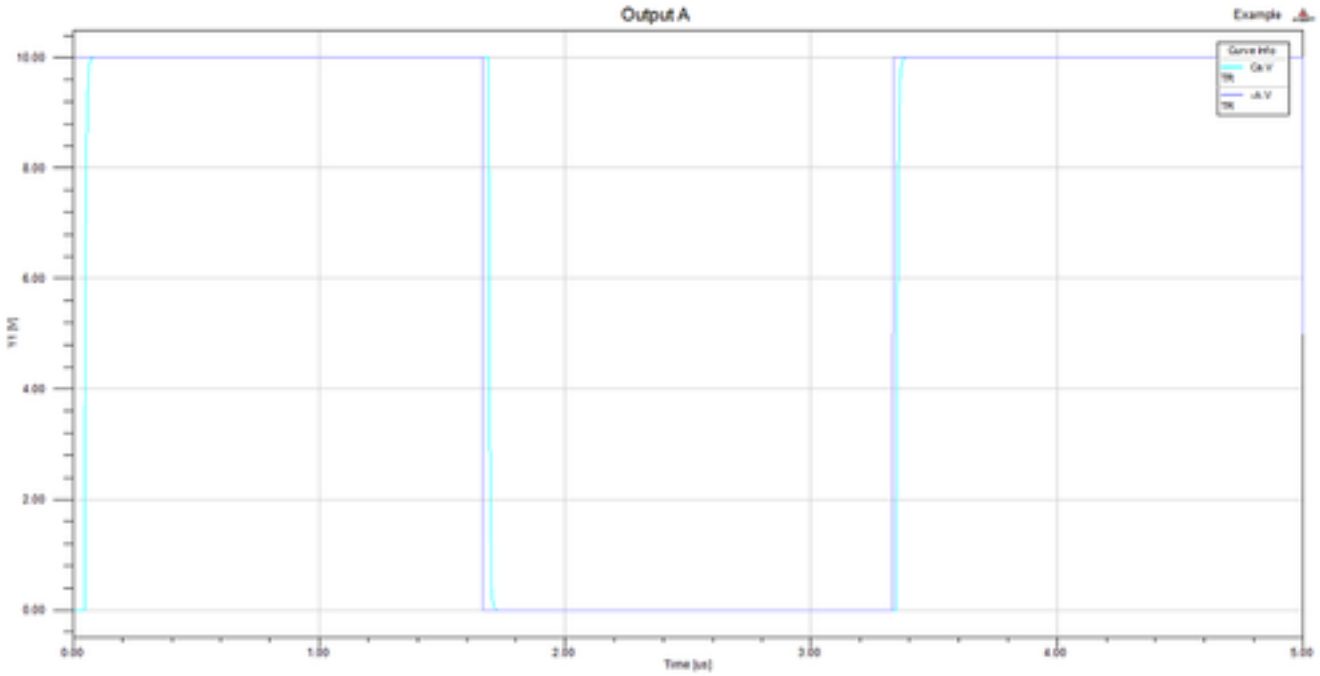


Figure 2. Example Circuit

Simulation results :



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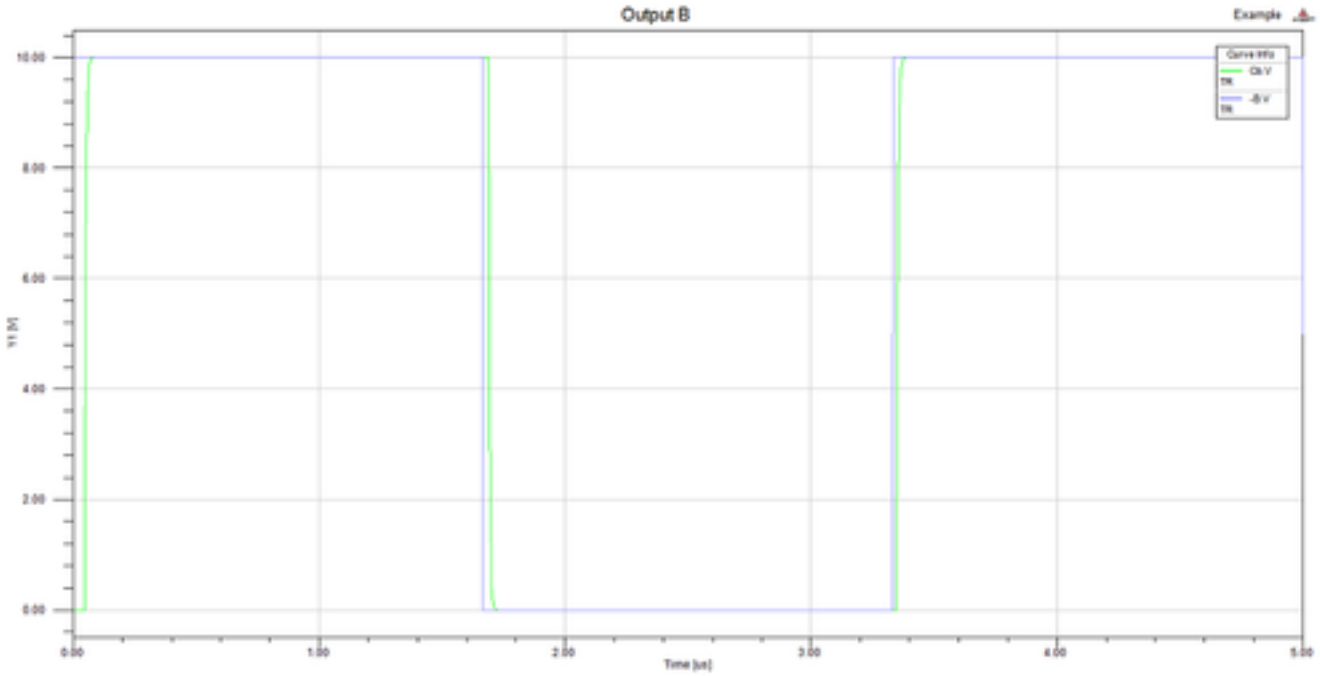

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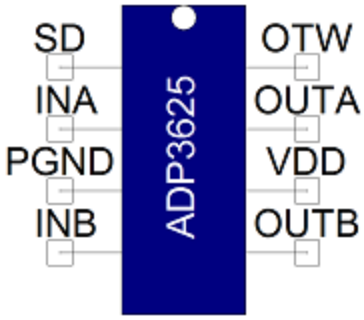
ADP3625: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

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when used with low voltage digital controllers. The device family is available in thermally enhanced SOIC_N_EP and MINI_SO_EP packaging to maximize high frequency and current switching in a small printed circuit board (PCB) area.

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4	INB	Input Pin for Channel B Gate Driver.
5	OUTB	Output Pin for Channel B Gate Driver.
6	VDD	Power Supply Voltage. Bypass this pin to PGND with a ~1 µF to 5 µF ceramic capacitor.
7	OUTA	Output Pin for Channel A Gate Driver.
8	OTW	Overtemperature Warning Flag. Open drain, active low.

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

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SUPPLY						
Supply Voltage Range		4.5		18	10	V
Supply Current	No switching, INA and INB disabled		1.2	3	1.2	mA
Standby Current			1.2	3	1.2	mA
UVLO						
Turn-On Threshold Voltage		3.8	4.2	4.5	4.2	V
Turn-Off Threshold Voltage		3.5	3.9	4.3	3.9	V
Hysteresis			0.3		0.3	V
DIGITAL INPUTS						
Input Voltage High		2			2	V
Input Voltage Low				0.8	0.8	V
Input Current	$0\ V < V_{IN} < V_{DD}$	-20		20	-20/20	uA
SD Threshold High		1.19	1.28	1.38	1.28	V
SD Threshold Low		0.95	1	1.05	1	V
SD Hysteresis			0.28		0.28	V
Internal Pull-up/Pull-Down Current			6		6	uA
OUTPUTS						
Output Resistance, Unbiased	VDD = PGND		80		80	kOhm
Peak Source Current			4		4	A
Peak Sink Current			-4		-4	A
SWITCHING TIME						

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

OUTA, OUTB Rise Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Fall Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Rise Propagation Delay	C_{LOAD} = 2.2 nF		14	30	14	ns
OUTA, OUTB Rise Time Propagation Delay	C_{LOAD} = 2.2 nF		22	35	22	ns
SD Propaga-tion Delay Low			32	45	32	ns
SD Propaga-tion Delay High			48	75	48	ns
Delay Match-ing Between Channels			2			ns
OVERTEMPERATURE PROTECTION				NOT IMPLEMENTED		

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Examples

Example circuit :

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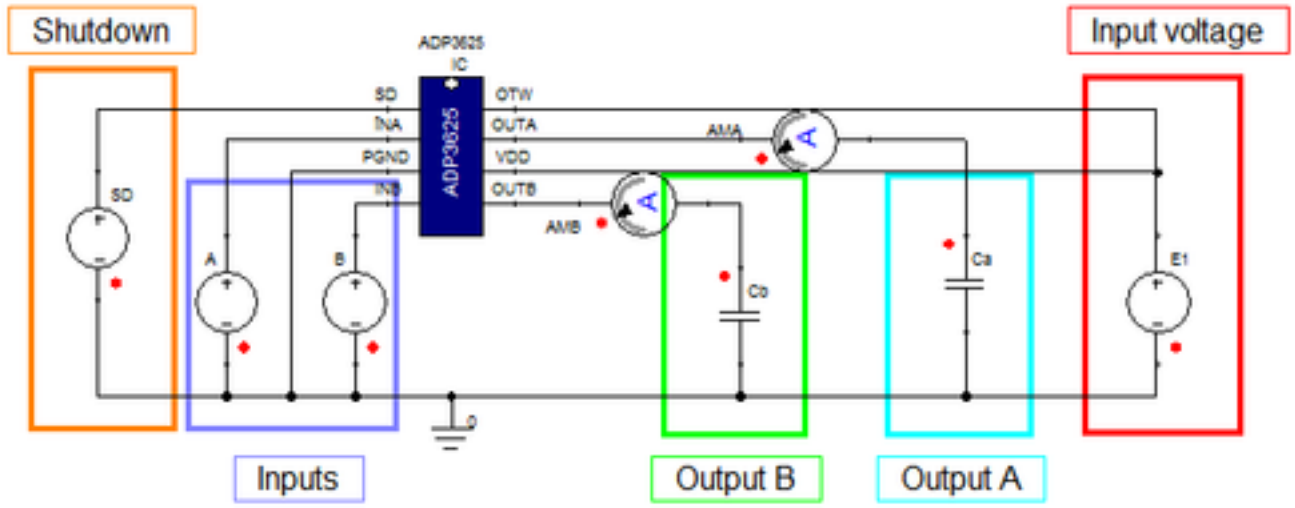
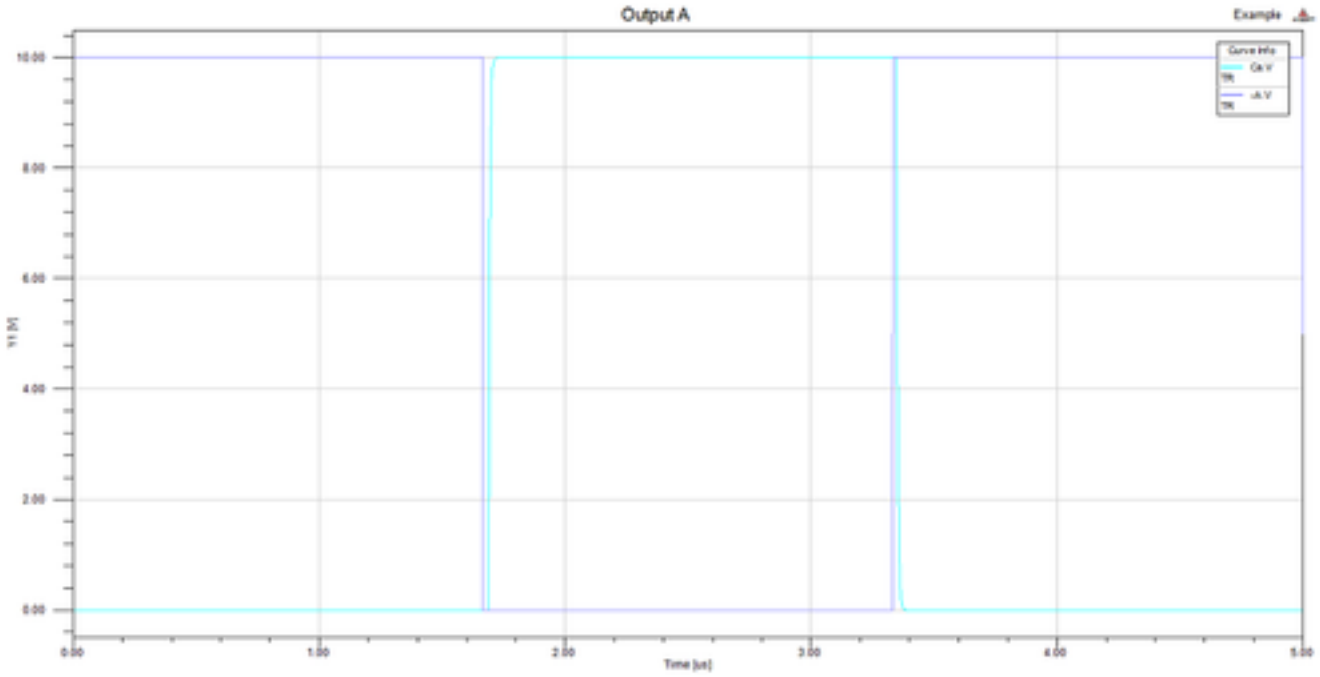


Figure 2. Example Circuit

Simulation results :



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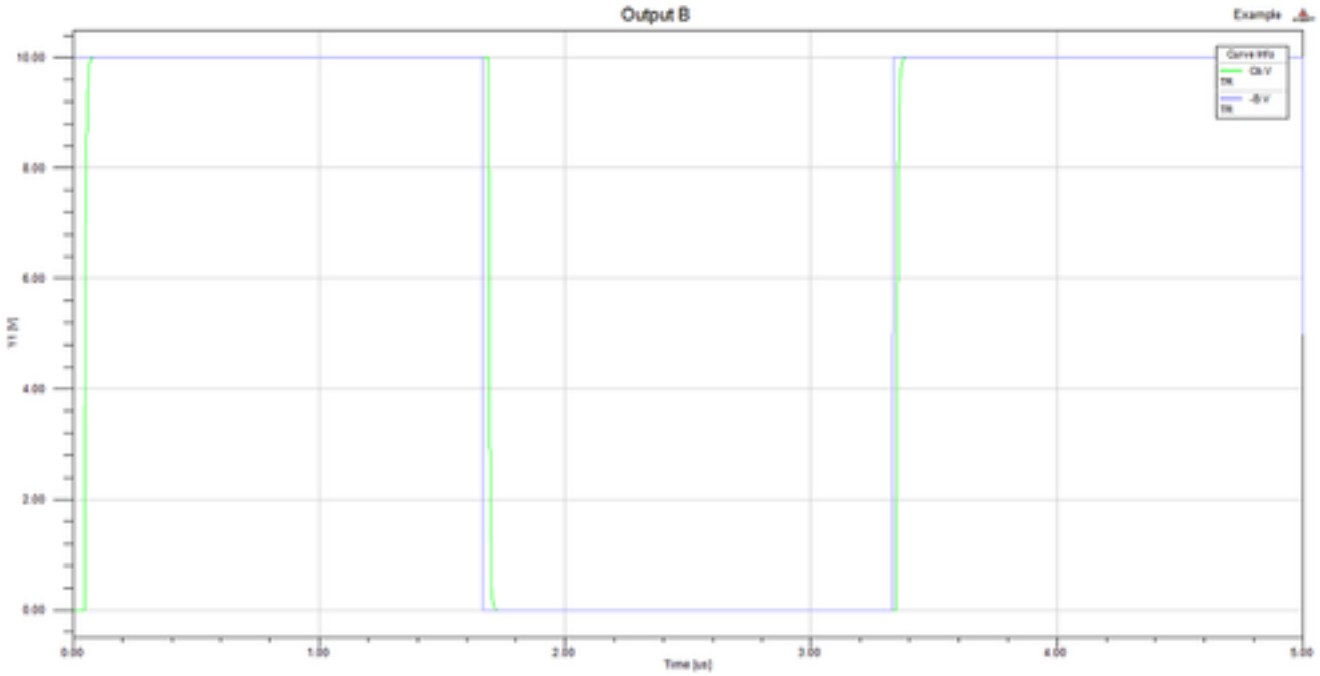

Figure 3. Simulation results

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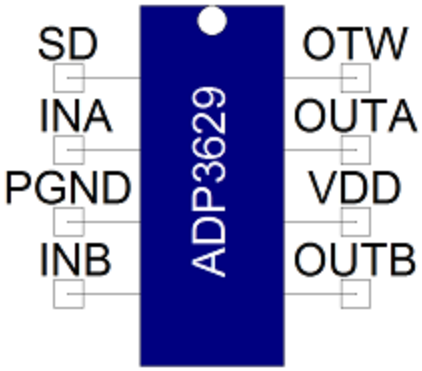
ADP3629: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *ADP3629/ADP3630/ADP3631* are dual, high current, high speed drivers, capable of driving two independent N-channel power MOSFETs. The *ADP3629/ADP3630/ADP3631* use the industry-standard footprint but add high speed switching performance and improved system reliability. The *ADP3629/ADP3630/ADP3631* have an internal temperature sensor and provide two levels of over-temperature protection: an over-temperature warning and an over-temperature shutdown at extreme junction temperatures. The SD function, generated from a precise internal comparator, provides fast system enable or shutdown. This feature allows redundant over-voltage protection, complementing the protection inside the main controller device, or provides safe system shutdown in the event of an over-temperature warning. The wide input voltage range allows the driver to be compatible with both analog and digital PWM controllers. Digital power controllers are supplied from a low voltage supply, and the driver is supplied from a higher voltage supply. The *ADP3629/ADP3630/ADP3631* add UVLO and hysteresis functions,

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allowing safe startup and shutdown of the higher voltage supply when used with low voltage digital controllers.

Inputs are modeled with voltage meters and resistances. The drivers outputs are modeled with ideal switches and resistances. The logic and delays are modeled with state machines.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	SD	Output Shutdown. When high, this pin disables normal operation, forcing OUTA and OUTB low.
2	INA	Inverted Input Pin for Channel A Gate Driver.
3	PGND	Ground. This pin should be closely connected to the source of the power MOSFET.
4	INB	Inverted Input Pin for Channel B Gate Driver.
5	OUTB	Output Pin for Channel B Gate Driver.
6	VDD	Power Supply Voltage. Bypass this pin to PGND with a ~1 µF to 5 µF ceramic capacitor.
7	OUTA	Output Pin for Channel A Gate Driver.
8	OTW	Overtemperature Warning Flag. Open drain, active low.

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

SUPPLY						
Supply Voltage Range		4.5		18	10	V
Supply Current	No switching, INA and INB disabled		1.2	3	1.2	mA
Standby Current			1.2	3	1.2	mA
UVLO						
Turn-On Threshold Voltage		8.0	8.7	9.5	8.7	V
Turn-Off Threshold Voltage		7.0	7.7	8.5	7.7	V
Hysteresis			1.0		1.0	V
DIGITAL INPUTS						
Input Voltage High		2			2	V
Input Voltage Low				0.8	0.8	V
Input Current	$0\ V < V_{IN} < V_{DD}$	-20		20	-20/20	uA
SD Threshold High		1.19	1.28	1.38	1.28	V
SD Threshold Low		0.95	1	1.05	1	V
SD Hysteresis			0.28		0.28	V
Internal Pull-up/Pull-Down Current			6		6	uA
OUTPUTS						
Output Resistance, Unbiased	VDD = PGND		80		80	kOhm
Peak Source Current			2		2	A
Peak Sink Current			-2		-2	A
SWITCHING TIME						

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OUTA, OUTB Rise Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Fall Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Rise Propagation Delay	C_{LOAD} = 2.2 nF		14	30	14	ns
OUTA, OUTB Rise Time Propagation Delay	C_{LOAD} = 2.2 nF		22	35	22	ns
SD Propaga-tion Delay Low			32	45	32	ns
SD Propaga-tion Delay High			48	75	48	ns
Delay Match-ing Between Channels			2			ns
OVERTEMPERATURE PROTECTION				NOT IMPLEMENTED		

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Example circuit :

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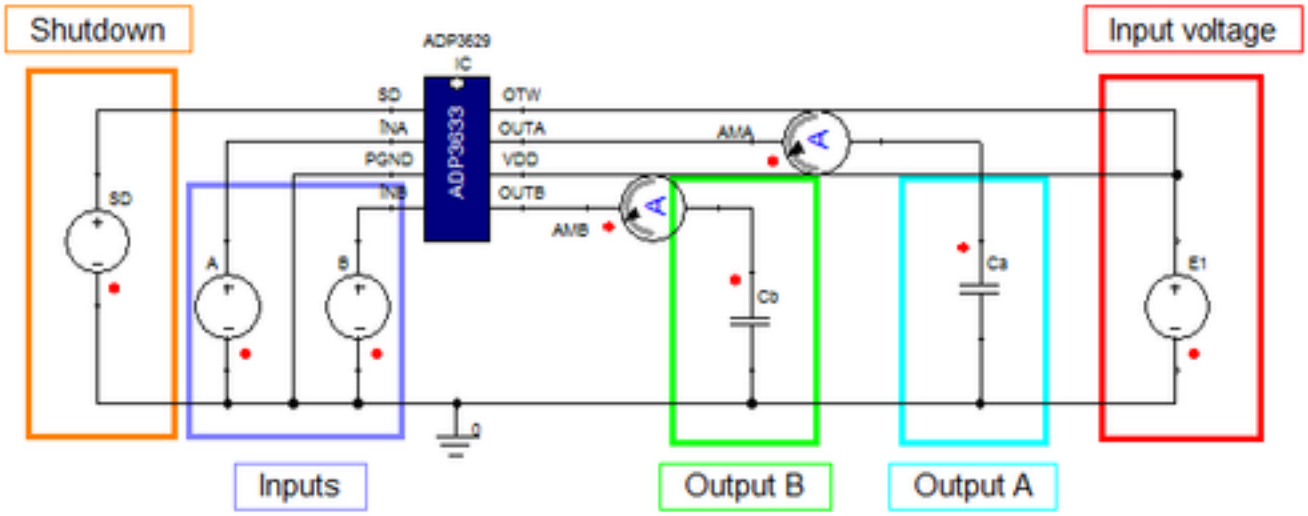
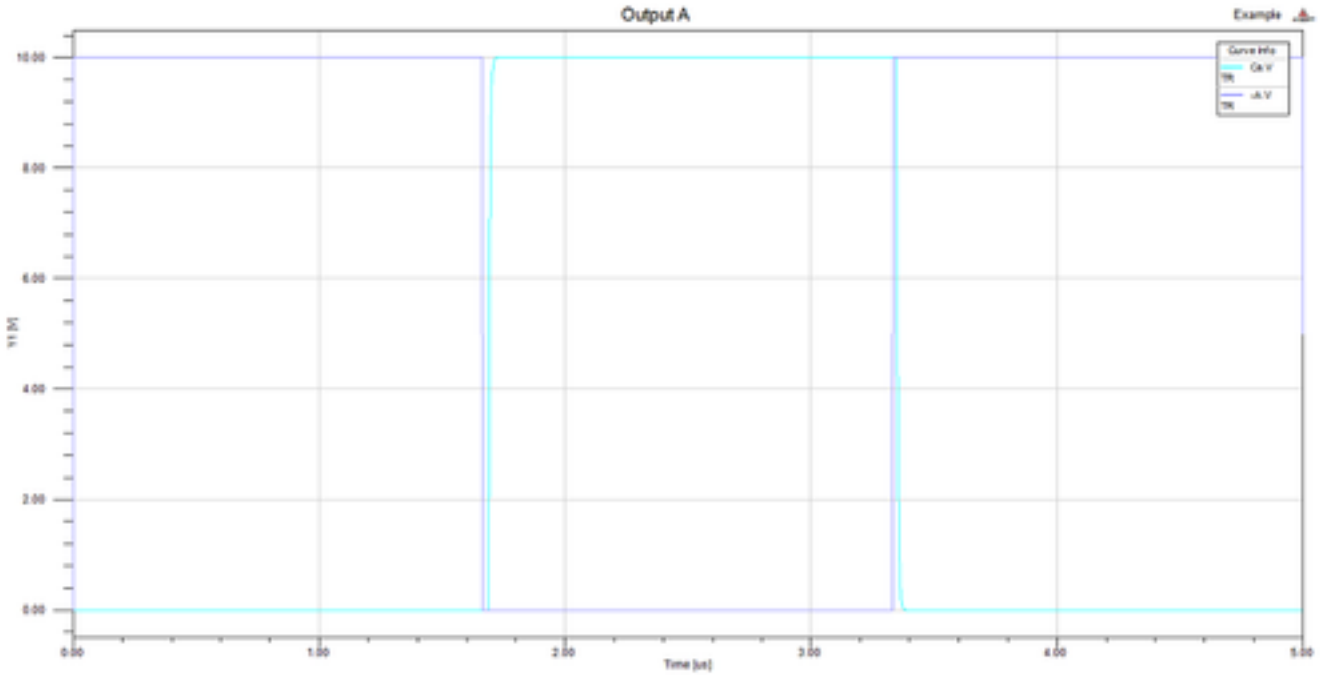


Figure 2. Example Circuit

Simulation results :



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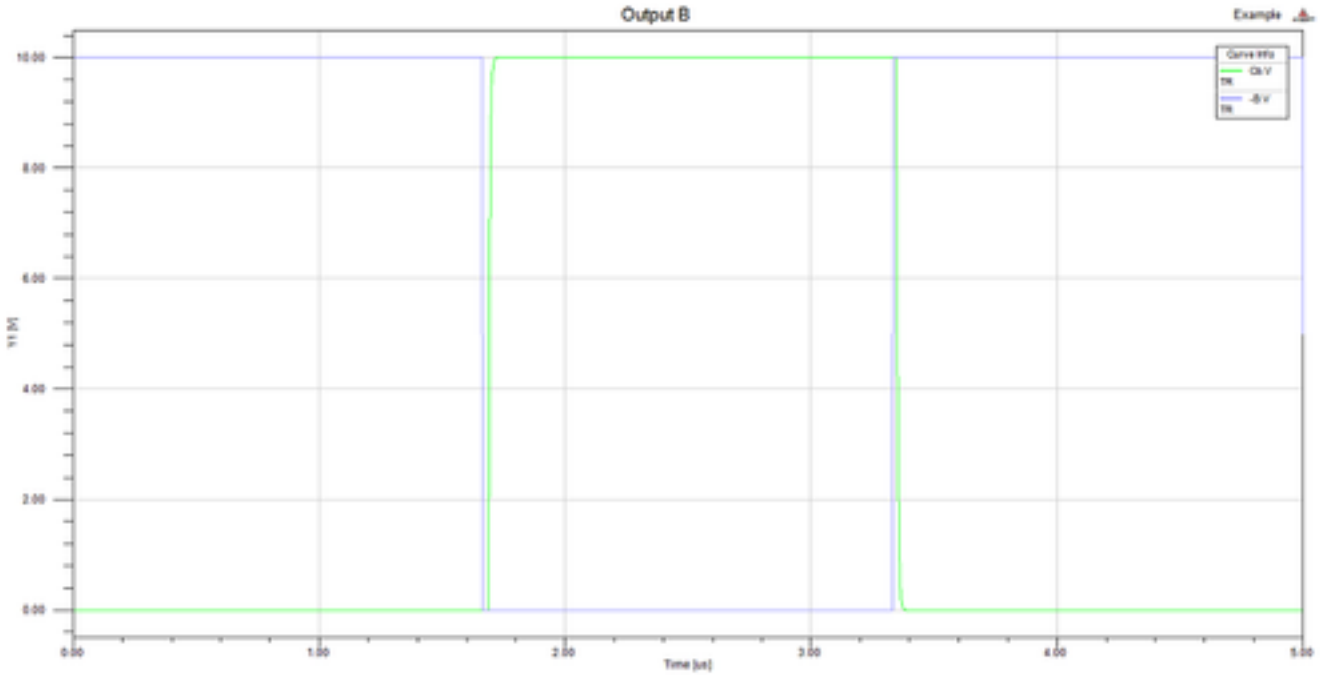

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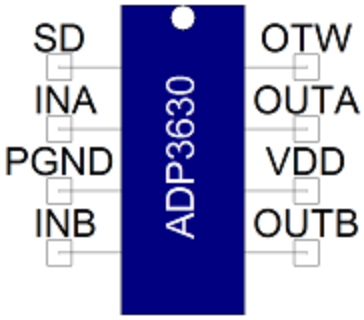
ADP3630: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *ADP3629/ADP3630/ADP3631* are dual, high current, high speed drivers, capable of driving two independent N-channel power MOSFETs. The *ADP3629/ADP3630/ADP3631* use the industry-standard footprint but add high speed switching performance and improved system reliability. The *ADP3629/ADP3630/ADP3631* have an internal temperature sensor and provide two levels of over-temperature protection: an over-temperature warning and an over-temperature shutdown at extreme junction temperatures. The SD function, generated from a precise internal comparator, provides fast system enable or shutdown. This feature allows redundant over-voltage protection, complementing the protection inside the main controller device, or provides safe system shutdown in the event of an over-temperature warning. The wide input voltage range allows the driver to be compatible with both analog and digital PWM controllers. Digital power controllers are supplied from a low voltage supply, and the driver is supplied from a higher voltage supply. The *ADP3629/ADP3630/ADP3631* add UVLO and hysteresis functions,

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allowing safe startup and shutdown of the higher voltage supply when used with low voltage digital controllers.

Inputs are modeled with voltage meters and resistances. The drivers outputs are modeled with ideal switches and resistances. The logic and delays are modeled with state machines.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	SD	Output Shutdown. When high, this pin disables normal operation, forcing OUTA and OUTB low.
2	INA	Input Pin for Channel A Gate Driver.
3	PGND	Ground. This pin should be closely connected to the source of the power MOSFET.
4	INB	Input Pin for Channel B Gate Driver.
5	OUTB	Output Pin for Channel B Gate Driver.
6	VDD	Power Supply Voltage. Bypass this pin to PGND with a ~1 µF to 5 µF ceramic capacitor.
7	OUTA	Output Pin for Channel A Gate Driver.
8	OTW	Overtemperature Warning Flag. Open drain, active low.

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

SUPPLY						
Supply Voltage Range		4.5		18	10	V
Supply Current	No switching, INA and INB disabled		1.2	3	1.2	mA
Standby Current			1.2	3	1.2	mA
UVLO						
Turn-On Threshold Voltage		8.0	8.7	9.5	8.7	V
Turn-Off Threshold Voltage		7.0	7.7	8.5	7.7	V
Hysteresis			1.0		1.0	V
DIGITAL INPUTS						
Input Voltage High		2			2	V
Input Voltage Low				0.8	0.8	V
Input Current	$0\ V < V_{IN} < V_{DD}$	-20		20	-20/20	uA
SD Threshold High		1.19	1.28	1.38	1.28	V
SD Threshold Low		0.95	1	1.05	1	V
SD Hysteresis			0.28		0.28	V
Internal Pull-up/Pull-Down Current			6		6	uA
OUTPUTS						
Output Resistance, Unbiased	VDD = PGND		80		80	kOhm
Peak Source Current			2		2	A
Peak Sink Current			-2		-2	A
SWITCHING TIME						

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OUTA, OUTB Rise Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Fall Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Rise Propagation Delay	C_{LOAD} = 2.2 nF		14	30	14	ns
OUTA, OUTB Rise Time Propagation Delay	C_{LOAD} = 2.2 nF		22	35	22	ns
SD Propaga-tion Delay Low			32	45	32	ns
SD Propaga-tion Delay High			48	75	48	ns
Delay Match-ing Between Channels			2		-	ns
OVERTEMPERATURE PROTECTION				NOT IMPLEMENTED		

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Examples

Example circuit :

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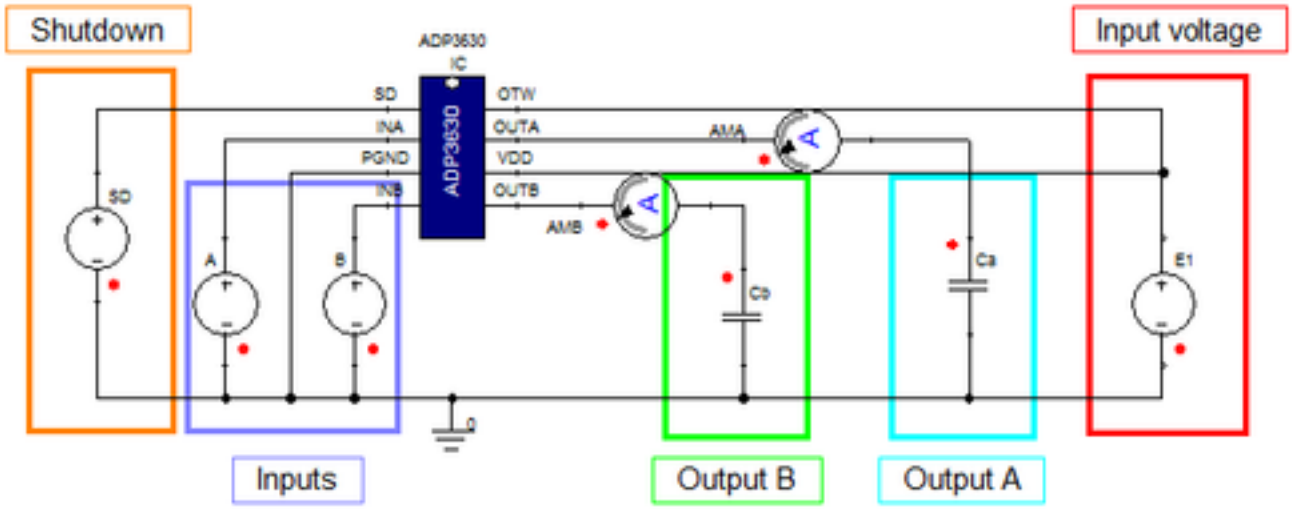
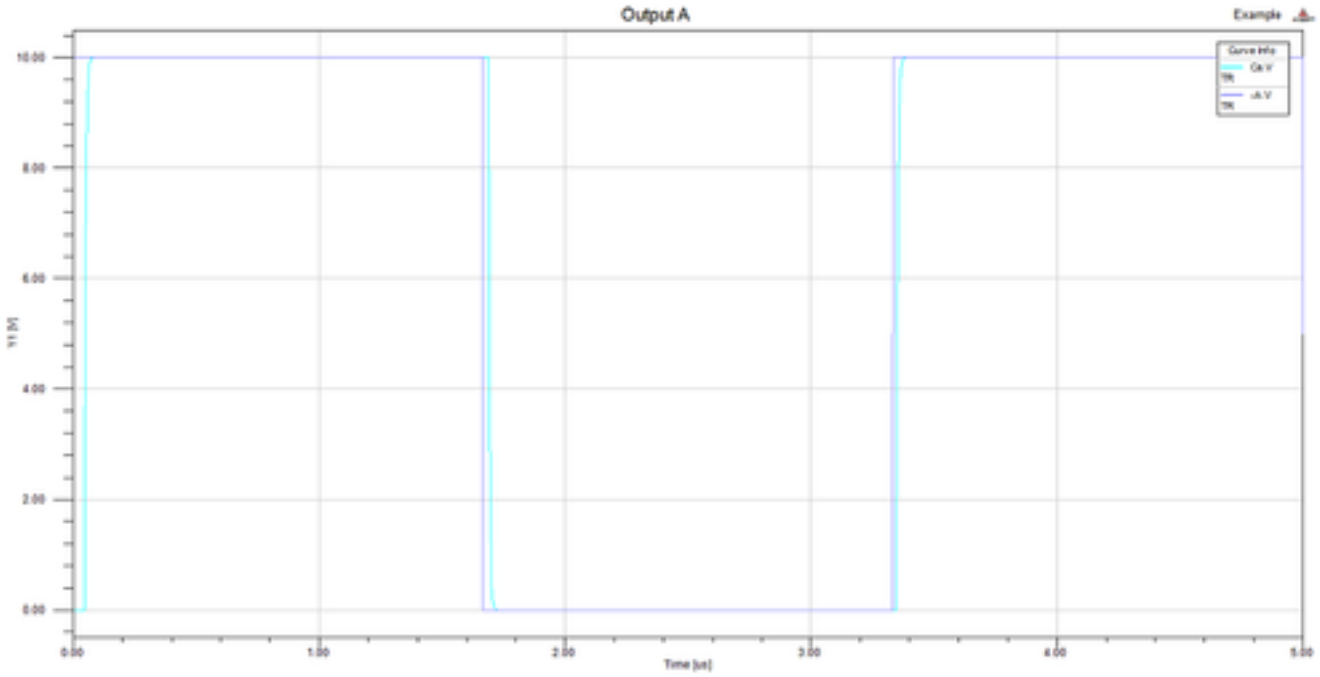


Figure 2. Example Circuit

Simulation results :



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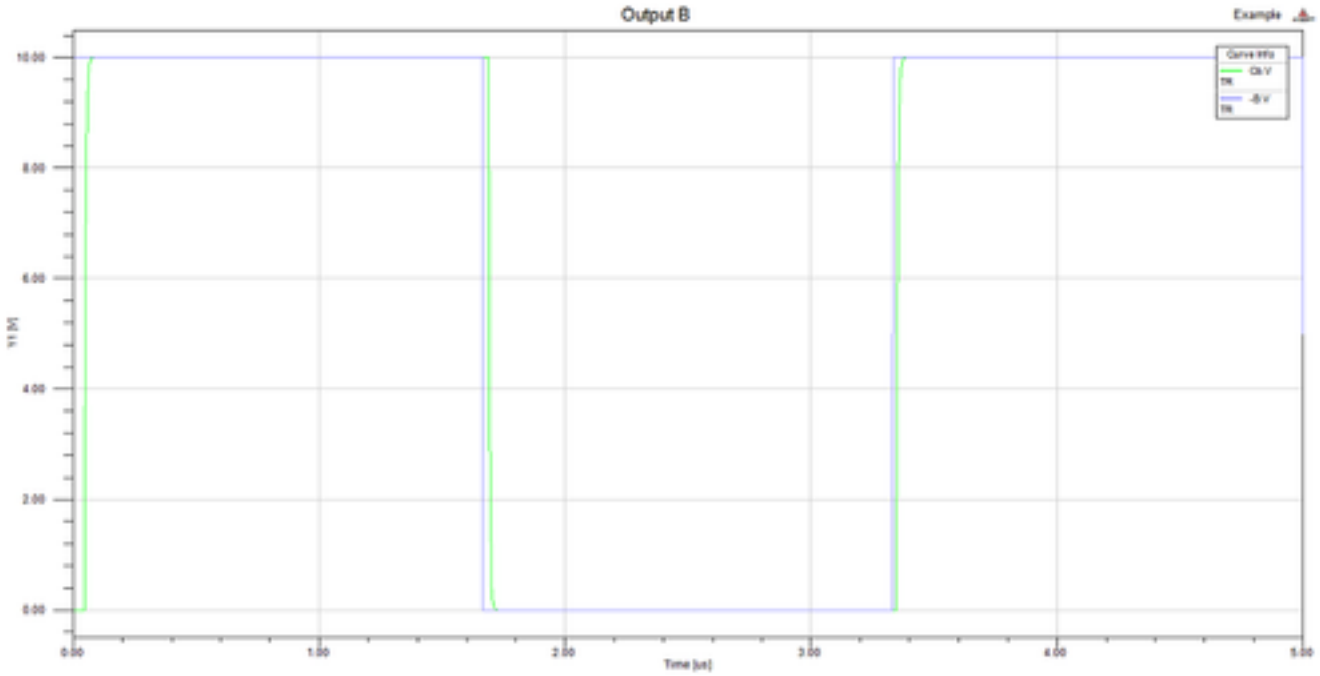

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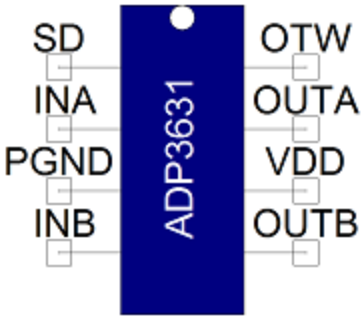
ADP3631: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *ADP3629/ADP3630/ADP3631* are dual, high current, high speed drivers, capable of driving two independent N-channel power MOSFETs. The *ADP3629/ADP3630/ADP3631* use the industry-standard footprint but add high speed switching performance and improved system reliability. The *ADP3629/ADP3630/ADP3631* have an internal temperature sensor and provide two levels of over-temperature protection: an over-temperature warning and an over-temperature shutdown at extreme junction temperatures. The SD function, generated from a precise internal comparator, provides fast system enable or shutdown. This feature allows redundant over-voltage protection, complementing the protection inside the main controller device, or provides safe system shutdown in the event of an over-temperature warning. The wide input voltage range allows the driver to be compatible with both analog and digital PWM controllers. Digital power controllers are supplied from a low voltage supply, and the driver is supplied from a higher voltage supply. The *ADP3629/ADP3630/ADP3631* add UVLO and hysteresis functions,

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allowing safe startup and shutdown of the higher voltage supply when used with low voltage digital controllers.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	SD	Output Shutdown. When high, this pin disables normal operation, forcing OUTA and OUTB low.
2	INA	Inverted Input Pin for Channel A Gate Driver.
3	PGND	Ground. This pin should be closely connected to the source of the power MOSFET.
4	INB	Input Pin for Channel B Gate Driver.
5	OUTB	Output Pin for Channel B Gate Driver.
6	VDD	Power Supply Voltage. Bypass this pin to PGND with a ~1 µF to 5 µF ceramic capacitor.
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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

SUPPLY						
Supply Voltage Range		4.5		18	10	V
Supply Current	No switching, INA and INB disabled		1.2	3	1.2	mA
Standby Current			1.2	3	1.2	mA
UVLO						
Turn-On Threshold Voltage		8.0	8.7	9.5	8.7	V
Turn-Off Threshold Voltage		7.0	7.7	8.5	7.7	V
Hysteresis			1.0		1.0	V
DIGITAL INPUTS						
Input Voltage High		2			2	V
Input Voltage Low				0.8	0.8	V
Input Current	$0\ V < V_{IN} < V_{DD}$	-20		20	-20/20	uA
SD Threshold High		1.19	1.28	1.38	1.28	V
SD Threshold Low		0.95	1	1.05	1	V
SD Hysteresis			0.28		0.28	V
Internal Pull-up/Pull-Down Current			6		6	uA
OUTPUTS						
Output Resistance, Unbiased	VDD = PGND		80		80	kOhm
Peak Source Current			2		2	A
Peak Sink Current			-2		-2	A
SWITCHING TIME						

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OUTA, OUTB Rise Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Fall Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Rise Propagation Delay	C_{LOAD} = 2.2 nF		14	30	14	ns
OUTA, OUTB Rise Time Propagation Delay	C_{LOAD} = 2.2 nF		22	35	22	ns
SD Propaga-tion Delay Low			32	45	32	ns
SD Propaga-tion Delay High			48	75	48	ns
Delay Match-ing Between Channels			2			ns
OVERTEMPERATURE PROTECTION				NOT IMPLEMENTED		

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Examples

Example circuit :

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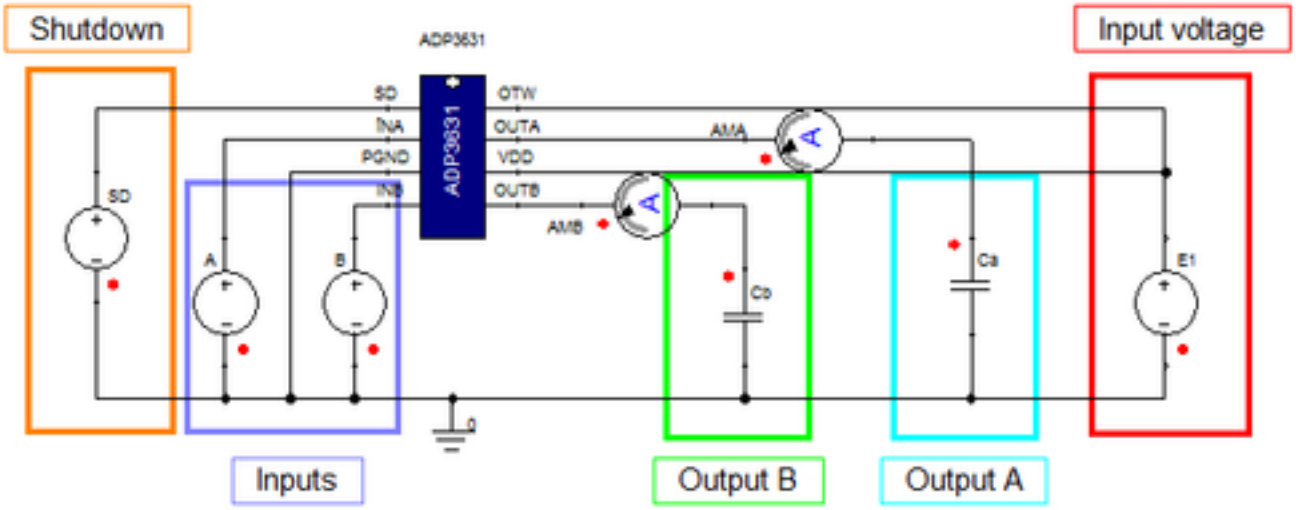
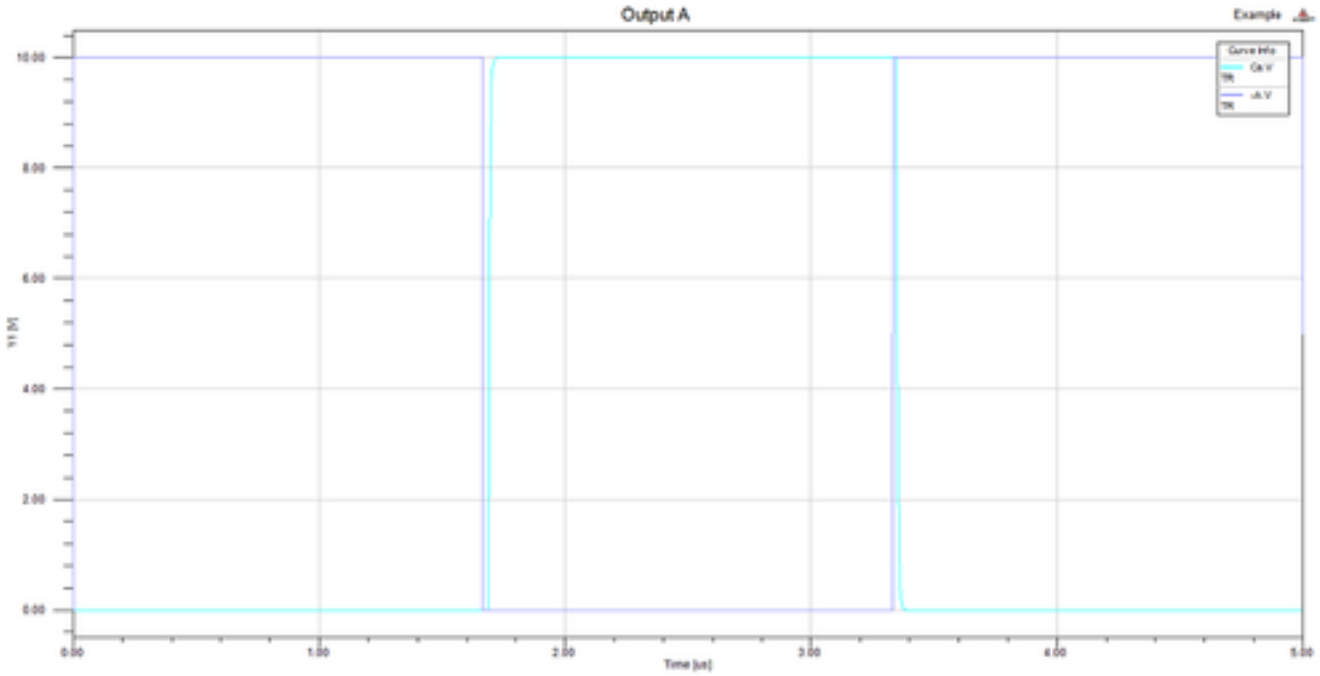


Figure 2. Example Circuit

Simulation results :



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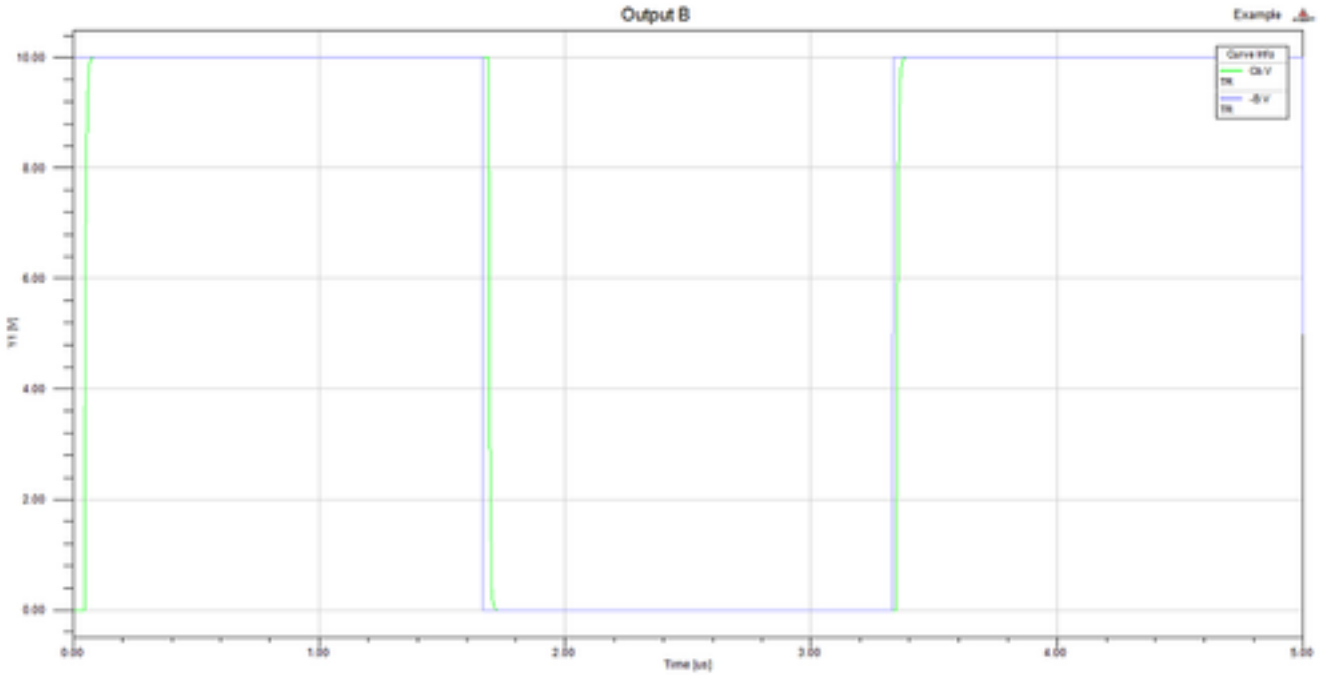

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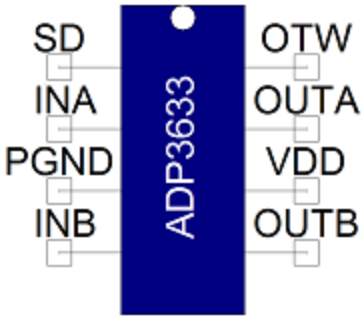
ADP3633: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *ADP362x/ADP363x* is a family of high current and dual high speed drivers, capable of driving two independent N-channel power MOSFETs. The family uses the industry-standard footprint but adds high speed switching performance and improved system reliability. The family has an internal temperature sensor and provides two levels of over-temperature protection, an over-temperature warning, and an over-temperature shutdown at extreme junction temperatures. The SD function, generated from a precise internal comparator, provides fast system enable or shutdown. This feature allows redundant overvoltage protection, complementing the protection inside the main controller device, or provides safe system shutdown in the event of an over-temperature warning. The wide input voltage range allows the driver to be compatible with both analog and digital PWM controllers. Digital power controllers are supplied from a low voltage supply, and the driver is supplied from a higher voltage supply. The *ADP362x/ADP363x* family adds UVLO and hysteresis functions, allowing safe startup and shutdown of the higher voltage supply

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when used with low voltage digital controllers. The device family is available in thermally enhanced SOIC_N_EP and MINI_SO_EP packaging to maximize high frequency and current switching in a small printed circuit board (PCB) area.

Inputs are modeled with voltage meters and resistances. The drivers outputs are modeled with ideal switches and resistances. The logic and delays are modeled with state machines.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	SD	Output Shutdown. When high, this pin disables normal operation, forcing OUTA and OUTB low.
2	INA	Inverted Input Pin for Channel A Gate Driver.
3	PGND	Ground. This pin should be closely connected to the source of the power MOSFET.
4	INB	Inverted Input Pin for Channel B Gate Driver.
5	OUTB	Output Pin for Channel B Gate Driver.
6	VDD	Power Supply Voltage. Bypass this pin to PGND with a ~1 µF to 5 µF ceramic capacitor.
7	OUTA	Output Pin for Channel A Gate Driver.
8	OTW	Overtemperature Warning Flag. Open drain, active low.

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Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

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SUPPLY						
Supply Voltage Range		4.5		18	10	V
Supply Current	No switching, INA and INB disabled		1.2	3	1.2	mA
Standby Current			1.2	3	1.2	mA
UVLO						
Turn-On Threshold Voltage		8.0	8.7	9.5	8.7	V
Turn-Off Threshold Voltage		7.0	7.7	8.5	7.7	V
Hysteresis			1.0		1.0	V
DIGITAL INPUTS						
Input Voltage High		2			2	V
Input Voltage Low				0.8	0.8	V
Input Current	$0\ V < V_{IN} < V_{DD}$	-20		20	-20/20	uA
SD Threshold High		1.19	1.28	1.38	1.28	V
SD Threshold Low		0.95	1	1.05	1	V
SD Hysteresis			0.28		0.28	V
Internal Pull-up/Pull-Down Current			6		6	uA
OUTPUTS						
Output Resistance, Unbiased	VDD = PGND		80		80	kOhm
Peak Source Current			4		4	A
Peak Sink Current			-4		-4	A
SWITCHING TIME						

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OUTA, OUTB Rise Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Fall Time	C_{LOAD} = 2.2 nF		10	25	10	ns
OUTA, OUTB Rise Propagation Delay	C_{LOAD} = 2.2 nF		14	30	14	ns
OUTA, OUTB Rise Time Propagation Delay	C_{LOAD} = 2.2 nF		22	35	22	ns
SD Propaga-tion Delay Low			32	45	32	ns
SD Propaga-tion Delay High			48	75	48	ns
Delay Match-ing Between Channels			2			ns
OVERTEMPERATURE PROTECTION				NOT IMPLEMENTED		

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Example circuit :

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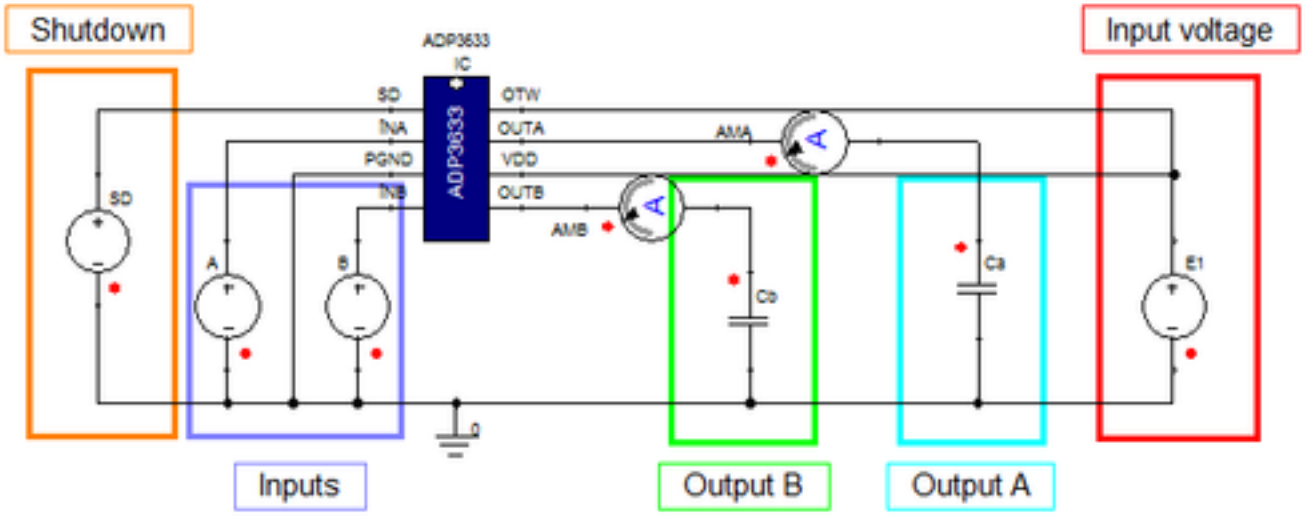
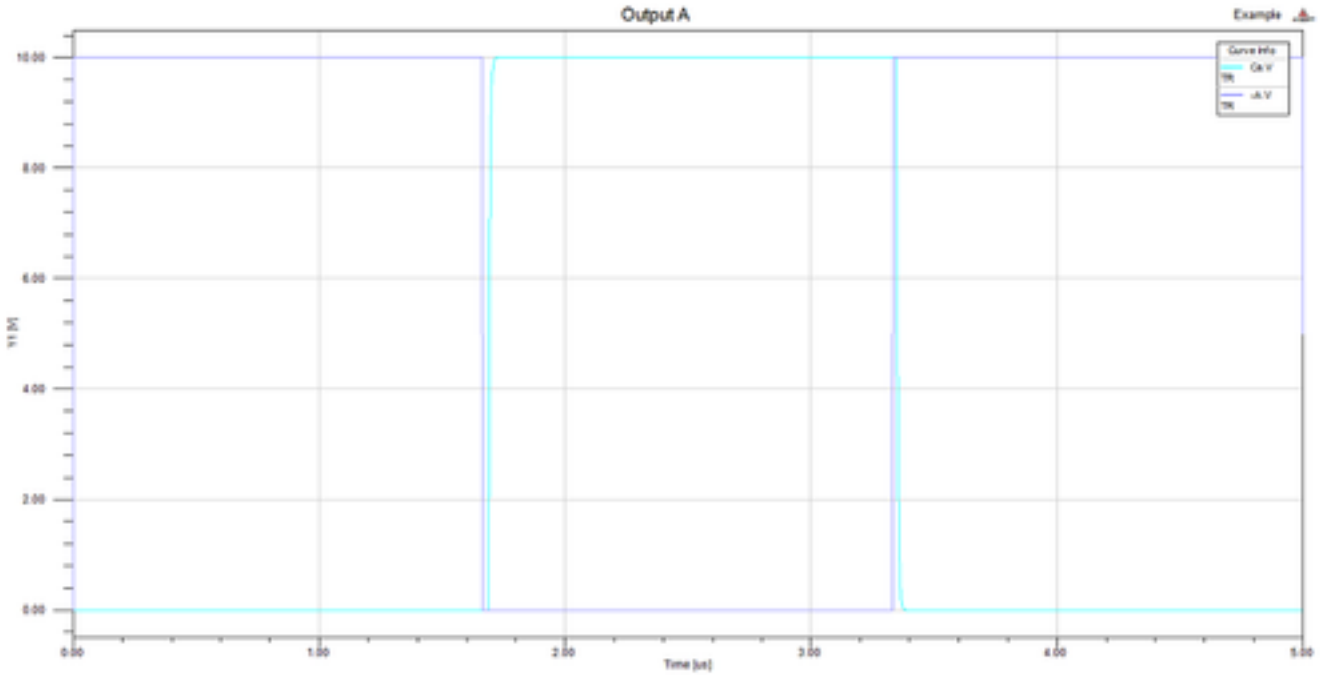


Figure 2. Example Circuit

Simulation results :



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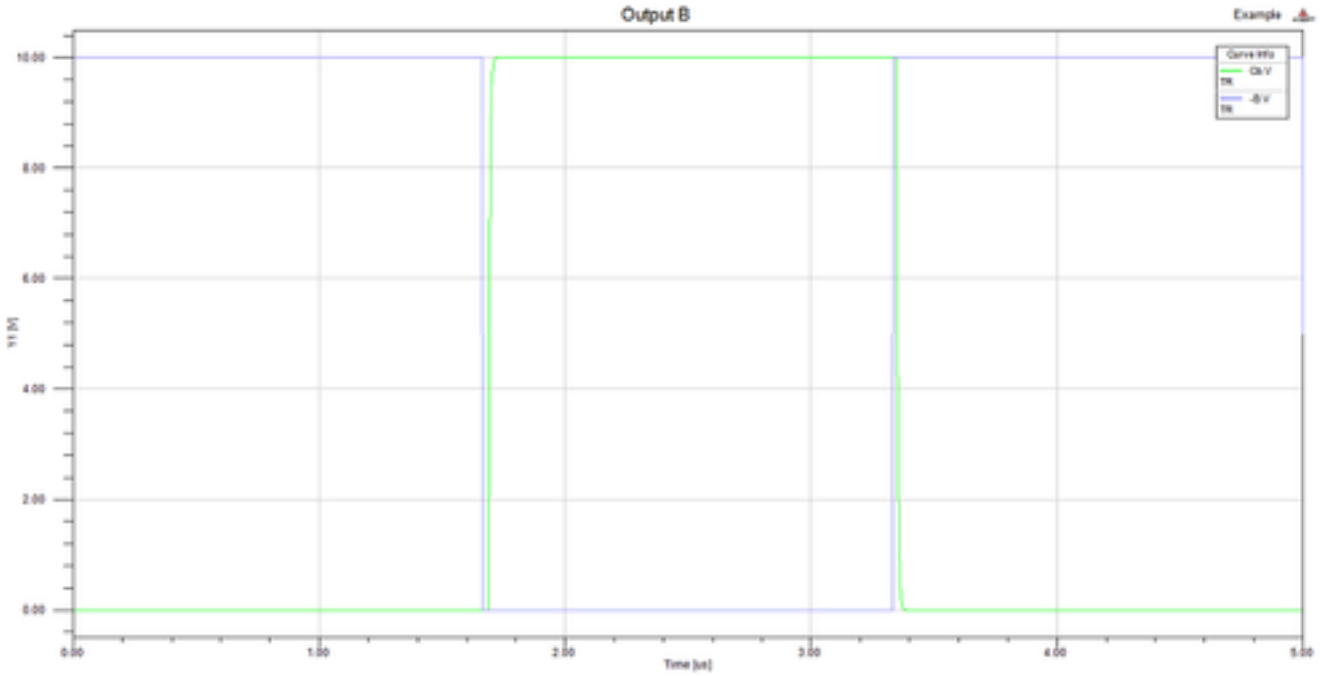

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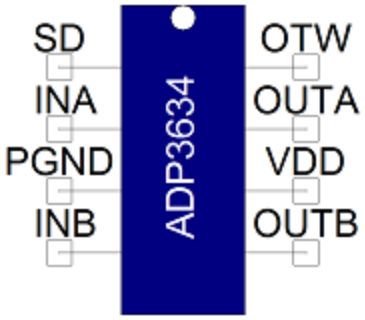
ADP3634: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *ADP362x/ADP363x* is a family of high current and dual high speed drivers, capable of driving two independent N-channel power MOSFETs. The family uses the industry-standard footprint but adds high speed switching performance and improved system reliability. The family has an internal temperature sensor and provides two levels of over-temperature protection, an over-temperature warning, and an over-temperature shutdown at extreme junction temperatures. The SD function, generated from a precise internal comparator, provides fast system enable or shutdown. This feature allows redundant overvoltage protection, complementing the protection inside the main controller device, or provides safe system shutdown in the event of an over-temperature warning. The wide input voltage range allows the driver to be compatible with both analog and digital PWM controllers. Digital power controllers are supplied from a low voltage supply, and the driver is supplied from a higher voltage supply. The *ADP362x/ADP363x* family adds UVLO and hysteresis functions, allowing safe startup and shutdown of the higher voltage supply

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Table 1

PIN	NAME	FUNCTION
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Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

SUPPLY						
Supply Voltage Range		4.5		18	10	V
Supply Current	No switching, INA and INB disabled		1.2	3	1.2	mA
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Turn-On Threshold Voltage		8.0	8.7	9.5	8.7	V
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SD Hysteresis			0.28		0.28	V
Internal Pull-up/Pull-Down Current			6		6	uA
OUTPUTS						
Output Resistance, Unbiased	VDD = PGND		80		80	kOhm
Peak Source Current			4		4	A
Peak Sink Current			-4		-4	A
SWITCHING TIME						

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OUTA, OUTB Rise Time	C_{LOAD} = 2.2 nF		10	25	10	ns
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OUTA, OUTB Rise Time Propagation Delay	C_{LOAD} = 2.2 nF		22	35	22	ns
SD Propaga-tion Delay Low			32	45	32	ns
SD Propaga-tion Delay High			48	75	48	ns
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OVERTEMPERATURE PROTECTION				NOT IMPLEMENTED		

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Example circuit :

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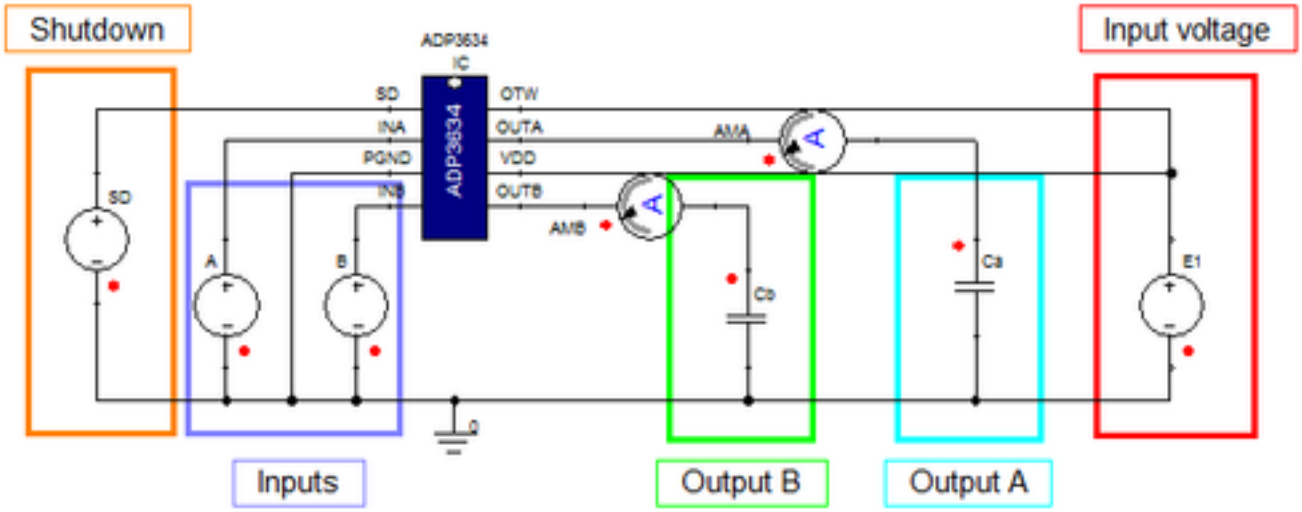

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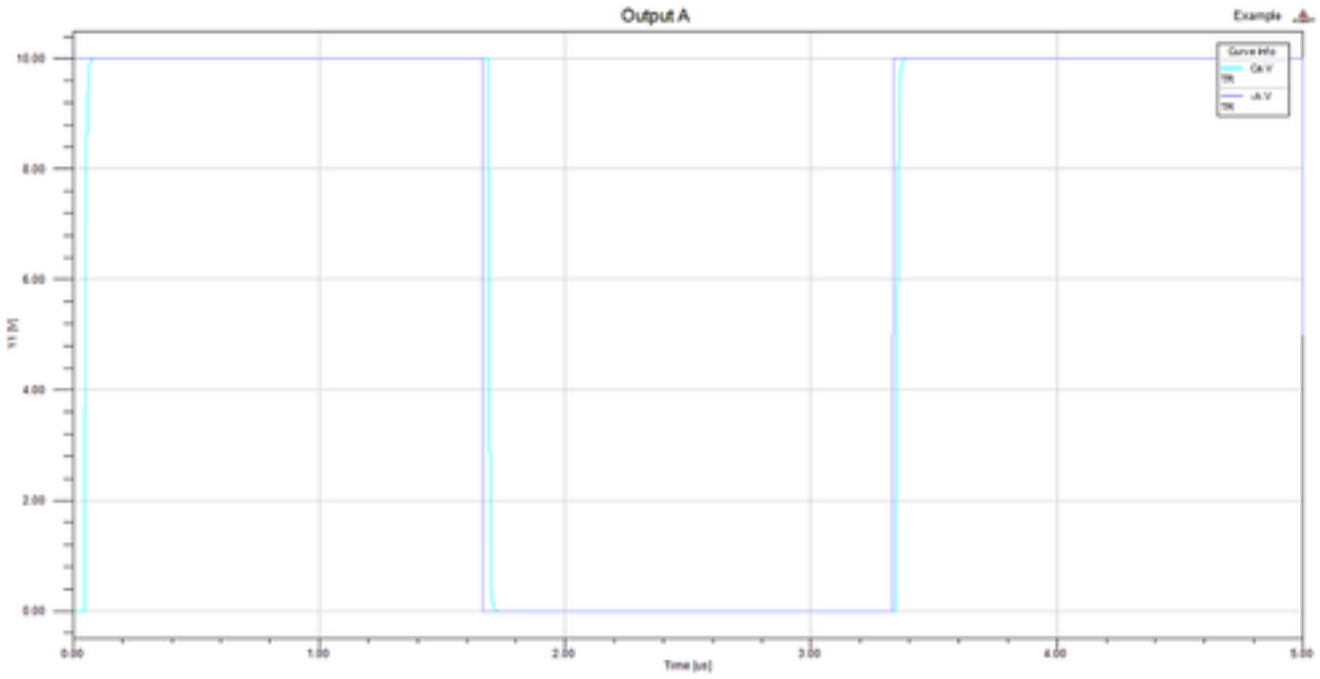

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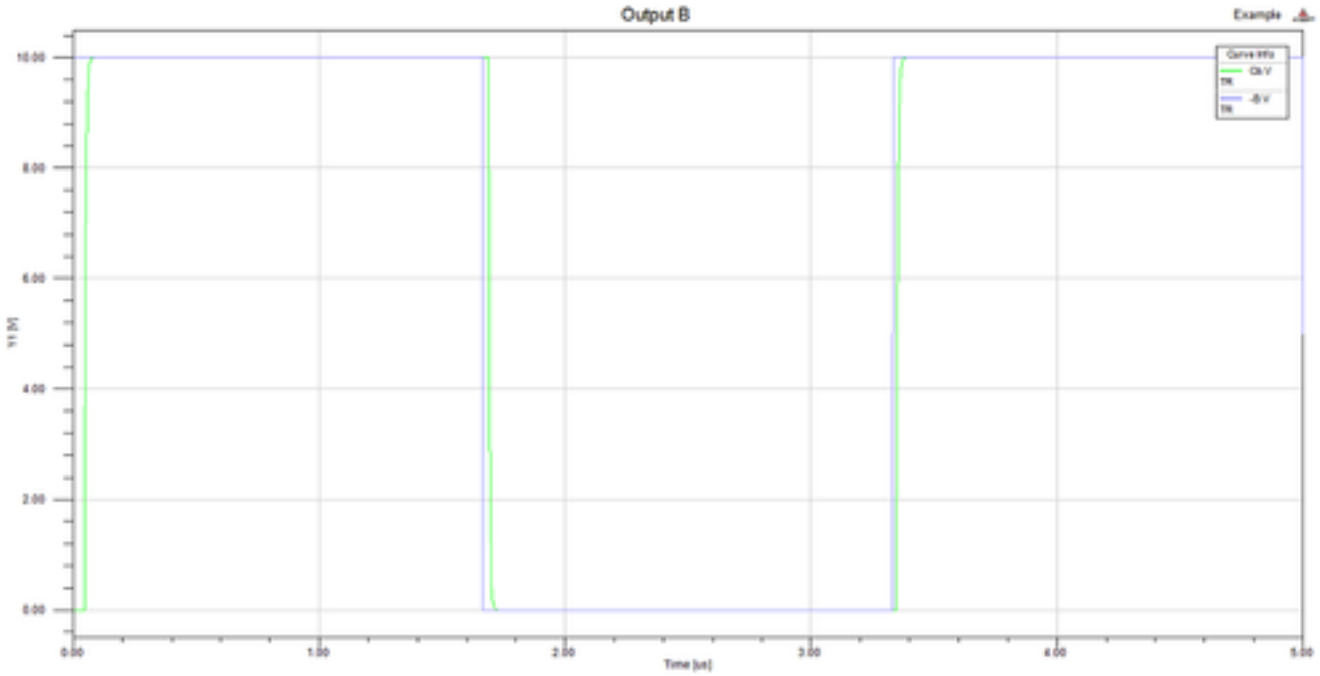

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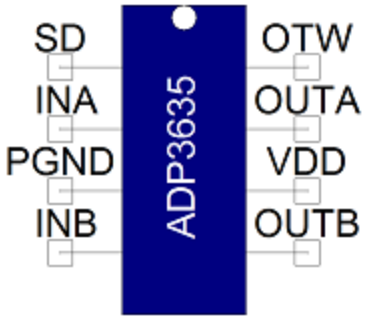
ADP3635: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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DIGITAL INPUTS						
Input Voltage High		2			2	V
Input Voltage Low				0.8	0.8	V
Input Current	$0\ V < V_{IN} < V_{DD}$	-20		20	-20/20	uA
SD Threshold High		1.19	1.28	1.38	1.28	V
SD Threshold Low		0.95	1	1.05	1	V
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Internal Pull-up/Pull-Down Current			6		6	uA
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Output Resistance, Unbiased	VDD = PGND		80		80	kOhm
Peak Source Current			4		4	A
Peak Sink Current			-4		-4	A
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Examples

Example circuit :

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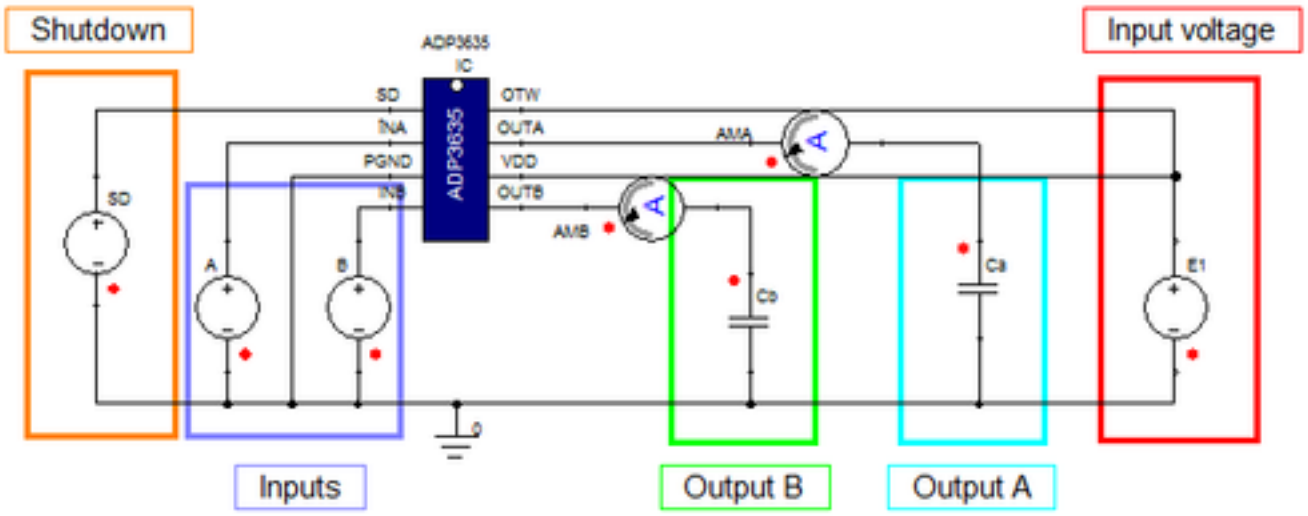
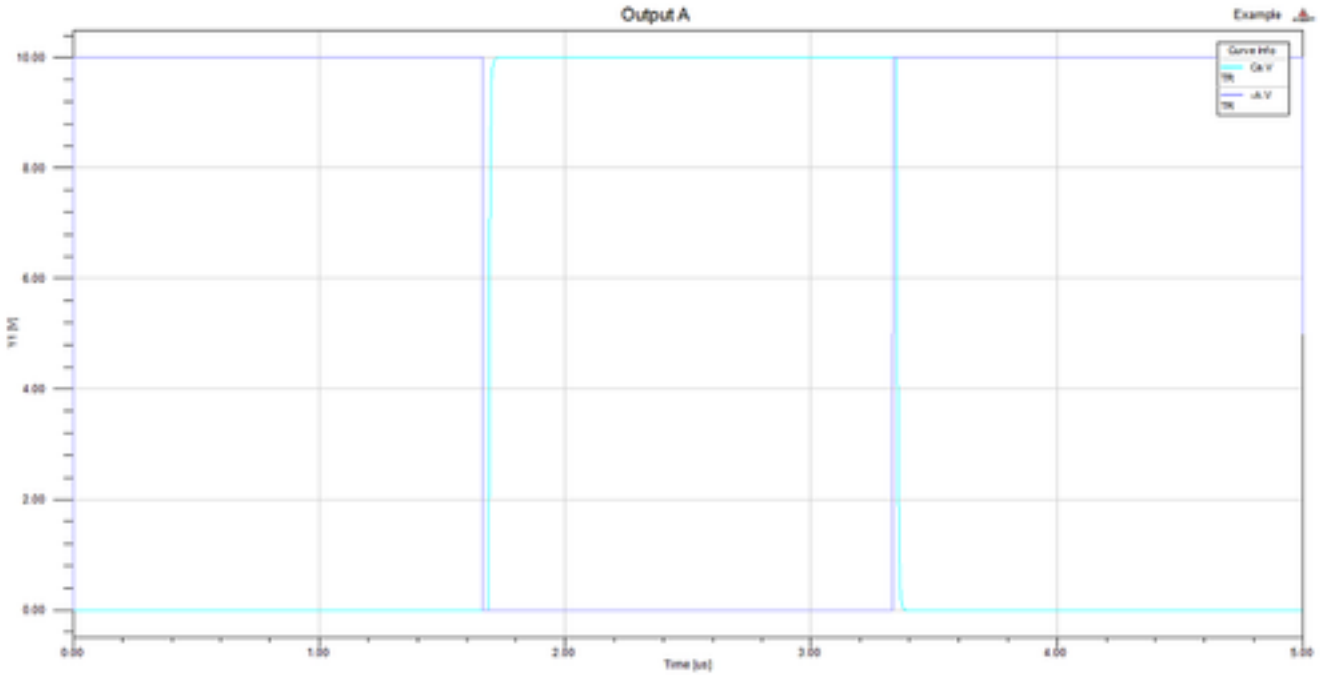


Figure 2. Example Circuit

Simulation results :



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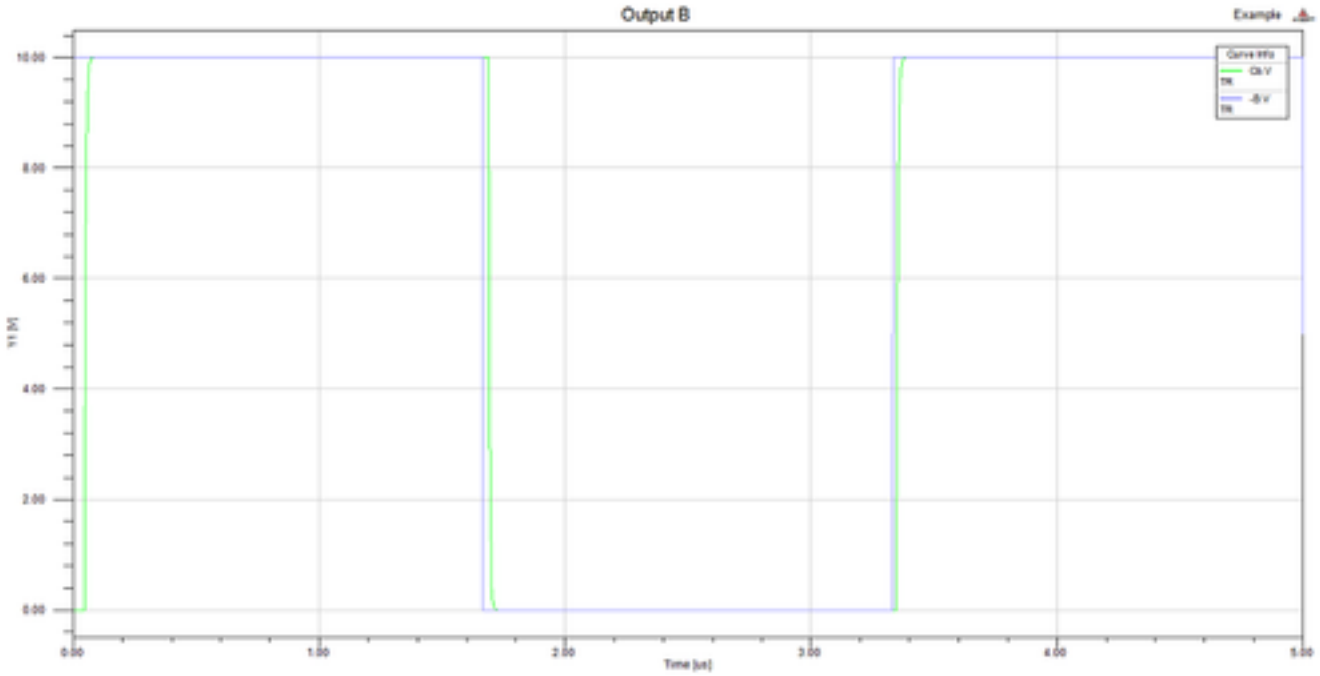

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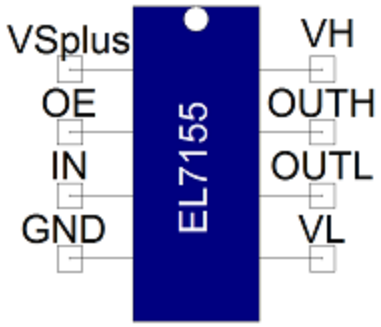
EL7155: Intersil

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *EL7155* high performance pin driver with 3-state is suited to many ATE and level-shifting applications. The 3.5A peak drive capability makes this part an excellent choice when driving high capacitance loads. Output pins OUTH and OUTL are connected to input pins VH and VL respectively, depending on the status of the IN pin. One of the output pins is always in tri-state, except when the OE pin is active low, in which case both outputs are in 3-state mode. The isolation of the output FETs from the power supplies enables VH and VL to be set independently, enabling level-shifting to be implemented. This pin driver has improved performance over existing pin drivers. It is specifically designed to operate at voltages down to 0V across the switch elements while maintaining good speed and on-resistance characteristics. Available in 8-Pin SO and 8-Pin PDIP packages, the *EL7155* is specified for operation over the full -40°C to +85°C temperature range.

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The model consists of state machines that control the logic and delays of the switches of high and low sides. The other set of state machines controls the Output Enable function to put the output in three-state (floating.) When the OE pin is low, the output is 3-state (floating.) The output voltage is the parasitic capacitance's voltage. It can be any voltage between VH and VL, depending on the previous state. At 3-state, output voltage can be pushed to any voltage between VH and VL. The output voltage can't be pushed higher than VH or lower than VL since the body diode at the output stage will turn on.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VS+	Positive Supply Voltage
2	OE	Output Enable
3	IN	Input
4	GND	Ground
5	VL	Negative Supply Voltage
6	OUTL	Lower Switch Output
7	OUTH	Upper Switch Output
8	VH	Upper Output Voltage

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Parameters

VS+ = +15V, VH = +15V, VL = 0V, TA = 25°C, unless otherwise specified.

Table 2

PARAM-ETER	DESCRI-PTION	CONDI TION	MIN	TYP	MAX	MODE-L	U NIT

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

INPUT							
V_{IH}	Logic '1' Input Voltage		2.4			2.4	V
I_{IH}	Logic '1' Input Current	V_{IH} = V_S+		0.1	10	0	uA
V_{IL}	Logic '0' Input Voltage				0.8	0.8	V
I_{IL}	Logic '0' Input Current	V_{IL} = 0V		0.1	10	0	uA
C_{IN}	Input Capacitance			3.5		0	pF
R_{IN}	Input Resistance			50		∞	MΩ
OUTPUT							
R_{OVH}	ON Resistance V_H to OUT_H	I_{OUT} = -200mA		2.7	4.5	2.7	Ω
R_{OVL}	ON Resistance V_L to OUT_L	I_{OUT} = +200mA		3.5	5.5	3.5	Ω
I_{OUT}	Output Leakage Current	OE = 0V, OUT_H = V_L, OUT_L = V_S+		0.1	10	0	uA
I_{PK}	Peak Output Current (linear resistive operation)	Source		3.5		X	A
		Sink		3.5		X	A
I_{DC}	Continuous Output Current	Source/ Sink	200			X	mA
POWER SUPPLY							
I_S	Power	Inputs		1.3	3	0	mA

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	Current	+					
I_{VH}	Off Leakage at V_H	V_H = 0V		4	10	0	uA
SWITCHING CHARACTERISTICS							
t_R	Rise Time	C_L = 2000pF		14.5			ns
t_F	Fall Time	C_L = 2000pF		15			ns
$t_{RF\Delta}$	t_R, t_F Mismatch	C_L = 2000pF		0.5			ns
t_{D-1}	Turn-Off Delay Time	C_L = 2000pF		9.5		9.5	ns
t_{D-2}	Turn-On Delay Time	C_L = 2000pF		10		10	ns
$t_{D\Delta}$	t_{D-1}-t_{D-2} Mismatch	C_L = 2000pF		0.5		0.5	ns
t_{D-3}	3-state Delay Enable			10		10	ns
t_{D-4}	3-state Delay Disable			10		10	ns

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Examples

Example circuit :

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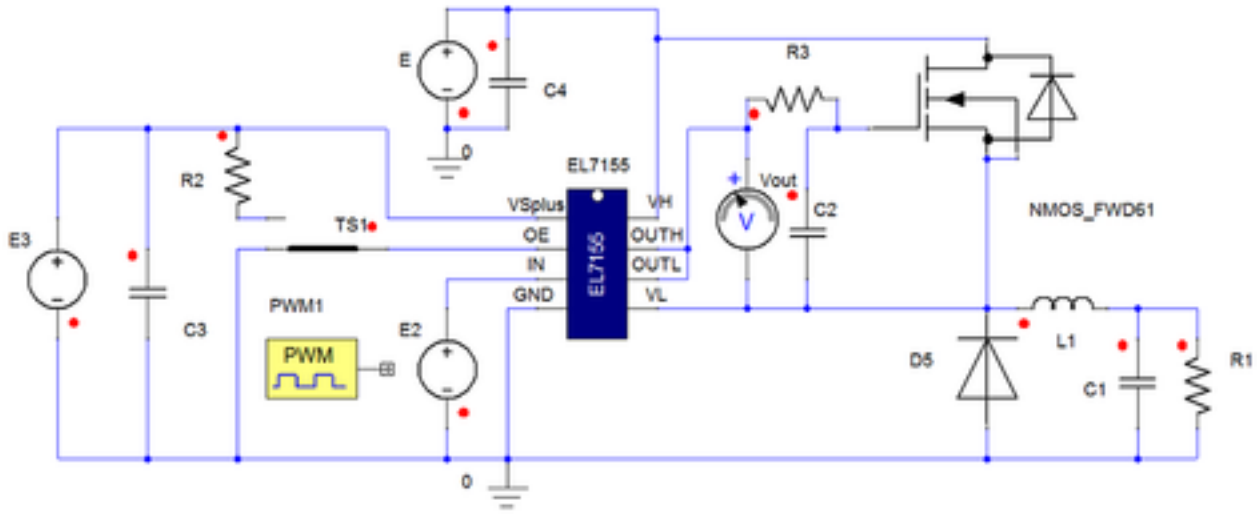
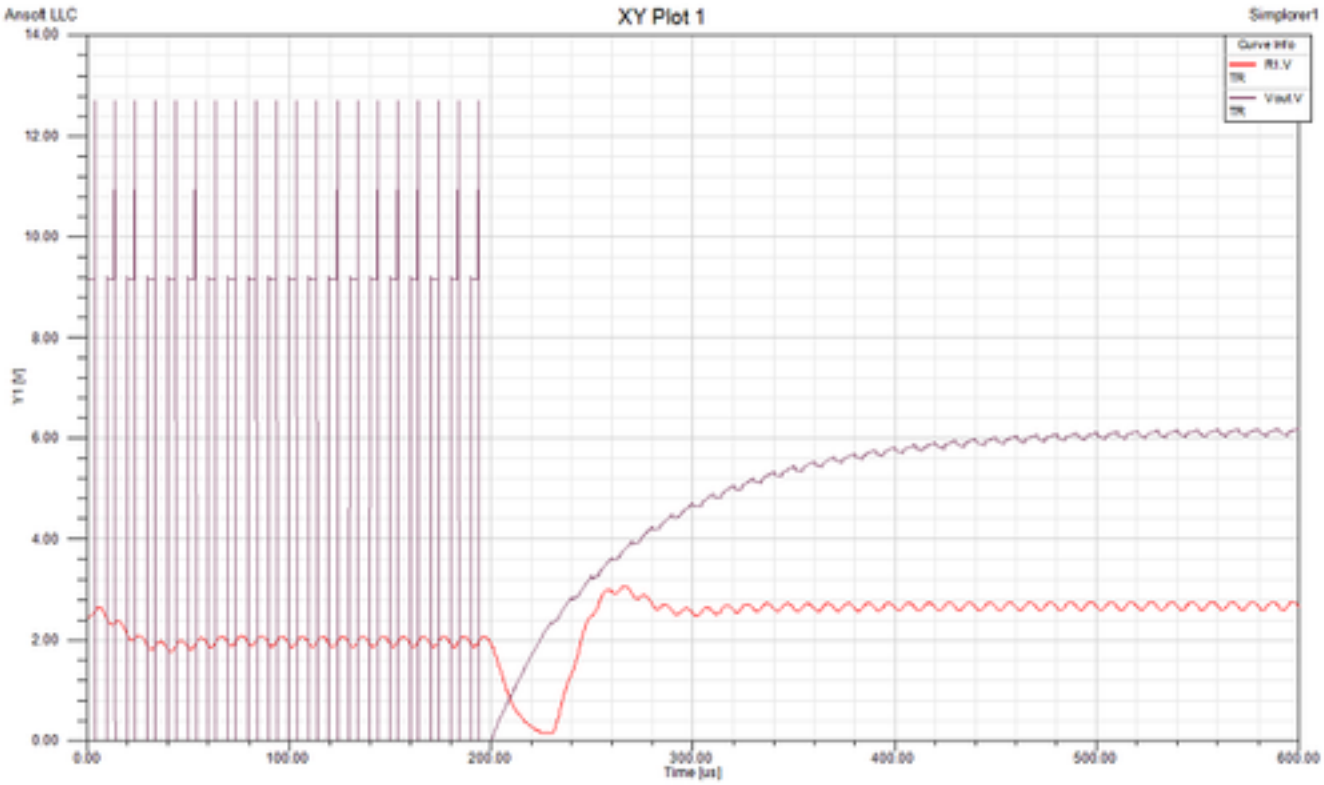


Figure 2. Example Circuit

Simulation results :



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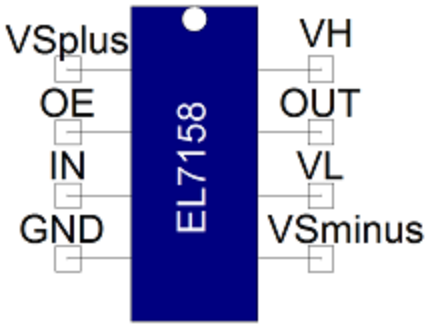
EL7158: Intersil

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *EL7158* high performance pin driver with three-state is suited to many ATE and level-shifting applications. The 12A peak drive capability makes this part an excellent choice when driving high capacitance loads. The output pin OUT is connected to input pins VH or VL respectively, depending on the status of the IN pin. When the OE pin is active low, the output is placed in the three-state mode. The isolation of the output FETs from the power supplies enables VH and VL to be set independently, enabling level-shifting to be implemented. Related to the EL7155, the *EL7158* adds a lower supply pin VS- and makes VL an isolated and independent input. This feature adds applications flexibility and improves switching response due to the increased enhancement of the output FETs. This pin driver has improved performance over existing pin drivers. It is specifically designed to operate at voltages down to 0V across the switch elements while maintaining good speed and on-resistance characteristics. Available in the 8-pin SO package, the EL7158 is specified for operation over the full -40°C to +85°C temperature range.

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The model consist of state machines that controls the logic and delays of the switches of high and low sides. The other set of state machines controls the Output Enable function to put the output in three-state (floating). The output voltage is the parasitic capacitance's voltage. It can be any voltage between VH and VL, depending on the previous state. At three-state, the output voltage can be pushed to any voltage between VH and VL. The output voltage can't be pushed higher than VH or lower than VL since the body diode at the output stage will turn on.

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Conservative Pins

Table 1

Pin #	Pin Name	Pin Function
1	Vs+	Positive Supply Voltage
2	OE	Output Enable
3	IN	Input
4	GND	Ground
5	VS-	Negative Supply Voltage
6	VL	Lower Output Voltage
7	OUT	Output
8	VH	High Output Voltage

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Parameters

VS+ = +12V, VH = +12V, VL = 0V, VS- = 0V, TA = 25°C, unless otherwise specified.

Table 2

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	MODEL	UNIT

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

INPUT							
VIH	Logic '1' Input Voltage		2.4			2.4	V
IIH	Logic '1' Input Current	VIH = VS+		0.1	10	0	uA
VIL	Logic '0' Input Voltage				0.8	0.8	V
IIL	Logic '0' Input Current	VIL = 0V		0.1	10	0	uA
CIN	Input Capacitance			3.5		0	pF
RIN	Input Resistance			50		∞	MΩ
OUTPUT							
ROVH	ON Resistance VH to OUT	IOUT = -500mA		0.5	1	0.5	Ω
ROVL	ON Resistance VL to OUT	IOUT = +500mA		0.5	1	0.5	Ω
IOUT	Output Leakage Current	OE = 0V, OUT = VH/VL		0.1	10	0	uA
IPK	Peak Output Current (linear resistive operation)	Source		12		X	A
		Sink		12		X	A
IDC	Continuous Output Current	Source/Sink	500			X	mA
POWER SUPPLY							
IS	Power Supply	Inputs = VS+		1.3	3	0	mA

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I_{VH}	Off Leakage at V_H and V_L	V_H, V_L = 0V		4	10	0	uA
	SWITCHING CHARACTERISTICS						
t_R	Rise Time	C_L = 2 000pF		12.0		12	ns
t_F	Fall Time	C_L = 2 000pF		12.2		12.2	ns
$t_{RF\Delta}$	t_R, t_F Mismatch	C_L = 2 000pF		0.2		0.2	ns
t_{D-1}	Turn-Off Delay Time	C_L = 2 000pF		22.5		22.5	ns
t_{D-2}	Turn-On Delay Time	C_L = 2 000pF		22.0		22	ns
$t_{D\Delta}$	t_{D-1}-t_{D-2} Mismatch	C_L = 2 000pF		0.5		0.5	ns
t_{D-3}	Three-State Delay Enable			22		22	ns
t_{D-4}	Three-State Delay Disable			22		22	ns
SR+	V_{OUT}+ Slew Rate	R_{LOAD} = 6Ω		800		∞	V/us
SR-	V_{OUT}- Slew Rate	R_{LOAD} = 6Ω		800		∞	V/us

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Examples

Example circuit :

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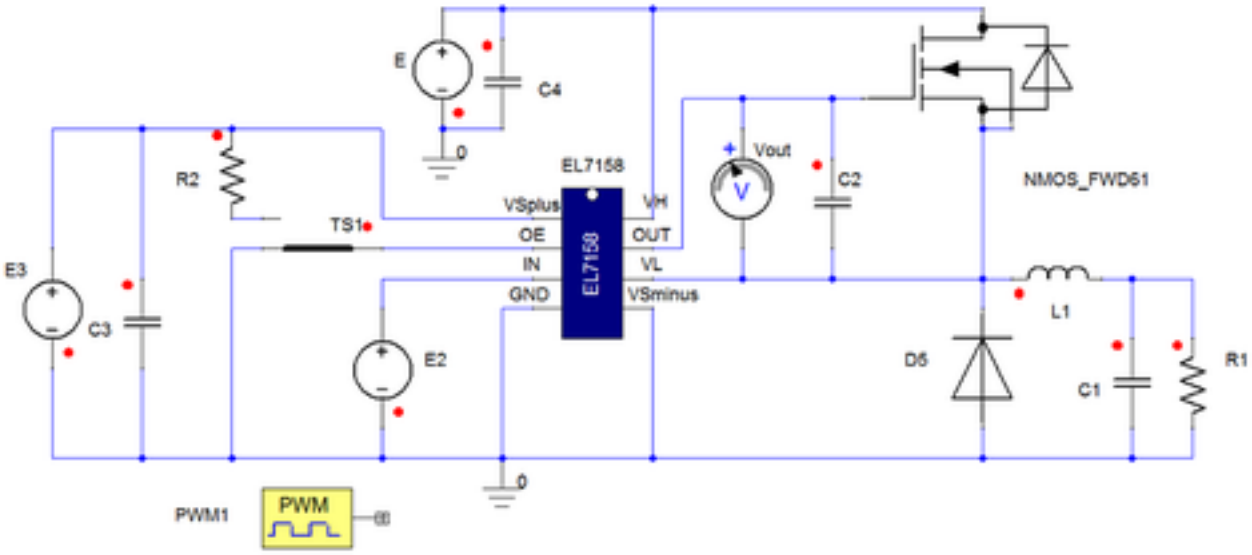

Figure 2. Example Circuit

Simulation results :

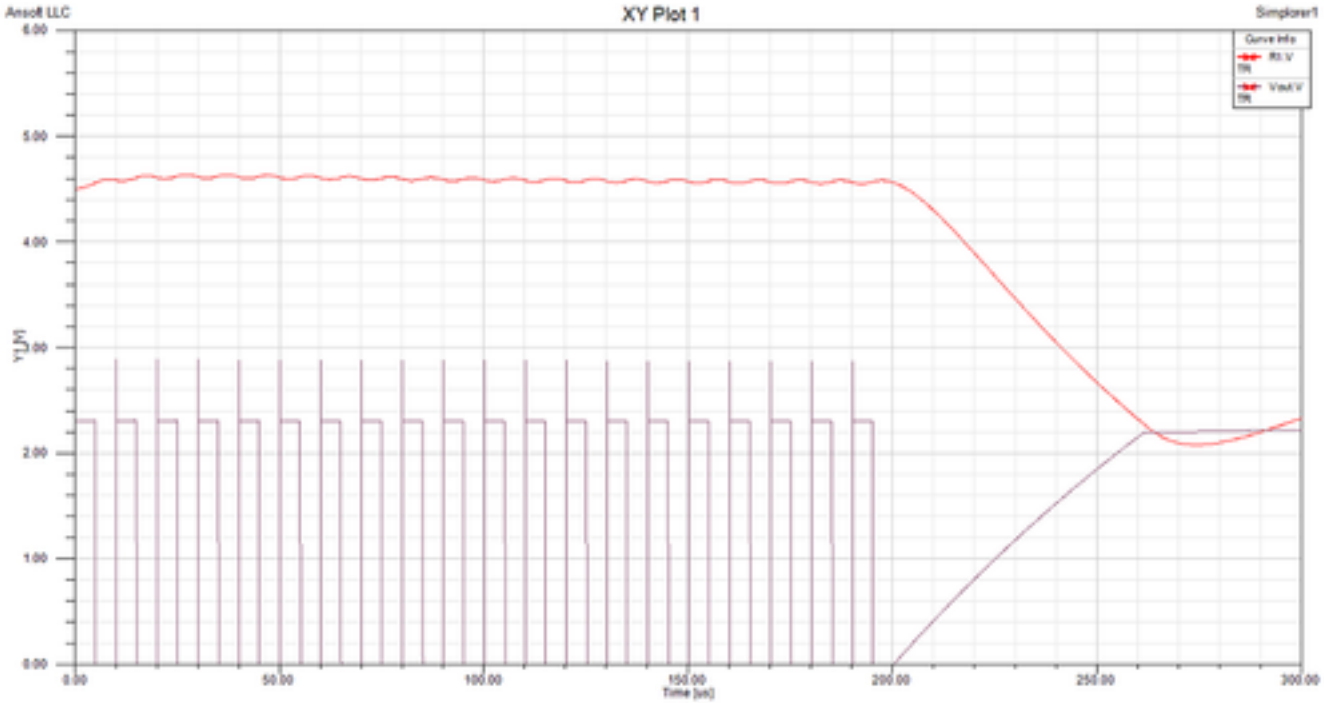

Figure 3. Simulation results

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References

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

IR2110: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

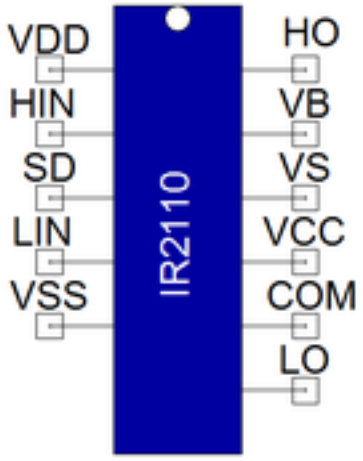

Figure 1. Component symbol

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Description

The International Rectifier *IR2110* is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels.

There are three parts clearly differentiated: the input part, in which control voltages are measured. State machines on the middle control the switches of the output signals (high and low side separately) and implements the real switching delays as well as the undervoltage protection and the shutdown system. The switches on the right side simulate the totem-pole outputs.

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Conservative Pins

Table 1

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	Hide side gate driver output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate driver output
COM	Low side return

Product summary:

Table 2

V_{OFFSET} (IR2110) (IR2113)	500V max. 600V max.
I_O+/-	2A / 2A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	120 & 94 ns

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Delay Matching (IR2110) (IR2113)	10 ns max. 20 ns max.

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Parameters

Comparison between model and real component.

Apart from the parameters appeared in the product summary section, which the model matches with, there are some others parameters implemented as well:

Table 3

PARAMETER	DEFINITION	IR2110	MODEL	UNITS
Static Electrical Characteristics				
V_{IH}	Logic '1' input voltage	9.5 (min)	9.5	V
V_{IL}	Logic '0' input voltage	6.0 (max)	6.0	V
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold	8.6	8.6	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold	8.2	8.2	V
V_{CCUV+}	V_{cc} supply under-voltage positive going threshold	8.5	8.5	V
V_{CCUV-}	V_{cc} supply under-voltage negative going threshold	8.2	8.2	V

Because of the pull down resistors connected to the input pins implemented inside the IC model, the input impedance is 100 kOhm (Zin=100kΩ) instead of infinite (as expected on an ideal model). Output impedance is zero (Zo=0). Temperature influence parameters as well as bias and leakage currents have not been implemented.

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Examples

In this circuit the IC provides the control signals of a half-bridge inverter with a resistive load, using a capacitive voltage divider to get high and low sides. A lower frequency pulse voltage source is connected to SD pin to check the behavior of the logic input for shutdown. Vcc is 15V.

Example circuit :

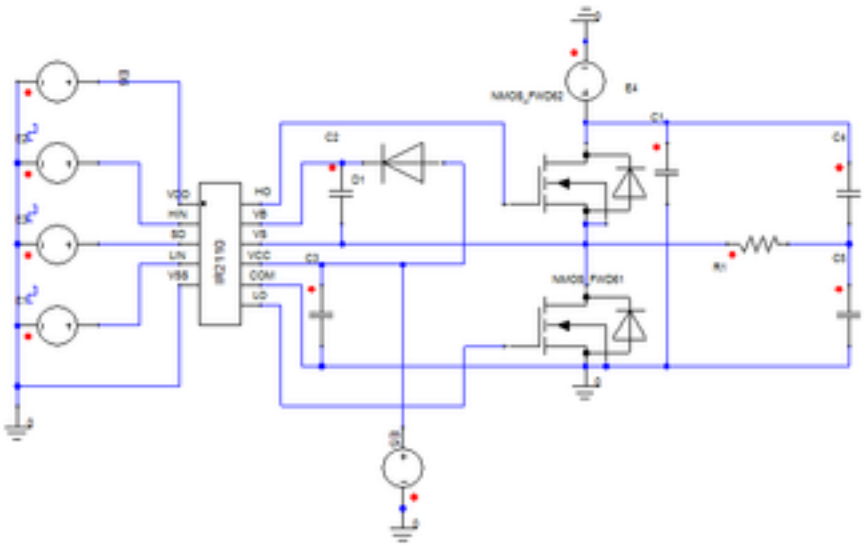

Figure 2. Example Circuit

Simulation results :

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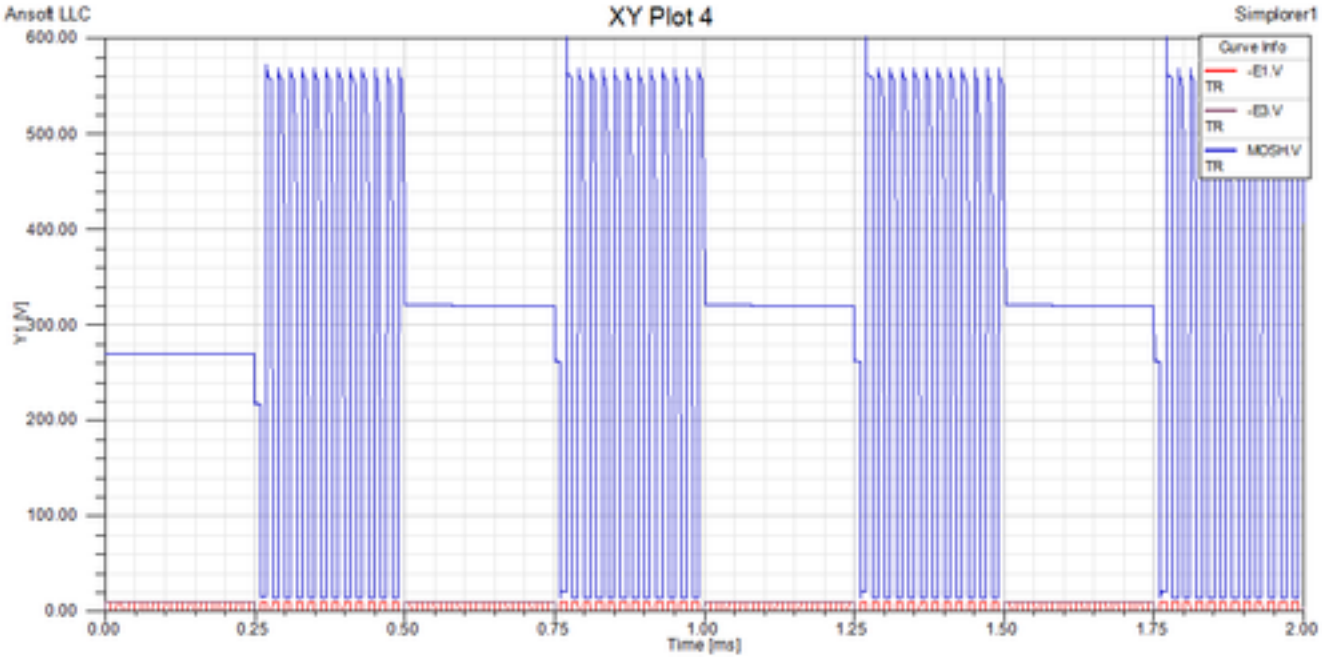
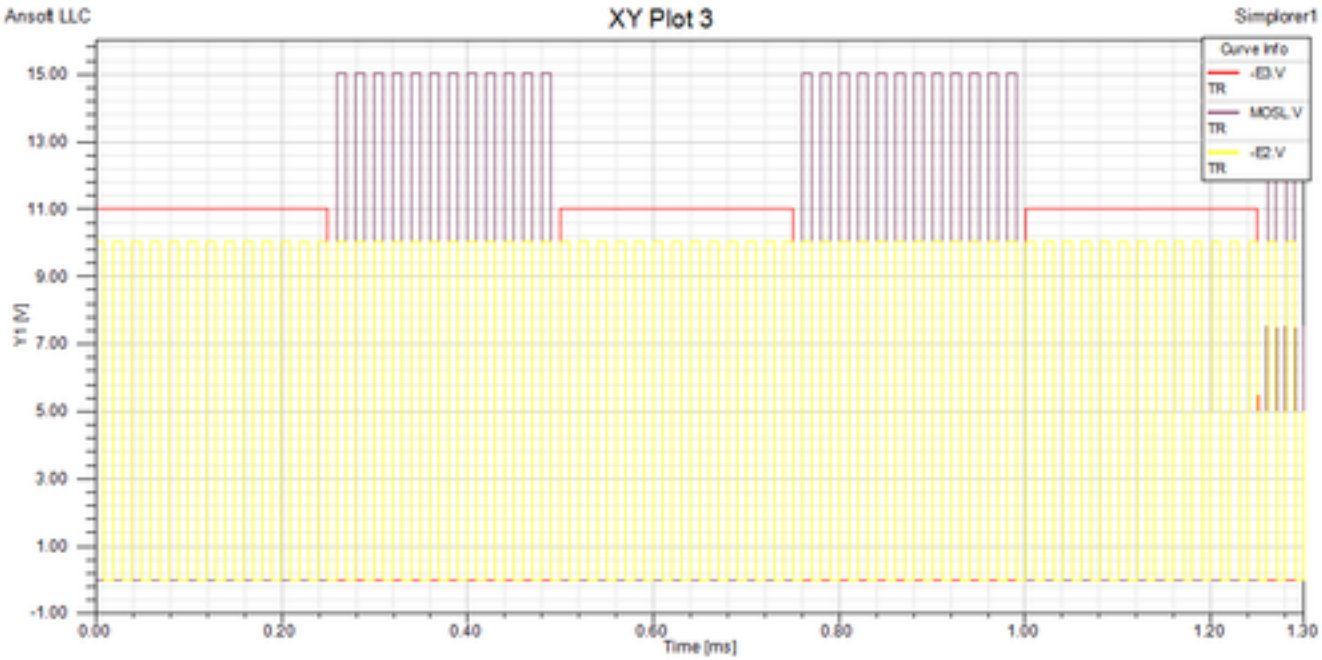


Blue: high side MOSFET gate voltage

Red: high side input voltage

Brown: shutdown input voltage



Brown: low side MOSFET gate voltage

Red: shutdown input voltage

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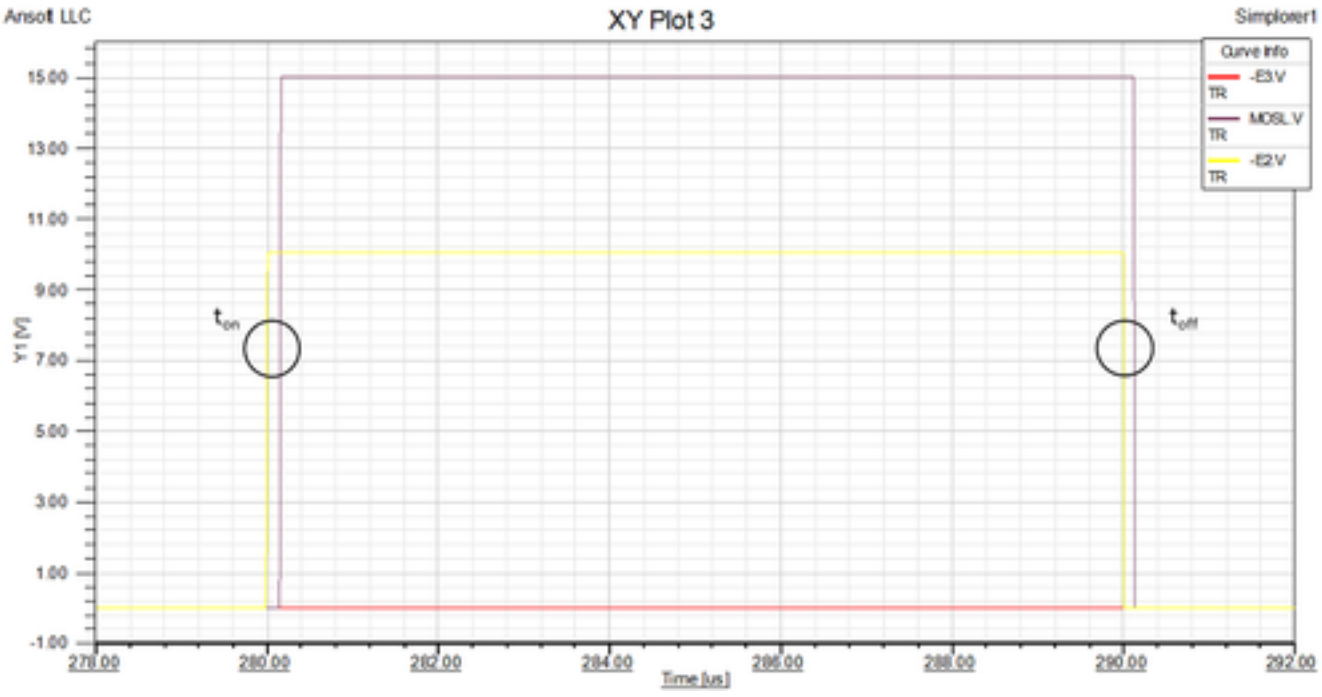
Yellow: low side input voltage

When SD (shutdown) is high, output HO and LO voltages fall to their low value.

Figure 3. Simulation results

Detail of timing implementation:



Brown: low side MOSFET gate voltage

Red: shutdown input voltage

Yellow: low side input voltage

Figure 4. Detail of timing implementation

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References

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IR2127: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

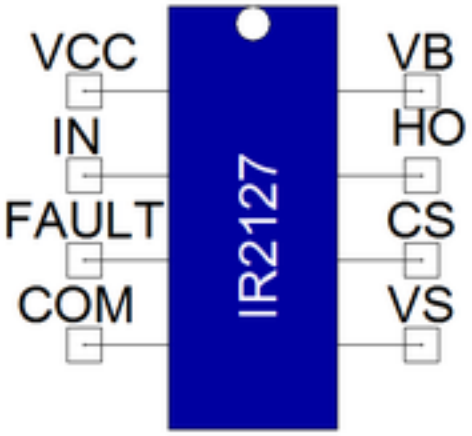

Figure 1. Component symbol

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Description

The *IR2127* is a high voltage, high speed power MOSFET and IGBT driver. The protection circuit detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain FAULT signal is provided to indicate that an over-current shutdown has occurred.

The operation of this IC is controlled by three states machines. The upper one controls the under-voltage protection. When Vb falls below 9V, output switches open. The middle state machine controls the switching on steady state, simulating the switching delays. The bottom one controls the overcurrent protection and the fault switch.

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Conservative Pins

Table 1

Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IR2127 / IR21271) out of phase with HO (IR2128)
FAULT	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Product summary:

Table 2

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT} (IR2127 / IR2128) (IR21271)	12 - 20V 9 - 20V
V_{CSth}	250 mV or 1.8V
$t_{on/off}$ (typ.)	200 & 150 ns

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Parameters

Comparison between model and real component.

Apart from the parameters appeared in the product summary section, which the model matches with, there are some others parameters implemented as well:

Table 3

PARAMETER	DEFINITION	IR2127	MODEL	UNITS
Static Electrical Characteristics				
V_{IH}	Logic '1' input voltage	3.0 (min)	3.0	V
V_{IL}	Logic '0' input voltage	0.8 (max)	0.8	V
V_{CSTH+}	CS input positive going threshold	250	250	mV
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold	10.3	10.3	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold	9.0	9.0	V

Temperature influence parameters as well as bias and leakage currents have not been implemented. Input and output impedances are ideal, so the input impedance is infinite (Zin=∞) and the output impedance is zero (Zo=0).

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Examples

In this circuit the IC controls a low side MOSFET with resistive load. When MOSFET gate voltage is high, the circuit is closed and the output voltage is zero. Fault pin is connected to a pull-up resistor. Vcc is 20V.

Example circuit :

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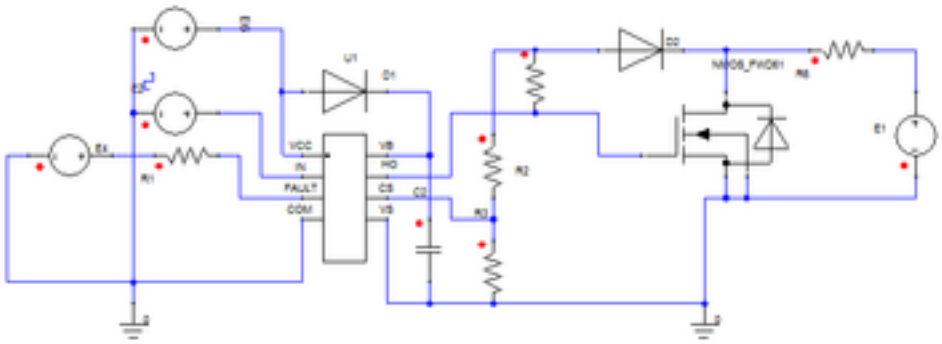
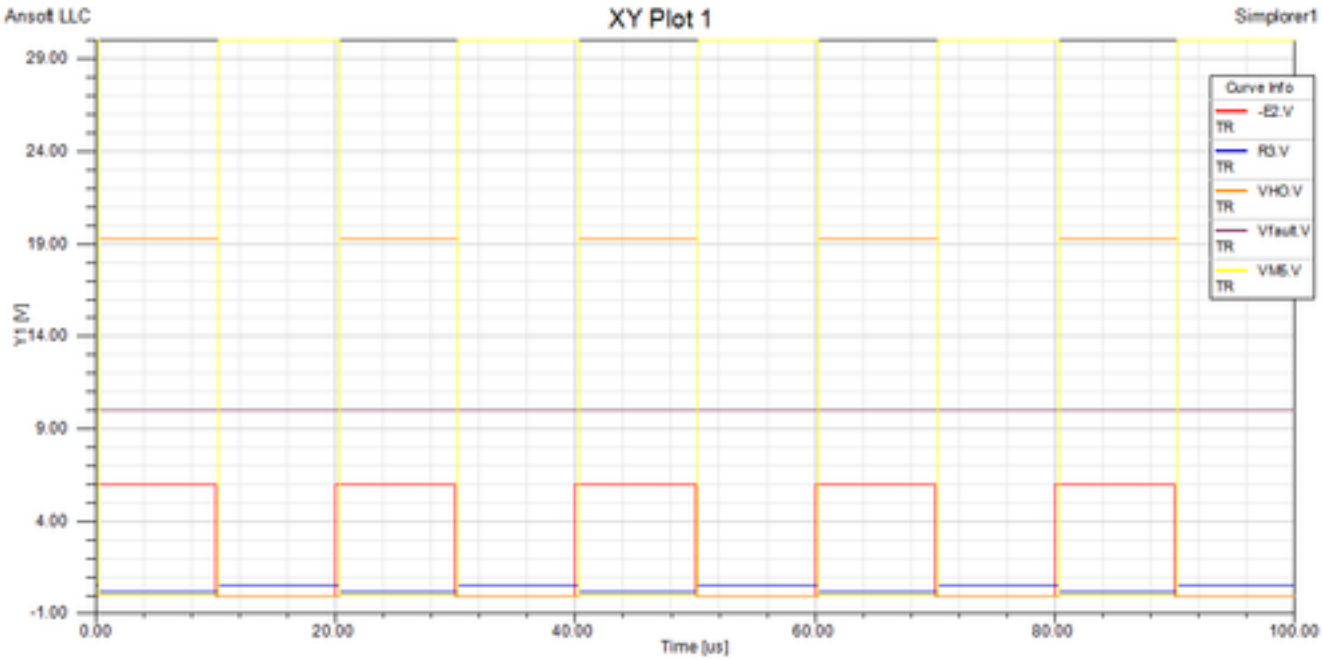


**Figure 2. Example Circuit **

Simulation results :

Steady state (no fault):



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Red: input voltage

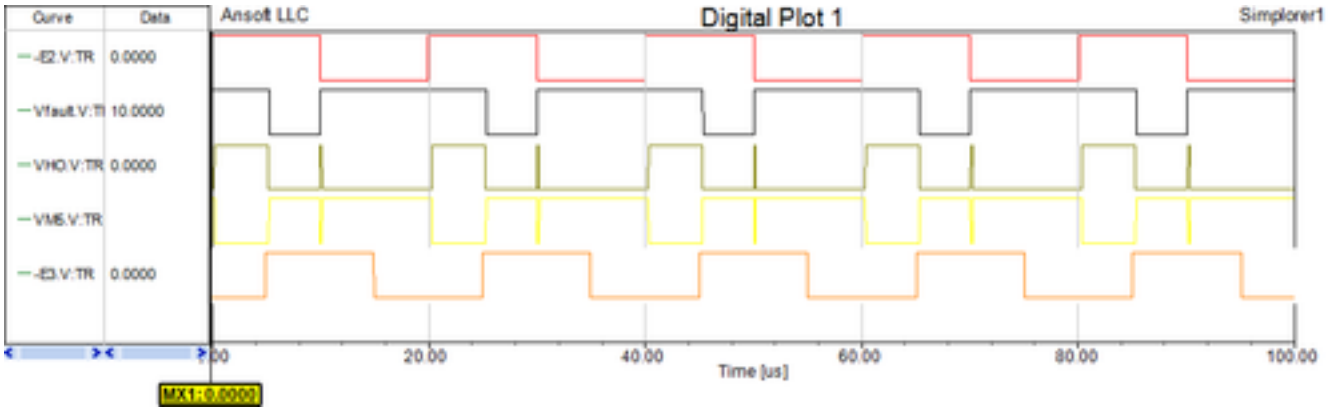
Blue: current sense voltage

Orange: MOSFET gate voltage (IC output)

Brown: fault voltage (negative logic)

Yellow: output voltage (to load)

Fault simulation:



Red: input voltage

Black: fault voltage (negative logic)

Green: MOSFET gate voltage (IC output)

Yellow: output voltage (to load)

Orange: current sense (CS) voltage

Figure 3. Simulation results

When CS voltage is higher than 0.25 V, open drain fault MOSFET is closed and the fault pin gets connected to ground through a pull-down resistor. When fault is detected, output voltage falls to low level.

Detail of timing implementation:

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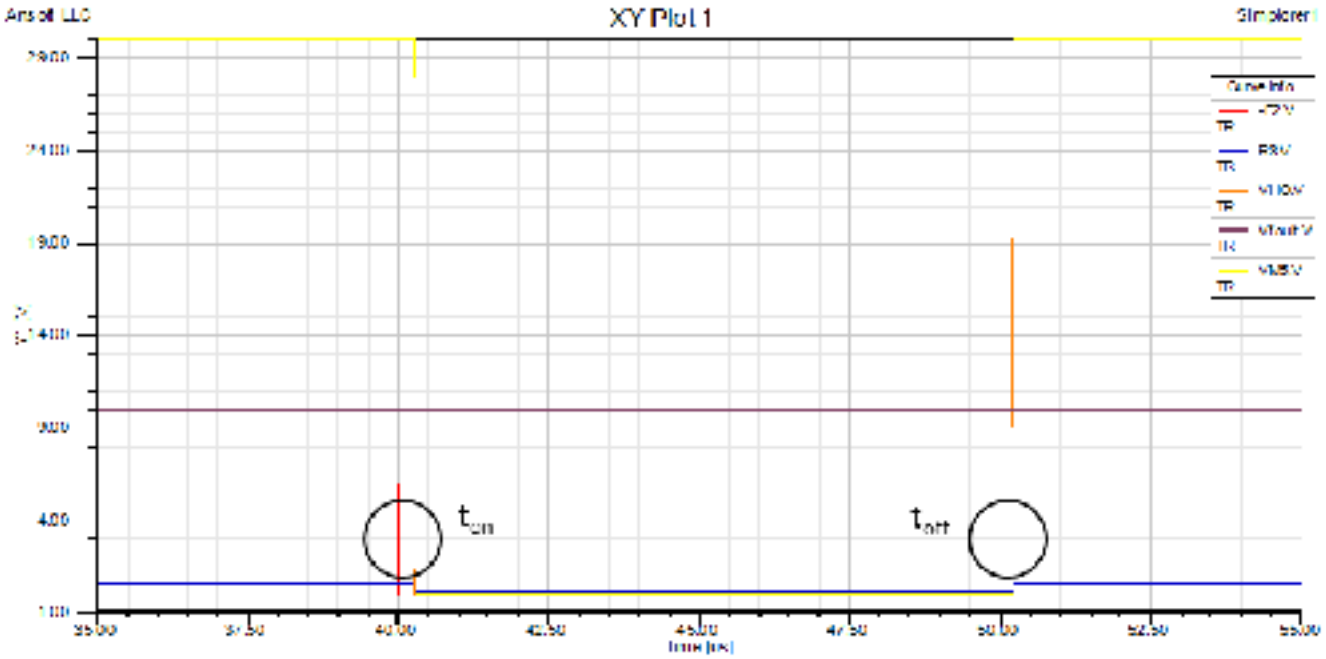

Red: input voltage

Blue: current sense voltage

Orange: MOSFET gate voltage (IC output)

Brown: fault voltage (negative logic)

Yellow: output voltage (to load)

Figure 4. Detail of timing implementation

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References

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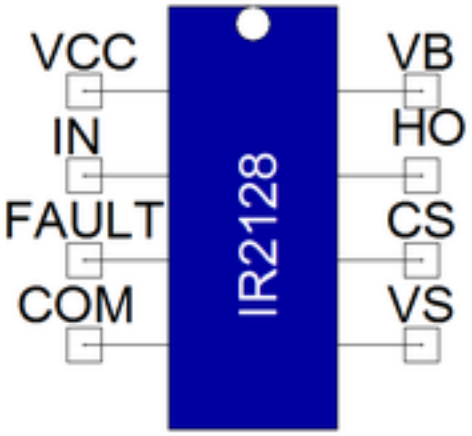
IR2128: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *IR2128* is a high voltage, high speed power MOSFET and IGBT driver. The protection circuit detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain FAULT signal is provided to indicate that an over-current shutdown has occurred.

The operation of this IC is controlled by three states machines. The upper one controls the under-voltage protection. When Vb falls below 9V, output switches open. The middle state machine controls the switching on steady state, simulating the switching delays. The bottom one controls the overcurrent protection and the fault switch.

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Table 1

Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IR2127 / IR21271) out of phase with HO (IR2128)
FAULT	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Product summary:

Table 2

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT} (IR2127 / IR2128) (IR21271)	12 - 20V 9 - 20V
V_{CSth}	250 mV or 1.8V
$t_{on/off}$ (typ.)	200 & 150 ns

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Parameters

Comparison between model and real component.

Apart from the parameters appeared in the product summary section, which the model matches with, there are some others parameters implemented as well:

Table 3

PARAMETER	DEFINITION	IR2128	MODEL	UNITS
Static Electrical Characteristics				
V_{IH}	Logic '1' input voltage	3.0 (min)	3.0	V
V_{IL}	Logic '0' input voltage	0.8 (max)	0.8	V
V_{CSTH+}	CS input positive going threshold	250	250	mV
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold	10.3	10.3	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold	9.0	9.0	V

Temperature influence parameters as well as bias and leakage currents have not been implemented. Input and output impedances are ideal, so the input impedance is infinite (Zin=∞) and the output impedance is zero (Zo=0).

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Examples

In this circuit the IC controls a low side MOSFET with resistive load. When MOSFET gate voltage is high, the circuit is closed and the output voltage is zero. Fault pin is connected to a pull-up resistor. Vcc is 20V.

Example circuit :

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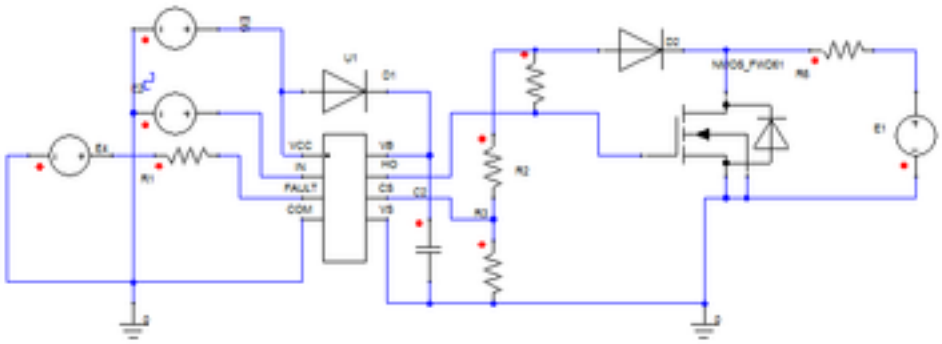
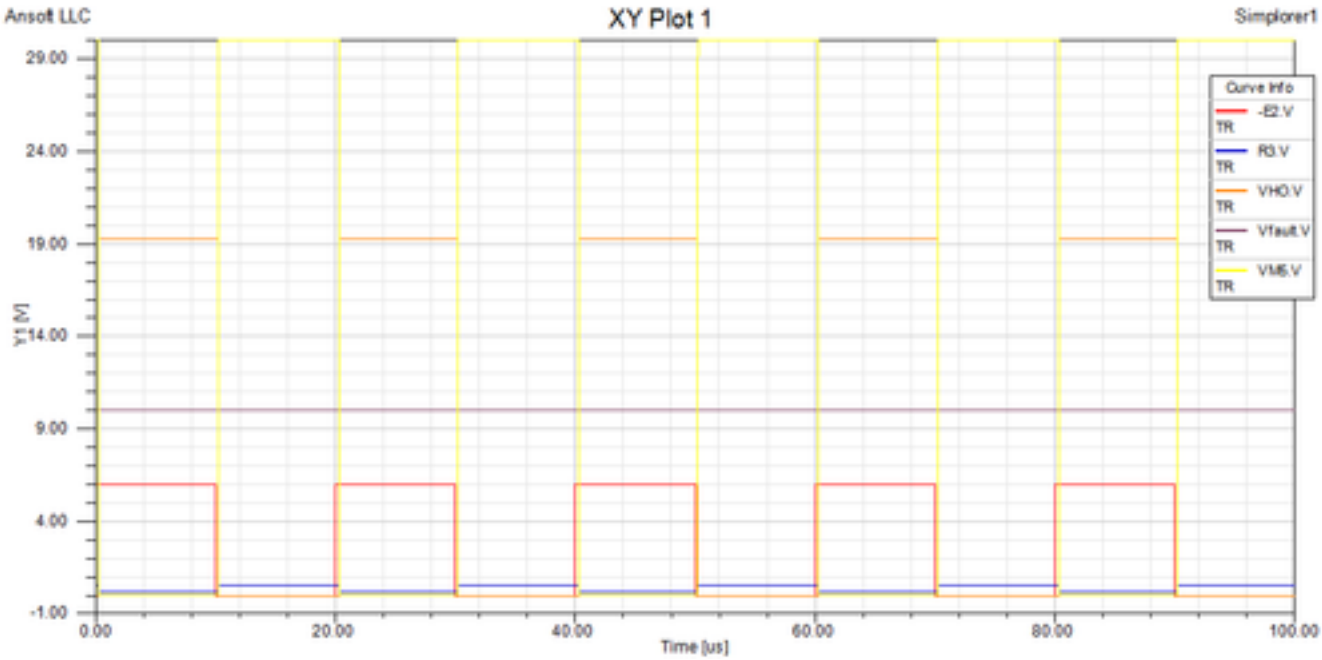


**Figure 2. Example Circuit **

Simulation results :

Steady state (no fault):



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Red: input voltage

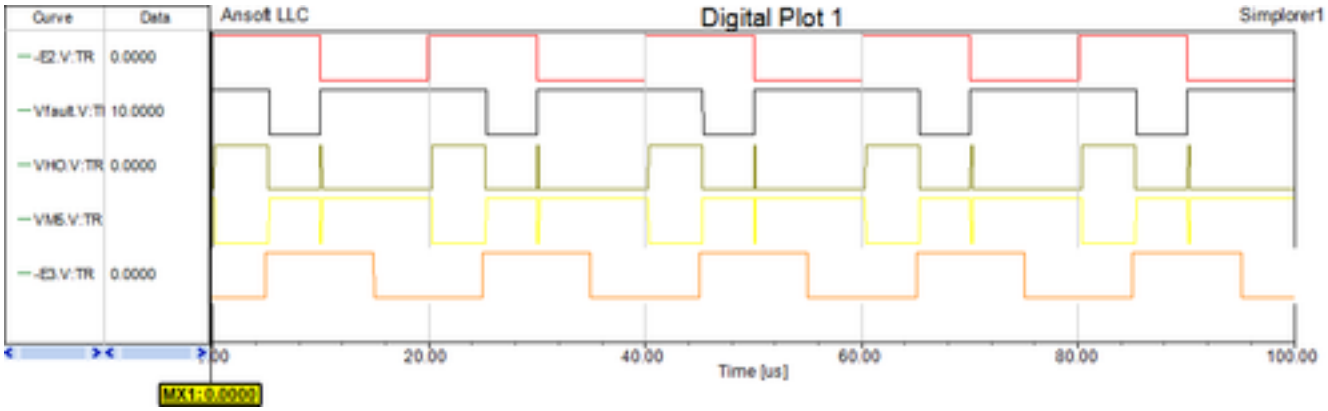
Blue: current sense voltage

Orange: MOSFET gate voltage (IC output)

Brown: fault voltage (negative logic)

Yellow: output voltage (to load)

Fault simulation:



Red: input voltage

Black: fault voltage (negative logic)

Green: MOSFET gate voltage (IC output)

Yellow: output voltage (to load)

Orange: current sense voltage

Figure 3. Simulation results

When CS voltage is higher than 0.25 V, open drain fault MOSFET is closed and the fault pin gets connected to ground through a pull-down resistor. When fault is detected, output voltage falls to low level.

IR2128 has negative logic, when input voltage is low, if there is no fault, output voltage is high.

Detail of timing implementation:

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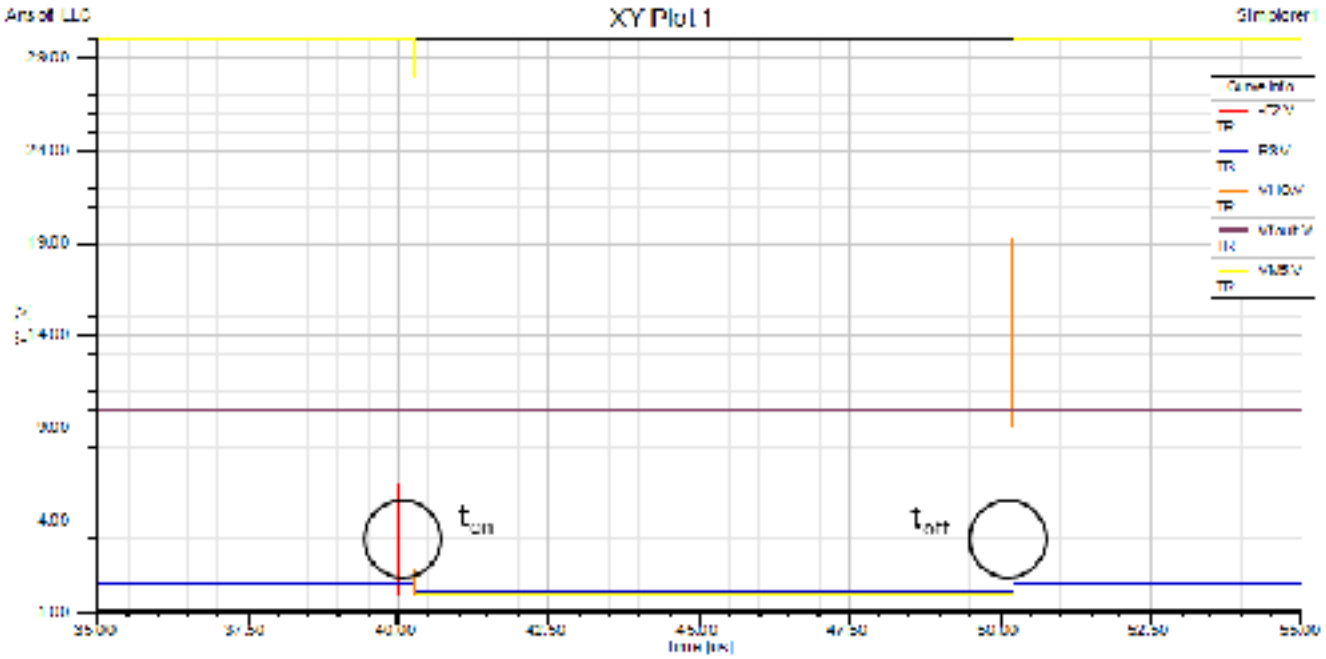

Red: input voltage

Blue: current sense voltage

Orange: MOSFET gate voltage (IC output)

Brown: fault voltage (negative logic)

Yellow: output voltage (to load)

Figure 4. Detail of timing implementation

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IR21271: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

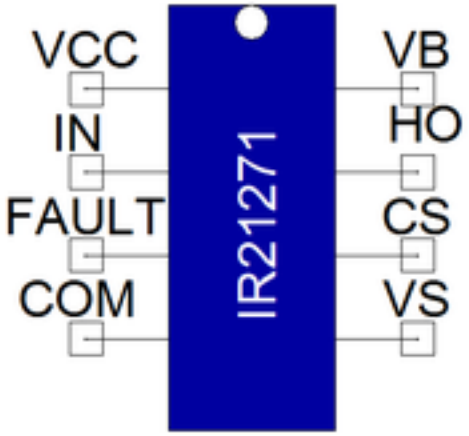

Figure 1. Component symbol

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• Input/Output Quantities

• Example

• References

Description

The *IR21271* is a high voltage, high speed power MOSFET and IGBT driver. The protection circuit detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain FAULT signal is provided to indicate that an over-current shutdown has occurred.

The operation of this IC is controlled by three states machines. The upper one controls the undervoltage protection. When Vb falls below 6.8V, output switches open. The middle state machine controls the switching on steady state, simulating the switching delays. The bottom one controls the overcurrent protection and the fault switch.

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Table 1

Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IR2127 / IR21271) out of phase with HO (IR2128)
FAULT	Indicates over-current shutdown has occurred, negative logic
COM	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
CS	Current sense input to current sense comparator

Product summary:

Table 2

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT} (IR2127 / IR2128) (IR21271)	12 - 20V 9 - 20V
V_{CSth}	250 mV or 1.8V
$t_{on/off}$ (typ.)	200 & 150 ns

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Parameters

Comparison between model and real component.

Apart from the parameters appeared in the product summary section, which the model matches with, there are some others parameters implemented as well:

Table 3

PARAMETER	DEFINITION	IR2110	MODEL	UNITS
Static Electrical Characteristics				
V_{IH}	Logic '1' input voltage	3.0 (min)	3.0	V
V_{IL}	Logic '0' input voltage	0.8 (max)	0.8	V
V_{CSTH+}	CS input positive going threshold	250	250	mV
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.2	7.2	V
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	6.8	6.8	V

Temperature influence parameters as well as bias and leakage currents have not been implemented. Input and output impedances are ideal, so the input impedance is infinite (Zin=∞) and the output impedance is zero (Zo=0).

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Examples

In this circuit the IC controls a low side MOSFET with resistive load. When MOSFET gate voltage is high, the circuit is closed and the output voltage is zero. Fault pin is connected to a pull-up resistor. Vcc is 20V.

Example circuit :

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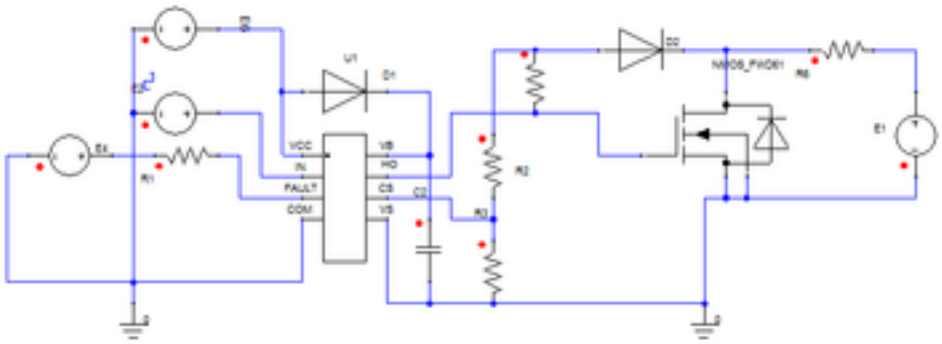
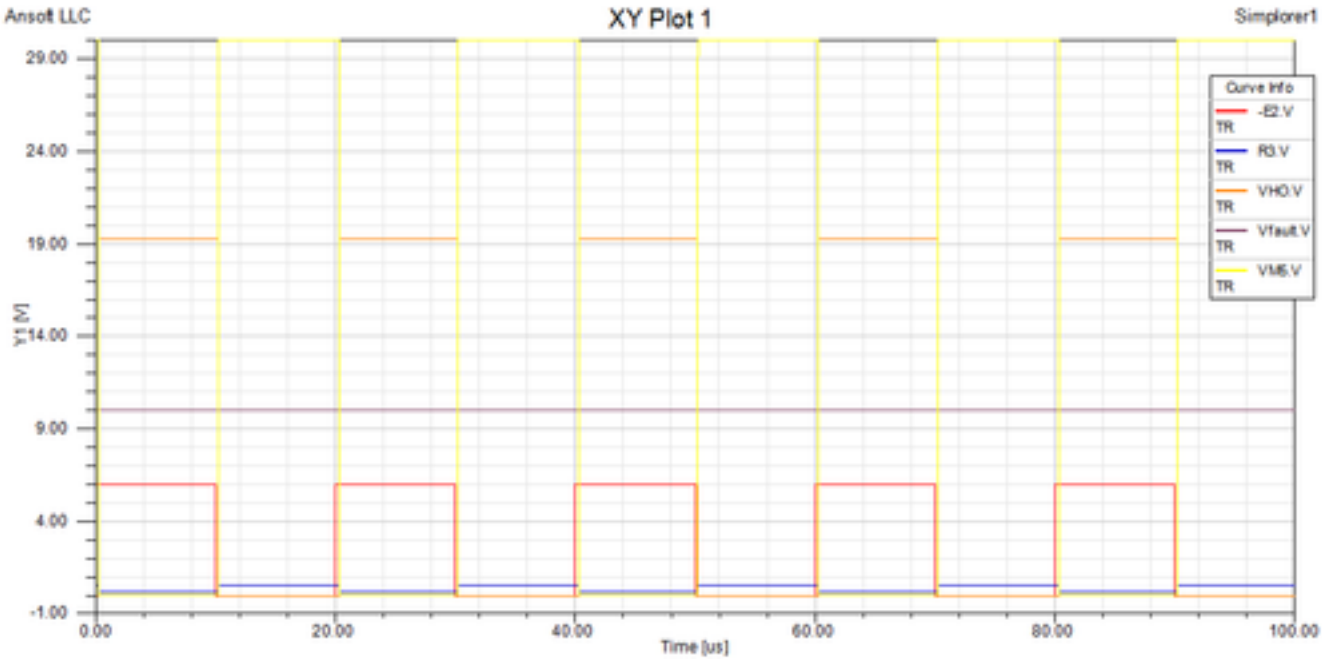


Figure 2. Example Circuit

Simulation results :

Steady state (no fault):



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Red: input voltage

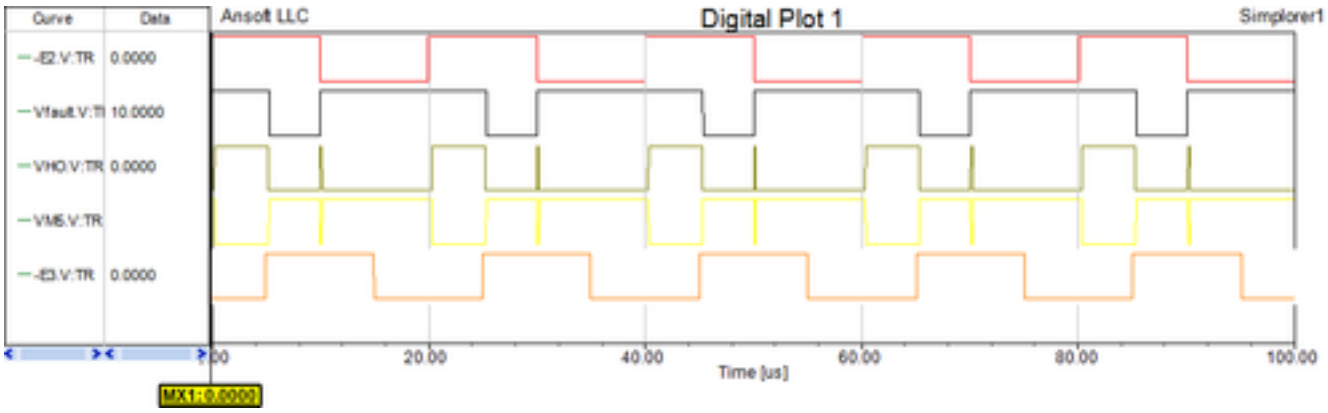
Blue: current sense voltage

Orange: MOSFET gate voltage (IC output)

Brown: fault voltage (negative logic)

Yellow: output voltage (to load)

Fault simulation:



Red: input voltage

Black: fault voltage (negative logic)

Green: MOSFET gate voltage (IC output)

Yellow: output voltage (to load)

Orange: current sense voltage

Figure 3. Simulation results

When CS voltage is higher than 1.8 V, open drain fault MOSFET is closed and the fault pin gets connected to ground through a pull-down resistor. When fault is detected, output voltage falls to low level.

Detail of timing implementation:

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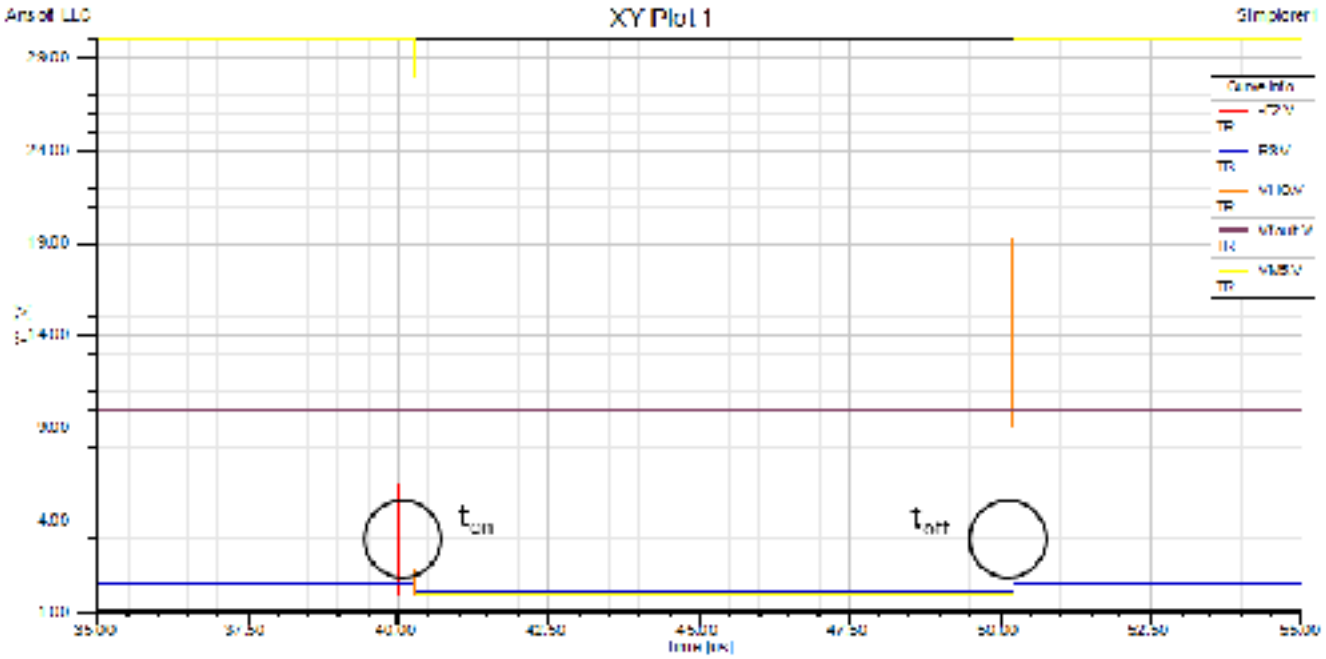

Red: input voltage

Blue: current sense voltage

Orange: MOSFET gate voltage (IC output)

Brown: fault voltage (negative logic)

Yellow: output voltage (to load)

Figure 4. Detail of timing implementation

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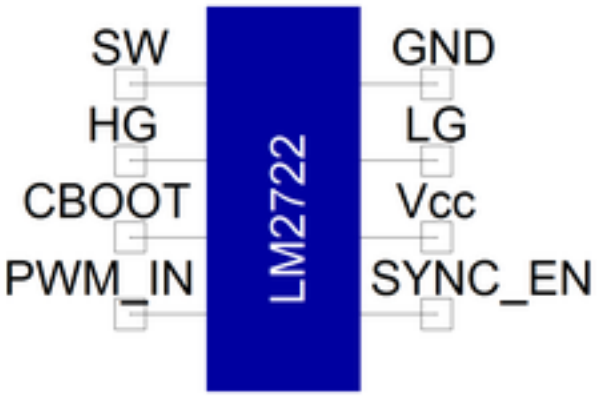
LM2722: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM2722*, part of the LM2726 family, is designed to be used with multi-phase controllers. This part differs from the LM2726 by changing the functionality of the SYNC_EN pin from a whole chip enable to a low side MOSFET enable. As a result, the SYNC_EN pin now provides control between Synchronous and Asynchronous operations. Having this control can be advantageous in portable systems since Asynchronous operations can be more efficient at very light loads.

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The *LM2722* drives both top and bottom MOSFETs in a push-pull structure simultaneously. It takes a logic level PWM input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in cross-conduction protection circuitry prevents the top and bottom FETs from turning on simultaneously. The cross-conduction protection circuitry detects both the driver outputs and will not turn on a driver until the other driver output is low. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the *LM2722* is typically 3A. In an SO-8 package, each driver is able to handle 50mA average current. Input UVLO (Under-Voltage-Lock-Out) forces both driver outputs low to ensure proper power-up and power-down operation. The gate drive bias voltage needed by the high side MOSFET is obtained through an external bootstrap. Minimum pulse width is as low as 55ns.

The model consist of state machines that controls the logic and delays of the switches of high and low sides, and the built-in shoot-through protection to ensure both Mosfets are not conducting at the same time.

Another set of state machines controls the Enable function to prevent spurious turn-on of the low-side MOSFET when the controller is inactive. And also there is a set of state machines that controls the under-voltage lockout of the controller.

Finally there are two additional sets of state machines that provides the controller with various inertial delays to prevent spurious pulses to turn the Mosfets.

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Conservative Pins

Table 1

Pin #	Pin Name	Pin Function
1	SW	Top driver return. Should be connected to the common node of top and bottomFETs
2	HG	Top gate drive output
3	CBOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver
4	PWM_IN	Accepts a 5V-logic control signal

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5	SYNC_EN	Low gateEnable
6	VCC	Connect to +5V supply.
7	LG	Bottom gate drive output
8	GND	Ground.

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Parameters

Comparison between model and real component.

Table 2

Symbol	Parameter	Conditions	Min	Type	Max	Model	Units
POWER SUPPLY							
Iq_op	Operating Quiescent Current	IN = 0V		190	300	x	µA
TOP DRIVER							
	Peak Pull-up Current			3		5.6	A
RH-pu	Pull-up Rds_on	IBOOT = IHG = 0.3A		1		1	Ohm
	Peak Pull-downCurrent			3.2		3.5	A
RH-pd	Pull-down Rds_on	ISW = IHG = 0.3A		0.5		0.5	Ohm
t4	Rise Time	Timing Diagram, CLOAD = 3.3nF		17		17	ns
t6	Fall Time			12		15	ns
t3	Pull-up Dead Time	Timing Diagram		23		23	ns
t5	Pull-down Delay	Timing Diagram		27		27	ns
BOTTOM DRIVER							

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	Peak Pull-up Current			3.2			A
RL-pu	Pull-up Rds_on	IVCC = ILG = 0.3A		1		1	Ohm
	Peak Pull-downCur-rent			3.2		3.5	A
RL-pd	Pull-down Rds_on	IGND = ILG = 0.3A		0.5		0.5	Ohm
t8	Rise Time	Timing Diagram, CLOAD = 3.3nF		17		17	ns
t2	Fall Time	Timing Diagram, CLOAD = 3.3nF		14		16	ns
t7	Pull-up Dead Time	Timing Diagram		28		28	ns
t1	Pull-down Delay	Timing Diagram		13		13	ns
LOGIC							
Vuvlo_up	VCC Under-Voltage Lock-Out Upper Threshol-d	VCC rises from 0V toward 5V	4	3.7		3.7	V
Vuvlo_dn	VCC Under-Voltage-Lock-Out Lower Threshol-d	VCC falls from 5V toward 0V		3	2.5	3	V
Vuvlo_hys	VCC Under-Voltage-Lock-Out Hys-teresis	VCC falls from 5V toward 0V		0.7		0.7	V
VIH_	SYNC	When	2.4			2.4	% of

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SYNC	Pin High Input	SYNC pin goes high from 0V					VCC
VIL_ SYNC	SYNC Pin Low Input	When SYNC pin goes low from 5V			0.8	0.8	
Ileak_ EN	SYNC_ EN Pin Leakage Current	EN = 5V	-2		2	0	uA
		EN = 0V	-2		2	0	
ton_ min	Minimum Positive Input Pulse Width			55		55	ns
Toff_ min	Minimum Negative Input Pulse Width			55		55	
VIH_ PWM	PWM_IN High Level Input Voltage	When PWM_IN pin goes high from 0V	2.4			2.4	V
VIL_ PWM	PWM_IN Low Level Input Voltage	When PWM_IN pin goes low from 5V			0.8	0.8	V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating ratings are conditions under which the device operates correctly. Operating Ratings do not imply guaranteed performance limits.

Note 2: Maximum allowable power dissipation is a function of the maximum junction temperature, TJMAX, the junction-to-ambient thermal resistance, qJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is calculated using: PMAX = (TJMAX-TA) / qJA. The junction-to-ambient thermal resistance, qJA, for the LM2722, it is 172°C/W. For a TJMAX of 150°C and TA of 25°C, the maximum allowable power dissipation is 0.7W.

Note 3: ESD machine model susceptibility is 100V.

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Note 4: If after a rising edge, a falling edge occurs sooner than the specified value, the IC may intermittently fail to turn on the bottom gate when the top gate is off. As the falling edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

Note 5: If after a falling edge, a rising edge occurs sooner than the specified value, the IC may intermittently fail to turn on the top gate when the bottom gate is off. As the rising edge occurs sooner and sooner, the driver may start to ignore the pulse and produce no output.

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Example circuit :

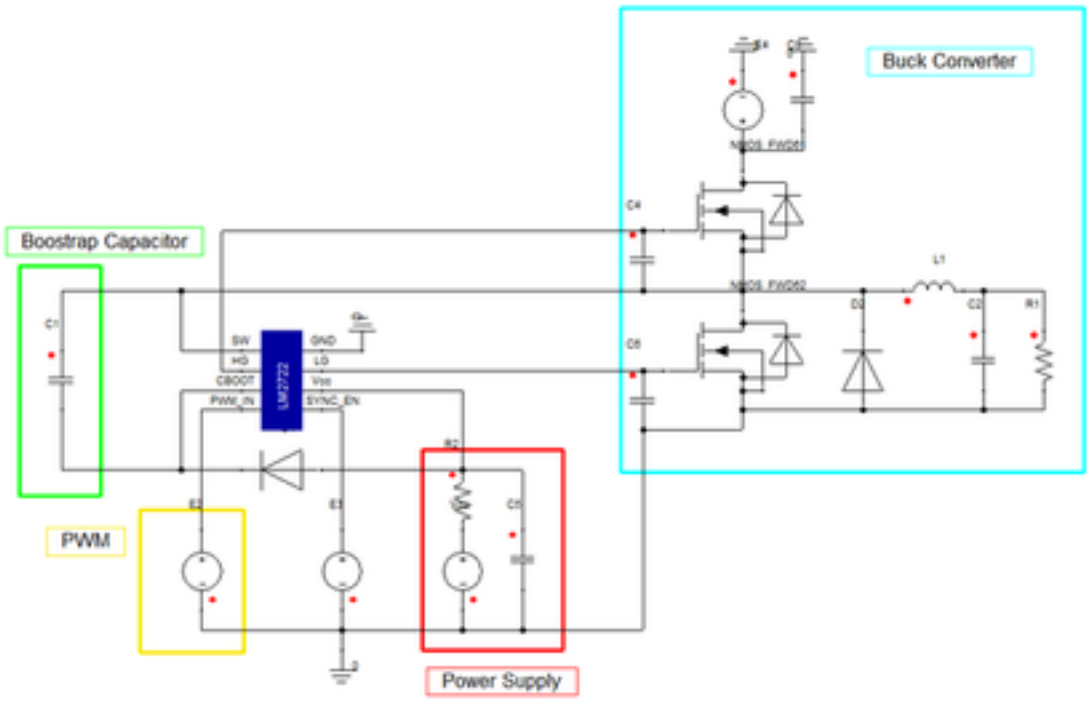

Figure 2. Example Circuit

Simulation results :

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Figure 3. Simulation results

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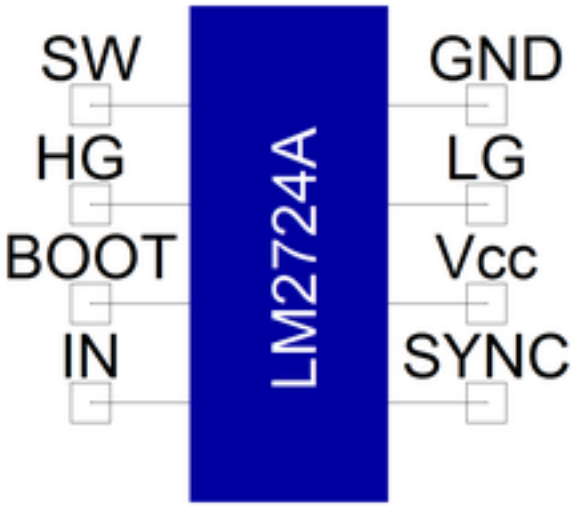
LM2724A: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM2724A* is a dual N-channel MOSFET driver which can drive both the top and bottom MOSFETs in a push-pull structure simultaneously. The LM2724A takes a logic input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in cross-conduction protection circuitry prevents the top and bottom MOSFETs from turning on simultaneously. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the *LM2724A* is about 3A. Input UVLO (Under-Voltage-Lock- Out) ensures that all the driver outputs stay low until the supply rail exceeds the power-on threshold during system power on, or

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after the supply rail drops below power-on threshold by a specified hysteresis during system power down.

The cross-conduction protection circuitry detects both driver outputs and will not turn on a driver until the other driver output is low. The top gate voltage needed by the top MOSFET is obtained through an external boot-strap structure. When not switching, the *LM2724A* only draws up to 195µA from the 5V rail. The synchronization operation of the bottom MOSFET can be disabled by pulling the SYNC pin to ground.

The model consist of state machines that controls the logic and delays of the switches of high and low sides, and the built-in shoot-through protection to ensure both Mosfets are not conducting at the same time.

Another set of state machines controls the Enable function to prevent spurious turn-on of the low-side MOSFET when the controller is inactive. And also there is a set of state machines that controls the under-voltage lockout of the controller.

Finally there are two additional sets of state machines that provides the controller with various inertial delays to prevent spurious pulses to turn the Mosfets

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Table 1

Pin #	Pin Name	Pin Function
1	SW	Top driver return. Should be connected to the common node of top and bottom FETs
2	HG	Top gate drive output. Should be connected to the top FET gate.
3	BOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver.
4	IN	Accepts a logic control signal
5	SYNC	Bottom gateenable
6	VCC	Connect to +5V supply.
7	LG	Bottom gate drive output. Should be connected to the bottom FET

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		gate.
8	GND	Ground.

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Parameters

Comparison between model and real component.

Table 2

Sym-bol	Para-meter	Condi-tions	Min	Typ	Max	Mode-l	Unit-s
POWER SUPPLY							
Iq_op	Oper-ating Qui-escent Current	IN = 0V		145	195	x	µA
TOP DRIVER							
	Peak Pull-up Current			3		6.25	A
RH-pu	Pull-up Rds_on	IBOOT = IHG = 0.3A		1.2		1.2	Ohm
	Peak Pull-downCur-rent			3.2		3.25	A
RH-pd	Pull-down Rds_on	ISW = IHG = 0.3A		0.5		0.2	Ohm
t4	Rise Time	Timing Diagram, CLOAD = 3.3nF		17		17	ns
t6	Fall Time			12		12	ns
t3	Pull-up Dead Time	Timing Diagram		19		19	ns
t5	Pull-down Delay	Timing Diagram		27		5.5	ns
BOTTOM DRIVER							
	Peak Pull-up Current			3.2		5.5	A
RL-pu	Pull-up Rds_on	IVCC = ILG =		1.1		1.1	Ohm

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		0.3A					
	Peak Pull-downCur-rent			3.2		3.5	A
RL-pd	Pull-down Rds_on	IGND = ILG = 0.3A		0.6		0.6	Ohm
t8	Rise Time	Timing Diagram, CLOAD = 3.3nF		17		17	ns
t2	Fall Time	Timing Diagram, CLOAD = 3.3nF		14		14	ns
t7	Pull-up Dead Time	Timing Diagram		22		23	ns
t1	Pull-down Delay	Timing Diagram		13		10	ns
LOGIC							
Vuvlo_up	VCC Under-Voltage Lock-Out Upper Threshol-d	VCC risesfrom 0V toward 5V			4	4	V
Vuvlo_dn	VCC Under-Voltage-Lock-Out Lower Threshol-d	VCC falls from 5V toward 0V	2.5			2.5	V
Vuvlo_hys	VCC Under-Voltage-Lock-Out Hys-teresis	VCC falls from 5V toward 0V		0.8		0.8	V
VIH_SYNC	SYNC Pin High Input	When SYNC pin goes high from 0V	55%			55%	% of VCC
VIL_	SYNC	When			25%	25%	

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SYNC	Pin Low Input	SYNC pin goes low from 5V					
Ileak_ SYNC	SYNC Pin Leakage Current	SYNC = 5V, SinkCurrent			2	0	uA
		SYNC = 0V, Source Current			10	0	
Ileak_ IN	IN Pin Leakage Current	IN = 0V, Source Current			2	0	
		IN = 5V, SinkCurrent			10	0	
ton_ min1	Minimum Positive Pulse Width at IN Pin			160		160	ns
ton_ min2	Minimum Positive pulse Width at IN Pin for HG to respond			45		45	
ton_ min3	Minimum Positive pulse width at IN Pin for LG to respond			10		10	
toff_ min1	Minimum Negative Pulse Width at IN Pin for LG to Respond			40		40	
toff_ min2	Minimum Negative Pulse Width at IN Pin for HG to Respond			5		5	

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VIH_IN	IN High Level Input Voltage	When IN pin goes high from 0V	55%			55%	% of VCC
VIL_IN	IN Low Level Input Voltage	When IN pin goes low from 5V			25%	25%	

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating ratings are conditions under which the device operates correctly. The gaurnteed specifications apply only for the listed test conditions. Some performance characteristics may degrade when the part is not operated under listed conditions.

Note 2: If BOOT voltage exceeds this value, the ESD structure will degrade.

Note 3: Maximum allowable power dissipation is a function of the maximum junction temperature, TJMAX, the junction-to-ambient thermal resistance, θJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is calculated using: PMAX = (TJMAX-TA) / θJA. The junction-toambient thermal resistance, θJA, for LM2724A is 172°C/W. For a TJMAX of 150°C and TA of 25°C, the maximum allowable power dissipation is 0.7W. The θJA, for LM2724A LLP package is 39°C/W. For a TJMAX of 150°C and TA of 25°C, the maximum allowable power dissipation is 3.2W.

Note 4: ESD machine model susceptibility is 200V.

Note 5: If the positive pulse width at IN pin is below this value but above ton_min2, the pulse is internally stretched to ton_min1, so the HG width will be a constant value.

Note 6: If the positive pulse width at IN pin is below this value but above ton_min3, then HG stops responding while LG still responds to the pulse.

Note 7: If the positive pulse width at IN pin is below this value, the pulse will be completely ignored. Neither HG or LG will respond to it.

Note 8: If the negative pulse width at IN pin is below this value but above toff_min2, then LG stops responding while HG still responds.

Note 9: If the negative pulse width at IN pin is below this value, the pulse will be completely ignored. Neither HG or LG willrespondtoit.

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Example circuit :

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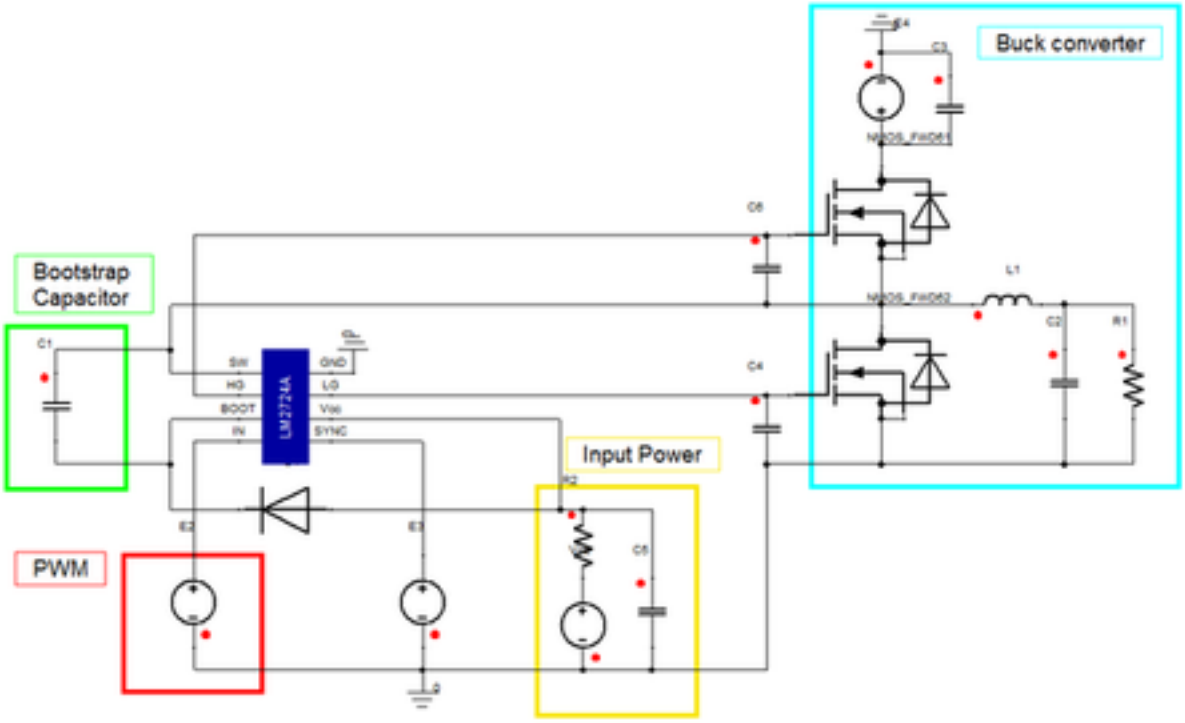

Figure 2. Example Circuit

Simulation results :

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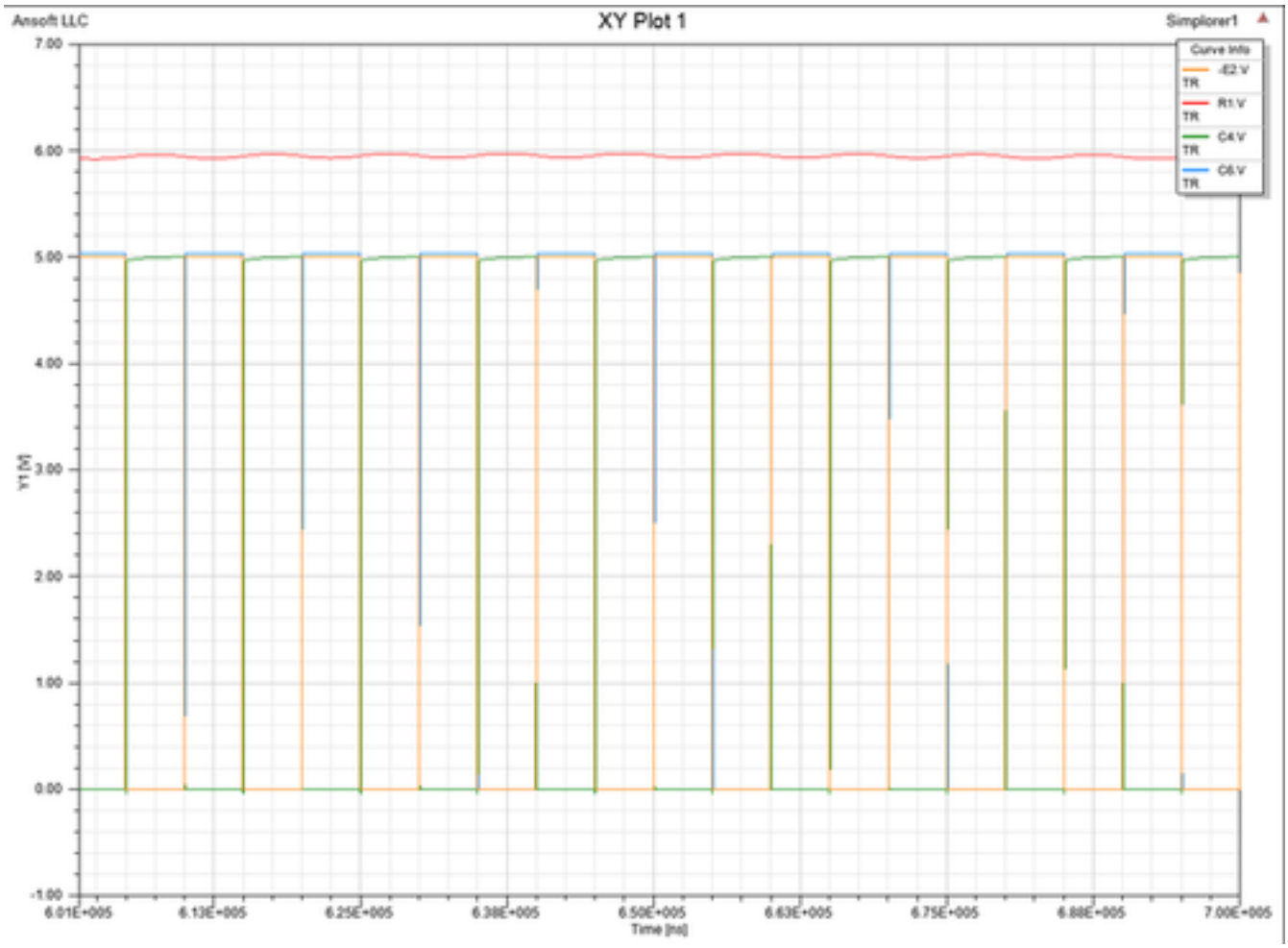

Figure 3. Simulation results

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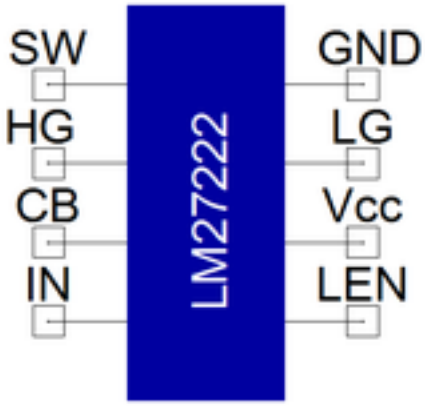
LM27222: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM27222* is a dual N-channel MOSFET driver designed to drive MOSFETs in push-pull configurations as typically used in synchronous buck regulators. The *LM27222* takes the PWM output from a controller and provides the proper timing and drive levels to the power stage MOSFETs.

Adaptive shoot-through protection prevents damaging and efficiency reducing shoot-through currents, thus ensuring a robust design capable of using nearly any MOSFET. The adaptive shoot-through protection circuitry also reduces the dead time down to as low as 10ns ensuring the

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highest operating efficiency. The peak sourcing and sinking current for each driver of the *LM27222* is about 3A and 4.5Amps respectively with a Vgs of 5V.

System performance is also enhanced by keeping propagation delay down to 8ns. Efficiency is once again improved at all load currents by supporting synchronous, non-synchronous, and diode emulation modes through the LEN pin. The minimum output pulse width realized at the output of the MOSFETs is as low as 30ns. This enables high operating frequencies at very high conversion ratios in buck regulator designs.

The *LM27222* simplifies sequencing requirements by keeping gate drives low until Vin and Vcc are stable and the switching controller starts operating. To support low power states in notebook systems, *LM27222* draws only 5µA from the 5V rail when the IN and LEN inputs are low or floating.

The model consist of state machines that controls the logic and delays of the switches of high and low sides, and the built-in shoot-through protection to ensure both Mosfet are not conducting at the same time.

The other set of state machines controls the Enable function to prevent spurious turn-on of the low-side MOSFET when the controller is inactive.

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Conservative Pins

Table 1

Pin #	Pin Name	Pin Function
1	SW	High-side driver return. Should be connected to the common node of high and low-side MOSFETs.
2	HG	High-side gate drive output. Should be connected to the high-side MOSFET gate. Pulled down internally to SW with a 10K resistor to prevent spurious turn on of the high-side MOSFET when the driver is off.
3	CB	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver.
4	IN	Accepts a logic control signal from a controller. Pulled down internally to GND with a 150K resistor

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		to prevent spurious turn on of the high-side MOSFET when the controller is inactive.
5	LEN	Low-side gate enable. Pulled down internally to GND with a 150K resistor to prevent spurious turn-on of the low-side MOSFET when the controller is inactive.
6	VCC	Connect to +5V supply.
7	LG	Low-side gate drive output. Should be connected to low-side MOSFET gate. Pulled down internally to GND with a 10K resistor to prevent spurious turn on of the low-side MOSFET when the driver is off.
8	GND	Ground.

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Comparison between model and real component.

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Table 2

Sym-bol	Para-meter	Condi-tions	Min	Typ	Max	Mode-l	Unit-s
POWER SUPPLY							
Iq_op	Oper-ating Qui-escent Current	IN = 0V, LEN = 0V		5	15	x	µA
					30	x	
		IN = 0V, LEN = 5V	500	540	650	x	µA
					825	x	
HIGH-SIDE DRIVER							
	Peak Pull-up Current			3		3.6	A
RH-pu	Pull-up Rds_on	ICB = IHG = 0.3A		0.9	2.5	1	Ohm
	Peak Pull-downCur-rent			4.5		4	A
RH-pd	Pull-down Rds_on	ISW = IHG = 0.3A		0.4	1.5	0.9	Ohm
t4	Rise Time	Timing Diagram, CLOAD = 3.3nF		17		17	ns
t6	Fall Time	Timing Diagram, CLOAD = 3.3nF		12		6.3	ns
t3	Pull-up Dead Time	Timing Diagram		9.5		10	ns
t5	Pull-down Delay	Timing Diagram		16.5		16.5	ns
ton_ min	Minimum Positive Output Pulse Width			30		X	ns
LOW-SIDE DRIVER							
	Peak Pull-up Current			3.2		4	A

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RL-pu	Pull-up Rds_on	IVCC = ILG = 0.3A		0.9	2.5	1	Ohm
	Peak Pull-downCur-rent			4.5		4.25	A
RL-pd	Pull-down Rds_on	IGND = ILG = 0.3A		0.4	1.5	0.9	Ohm
t8	Rise Time	Timing Diagram, CLOAD = 3.3nF		17		17	ns
t2	Fall Time	Timing Diagram, CLOAD = 3.3nF		14		7.8	ns
t7	Pull-up Dead Time	Timing Diagram		11.5		12.3	ns
t1	Pull-down Delay	Timing Diagram		7.7		7.7	ns
PULL-DOWN RESISTANCES							
	HG-SW Pull-down Resist-ance			10k		10k	Ohm
	LG-GND Pull-down Resist-ance			10k		10k	Ohm
	LEN-GND Pull-down Resist-ance			150k		150k	Ohm
	IN-GND Pull-down Resist-ance			150k		150k	Ohm

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LEAKAGE CURRENTS							
Ileak_ IN	IN pin Leakage Current	IN = 0V, Source Current		50		0	nA
		IN = 5V, SinkCur-rent		33		0	µA
Ileak_ LEN	LEN pin Leakage Current	LEN = 0V, Source Current		200		0	nA
		LEN = 5V, SinkCur-rent		33		0	µA

Table 3

LOGIC							
Sym-bol	**Para-meter**	**Condi-tions**	**Min**	**Typ**	**Max**	**Mode-l**	**Unit-s**
VIH_ LEN	LEN Pin High Input	When LEN pin goes high from 0V			65	65	% of VCC
VIL_ LEN	LEN Pin Low Input	When LEN pin goes low from 5V	30			30	% of VCC
VIH_IN	IN High Level Input Voltage	When IN pin goes high from 0V			65	65	% of VCC
VIL_IN	IN Low Level Input Voltage	When IN pin goes low from 5V	30			30	% of VCC

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. Operating Ratings do not imply guaranteed performance limits.

Note 2: The SW pin can have -2V to -0.5 volts applied for a maximum duty cycle of 10% with a maximum period of 1 second. There is no duty cycle or maximum period limitation for a SW pin voltage range of -0.5V to 30 Volts.

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Note 3: Maximum allowable power dissipation is a function of the maximum junction temperature, TJMAX, the junction-to-ambient thermal resistance, θJA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is calculated using: PMAX = (TJMAX-TA) / θJA. The junction-to ambient thermal resistance, θJA, for the LM2722, it is 172°C/W. For a TJMAX of 150°C and TA of 25°C, the maximum allowable power dissipation is 0.7W. The θJA for the LM2724 LLP-8 package is 39°C/W. For a TJMAX of 150°C and TA of 25°C, the maximum allowable power dissipation is 3.2W.

Note 4: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical

Quality Control (SQC) methods. Limits are used to calculate National™s Average Outgoing Quality Level (AOQL).

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Example circuit :

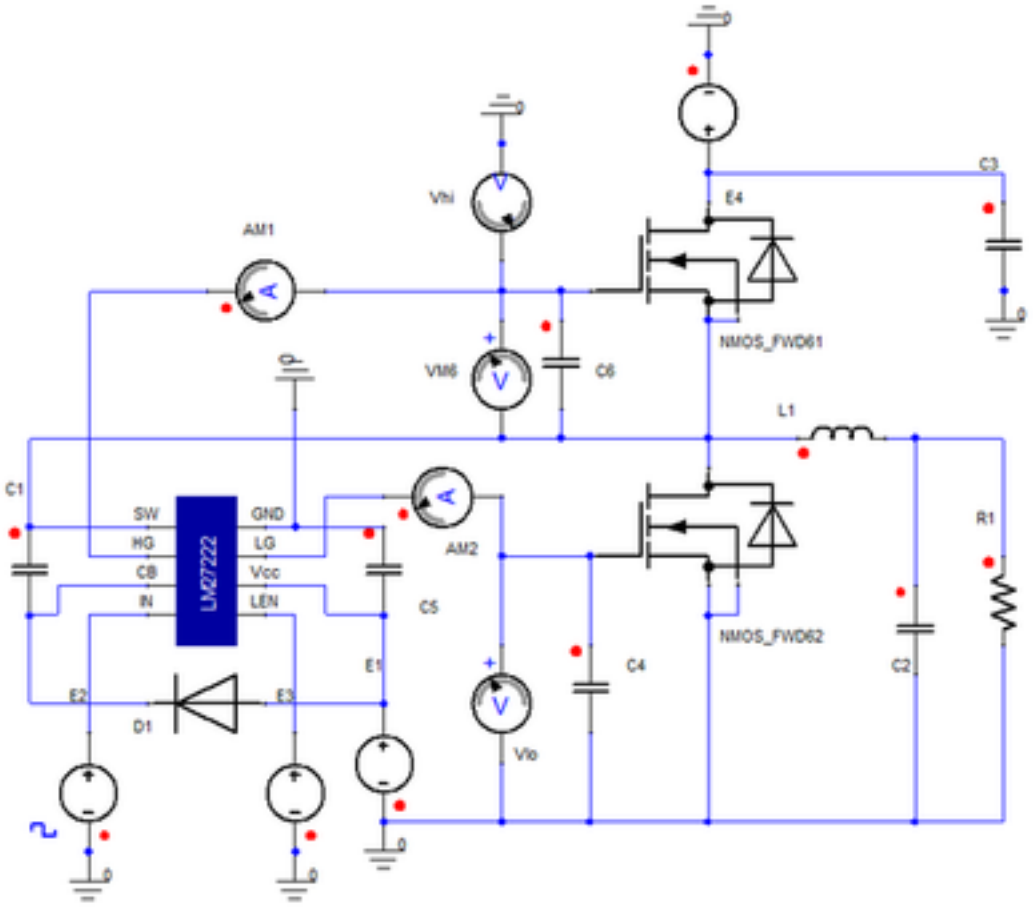

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Figure 2. Example Circuit

Simulation results :

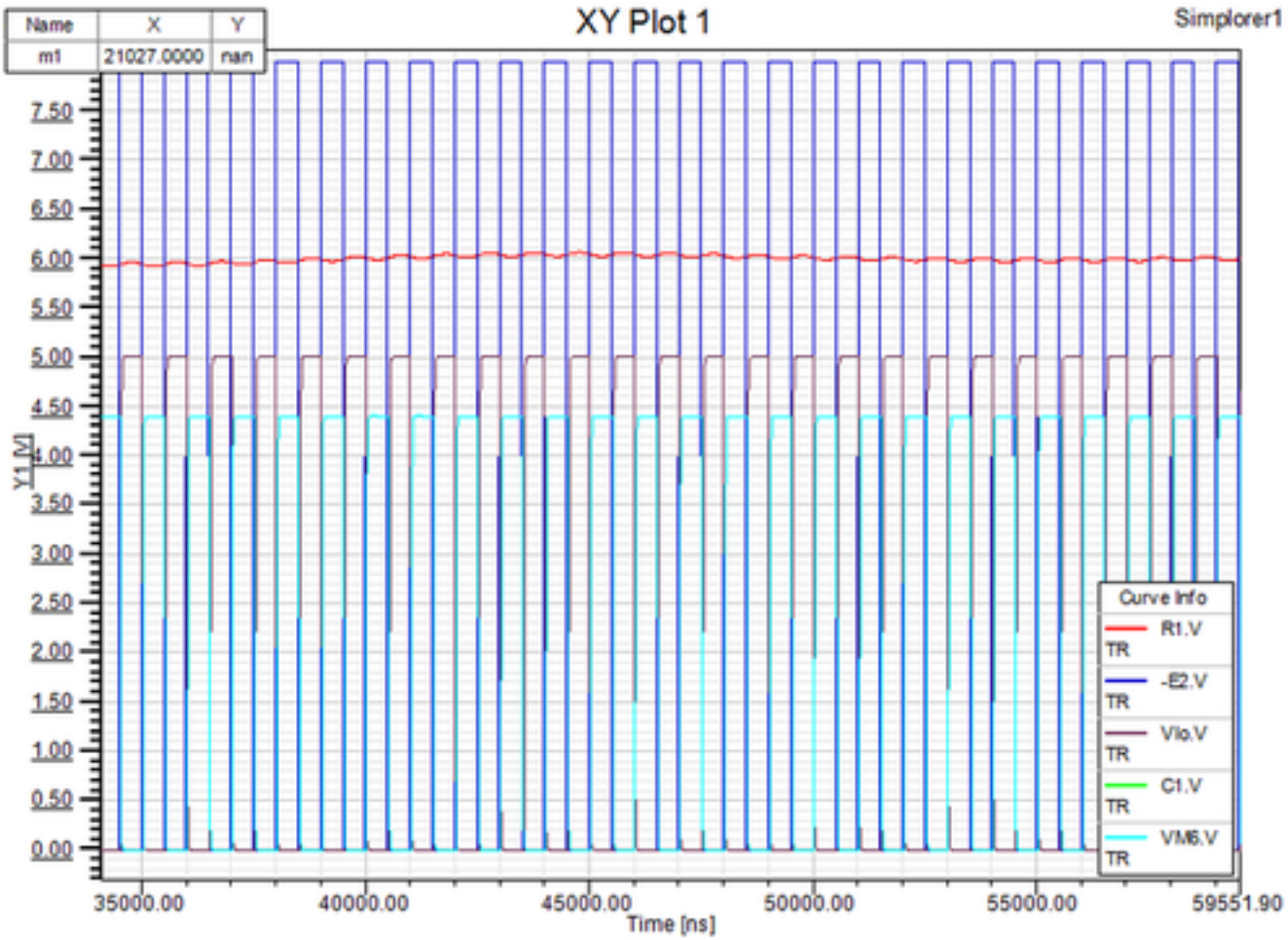

Figure 3. Simulation results

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References

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LM5100A: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

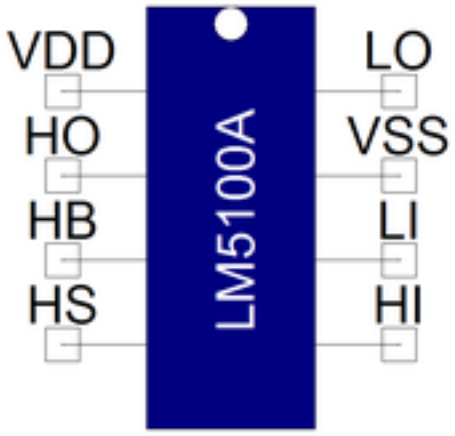

Figure 1. Component symbol

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Description

The *LM5100A/B/C* and *LM5101A/B/C* High Voltage Gate Drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The "A" versions provide a full 3A of gate drive while the "B" and "C" versions provide 2A and 1A respectively. The outputs are independently controlled with CMOS input thresholds (*LM5100A/B/C*) or TTL input thresholds (*LM5101A/B/C*). An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control

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logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin, PSOP-8 pin and the LLP-10 pin packages. The *LM5100C* and *LM5101C* are also available in eMSOP-8 package. The *LM5101A* is also available in LLP-8 pin package.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

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Table 2

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
Supply Currents						
VDD Qui-escent Cur-rent, LM5100A/B/-C	LI = HI = 0V		0.1	0.2	0.1	mA
VDD Qui-escent Cur-rent, LM5101A/B/-C	LI = HI = 0V		0.25	0.4	0.25	mA
VDD Oper-ating Current	f = 500 kHz		2.0	3	-	mA
Total HB Qui-escent Cur-rent	LI = HI = 0V		0.06	0.2	-	mA
Total HB Operating Current	f = 500 kHz		1.6	3	-	mA
HB to VSS Current, Qui-escent	HS = HB = 100V		0.1	10	-	uA
HB to VSS Current, Operating	f = 500 kHz		0.4		-	mA
Input Pins						
Input Voltage Threshold LM5100A/B/-C	Rising Edge	4.5	5.4	6.3	5.4	V
Input Voltage Threshold LM5101A/B/-C	Rising Edge	1.3	1.8	2.3	1.8	V
Input Voltage Hysteresis LM5100A/B/-C			500		500	mV
Input Voltage Hysteresis LM5101A/B/-C			50		50	mV
Input Pull-down Resist-		100	200	400	200	kohm

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Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current Forward Voltage	IVDD-HB = 100 µA		0.52	0.85	0.52	V
High-Current Forward Voltage	IVDD-HB = 100 mA		0.8	1	0.8	V
Dynamic Resistance LM5100A/B/-C, LM5101A/B/-C	IVDD-HB = 100 mA		1.0	1.65	-	ohm

Table 3

PARAMETERS	TEST CONDITIO-NS	MIN	TYP	MA-X	MODE-L	UNIT-S
LO &HO Gate Driver						
Low-Level Out-put Voltage LM5100A/LM51-01A	IHO = ILO = 100 mA		0.12	0.25	0.12	V
Low-Level Out-put Voltage LM5100B/LM51-01B			0.16	0.4	0.16	V
Low-Level Out-put Voltage LM5100C/LM5-101C			0.28	0.65	0.28	V
High-Level Out-	IHO = ILO		0.24	0.45	0.24	V

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	= 100 mA					
High-Level Output Voltage LM5100B/LM5101B	VOH = VDD - LO or		0.28	0.60	0.28	V
High-Level Output Voltage LM5100C/LM5101C	VOH = HB - HO		0.60	1.10	0.60	V
Peak Pullup Current LM5100A/LM5101A	HO, LO = 0V		3		3	A
Peak Pullup Current LM5100B/LM5101B			2		2	A
Peak Pullup Current LM5100C/LM5101C			1		1	A
Peak Pulldown Current LM5100A/LM5101A	HO, LO = 12V		3		3	A
Peak Pulldown Current LM5100B/LM5101B			2		2	A
Peak Pulldown Current LM5100C/LM5101C			1		1	A

Table 4

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Switching Characteristics						
LO Turn-Off Propagation Delay LM5100A/B/C	LI Falling to LO Falling		20	45	20	ns
LO Turn-Off Propagation Delay			22	56	22	ns

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LM5101A/B/C						
LO Turn-On Propagation Delay LM5100A/B/C	LI Rising to LO Rising		20	45	20	ns
LO Turn-On Propagation Delay LM5101A/B/C			26	56	26	ns
HO Turn-Off Propagation Delay LM5100A/B/C	HI Falling to HO Falling		20	45	20	ns
HO Turn-Off Propagation Delay LM5101A/B/C			22	56	22	ns
LO Turn-On Propagation Delay LM5100A/B/C	HI Rising to HO Rising		20	45	20	ns
LO Turn-On Propagation Delay LM5101A/B/C			26	56	26	ns
Delay Matching: LO on & HO off LM5100A/B/C			1		0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Delay Matching: LO off & HO on LM5100A/B/C			1	10	0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Either Output Rise/Fall Time	CL = 1000 pF		8		3	ns
Output Rise Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		430		242	ns
Output Rise Time (3V to 9V) LM5100B/LM51-01B			570		282	ns
Output Rise Time(3V to 9V)			990		606	ns

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LM5100C/LM5-101C						
Output Fall Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		260		121	ns
Output Fall Time (3V to 9V) LM5100B/LM51-01B			430		161	ns
Output Fall Time (3V to 9V) LM5100C/LM5-101C			715		282	ns

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Example circuit :

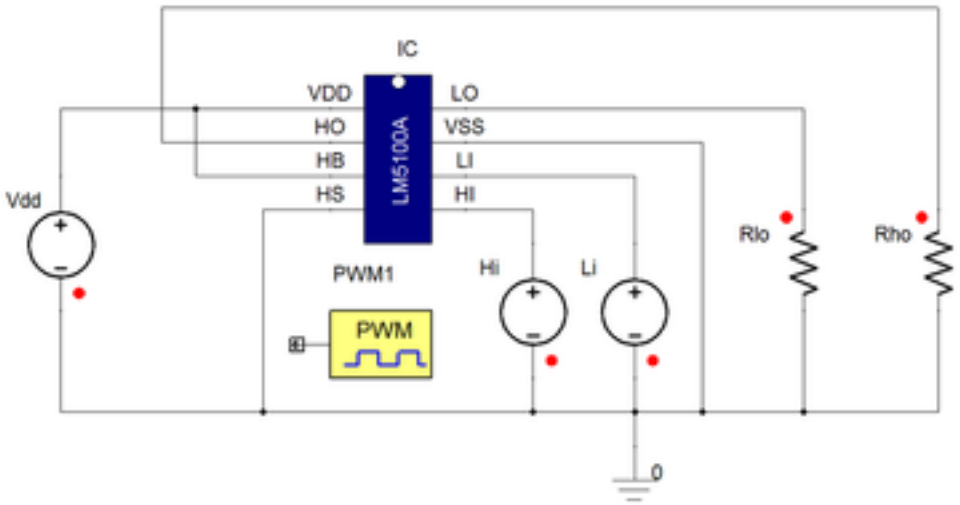

Figure 2. Example Circuit

Simulation results :

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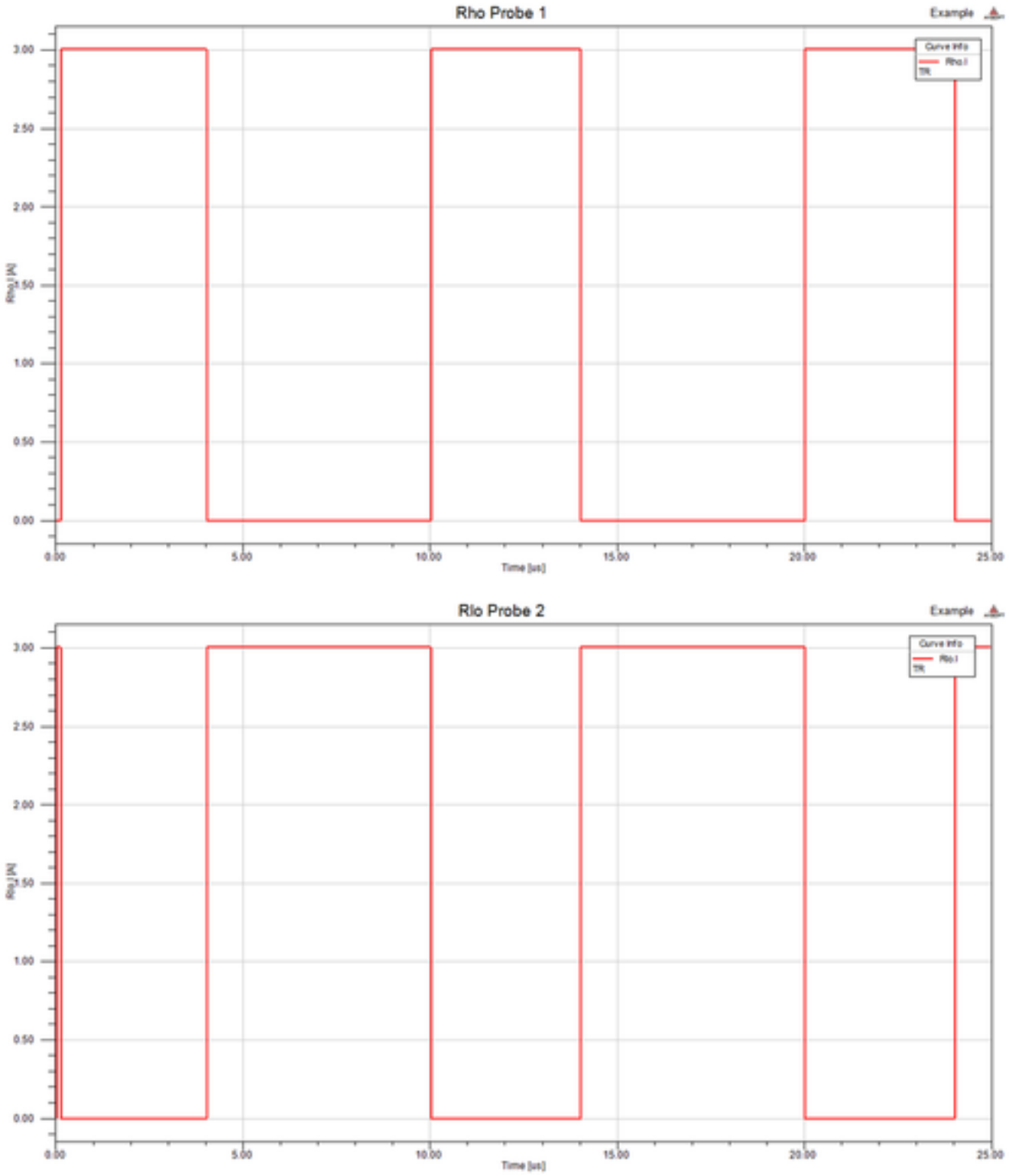

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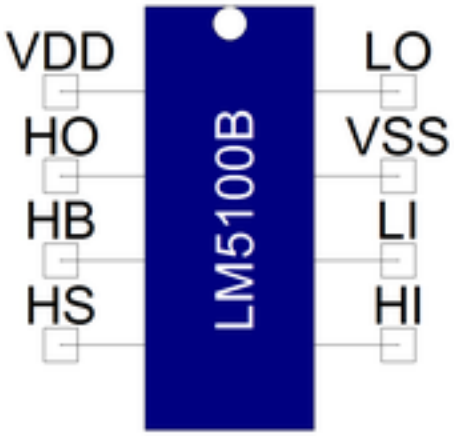
Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM5100A/B/C* and *LM5101A/B/C* High Voltage Gate Drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The "A" versions provide a full 3A of gate drive while the "B" and "C" versions provide 2A and 1A respectively. The outputs are independently controlled with CMOS input thresholds (*LM5100A/B/C*) or TTL input thresholds (*LM5101A/B/C*). An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control

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logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin, PSOP-8 pin and the LLP-10 pin packages. The *LM5100C* and *LM5101C* are also available in eMSOP-8 package. The LM5101A is also available in LLP-8 pin package.

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Table 1

PIN	NAME	FUNCTION
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2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

Table 2

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
Supply Currents						
VDD Qui-escent Cur-	LI = HI = 0V		0.1	0.2	0.1	mA

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rent, LM5100A/B/-C						
VDD Quiescent Current, LM5101A/B/-C	LI = HI = 0V		0.25	0.4	0.25	mA
VDD Operating Current	f = 500 kHz		2.0	3	-	mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2	-	mA
Total HB Operating Current	f = 500 kHz		1.6	3	-	mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.1	10	-	uA
HB to VSS Current, Operating	f = 500 kHz		0.4		-	mA
Input Pins						
Input Voltage Threshold LM5100A/B/-C	Rising Edge	4.5	5.4	6.3	5.4	V
Input Voltage Threshold LM5101A/B/-C	Rising Edge	1.3	1.8	2.3	1.8	V
Input Voltage Hysteresis LM5100A/B/-C			500		500	mV
Input Voltage Hysteresis LM5101A/B/-C			50		50	mV
Input Pull-down Resistance		100	200	400	200	kohm
Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V

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HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current Forward Voltage	IVDD-HB = 100 µA		0.52	0.85	0.52	V
High-Current Forward Voltage	IVDD-HB = 100 mA		0.8	1	0.8	V
Dynamic Resistance LM5100A/B/-C, LM5101A/B/-C	IVDD-HB = 100 mA		1.0	1.65	-	ohm

Table 3

PARAMETERS	TEST CONDITIO-NS	MIN	TYP	MA-X	MODE-L	UNIT-S
LO &HO Gate Driver						
Low-Level Out-put Voltage LM5100A/LM51-01A	IHO = ILO = 100 mA		0.12	0.25	0.12	V
Low-Level Out-put Voltage LM5100B/LM51-01B			0.16	0.4	0.16	V
Low-Level Out-put Voltage LM5100C/LM5-101C			0.28	0.65	0.28	V
High-Level Out-put Voltage LM5100A/LM51-01A	IHO = ILO = 100 mA VOH = VDD - LO or VOH = HB - HO		0.24	0.45	0.24	V
High-Level Out-put Voltage LM5100B/LM51-01B			0.28	0.60	0.28	V
High-Level Out-put Voltage			0.60	1.10	0.60	V

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Peak Pullup Current LM5100A/LM5101A	HO, LO = 0V		3		3	A
Peak Pullup Current LM5100B/LM5101B			2		2	A
Peak Pullup Current LM5100C/LM5101C			1		1	A
Peak Pulldown Current LM5100A/LM5101A	HO, LO = 12V		3		3	A
Peak Pulldown Current LM5100B/LM5101B			2		2	A
Peak Pulldown Current LM5100C/LM5101C			1		1	A

Table 4

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Switching Characteristics						
LO Turn-Off Propagation Delay LM5100A/B/C	LI Falling to LO Falling		20	45	20	ns
LO Turn-Off Propagation Delay LM5101A/B/C			22	56	22	ns
LO Turn-On Propagation Delay LM5100A/B/C	LI Rising to LO Rising		20	45	20	ns
LO Turn-On Propagation Delay			26	56	26	ns

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LM5101A/B/C						
HO Turn-Off Propagation Delay LM5100A/B/C	HI Falling to HO Falling		20	45	20	ns
HO Turn-Off Propagation Delay LM5101A/B/C			22	56	22	ns
LO Turn-On Propagation Delay LM5100A/B/C	HI Rising to HO Rising		20	45	20	ns
LO Turn-On Propagation Delay LM5101A/B/C			26	56	26	ns
Delay Matching: LO on & HO off LM5100A/B/C			1		0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Delay Matching: LO off & HO on LM5100A/B/C			1	10	0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Either Output Rise/Fall Time	CL = 1000 pF		8		3	ns
Output Rise Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		430		242	ns
Output Rise Time (3V to 9V) LM5100B/LM51-01B			570		282	ns
Output Rise Time(3V to 9V) LM5100C/LM5-101C			990		606	ns
Output Fall Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		260		121	ns
Output Fall Time (3V to 9V)			430		161	ns

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LM5100B/LM51-01B						
Output Fall Time (3V to 9V) LM5100C/LM5-101C			715		282	ns

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Examples

Example circuit :

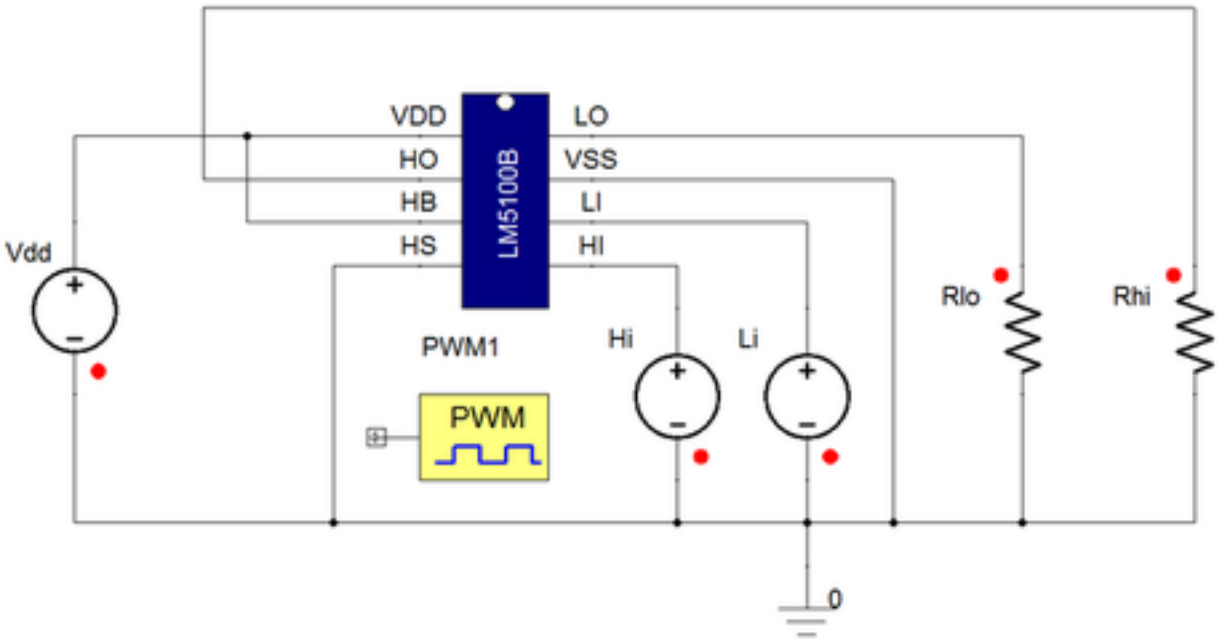

Figure 2. Example Circuit

Simulation results :

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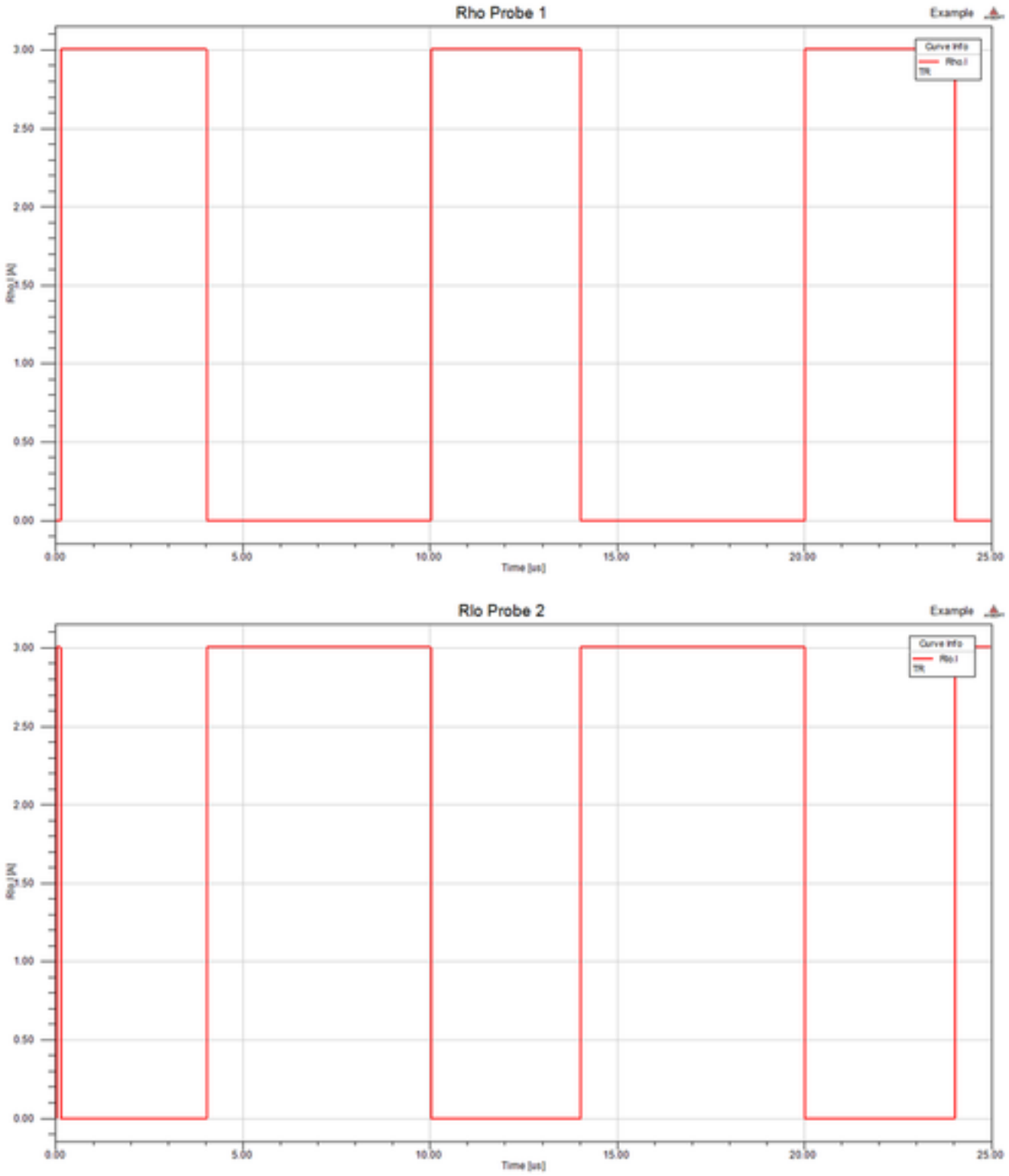

Figure 3. Simulation results

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References

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LM5100C: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

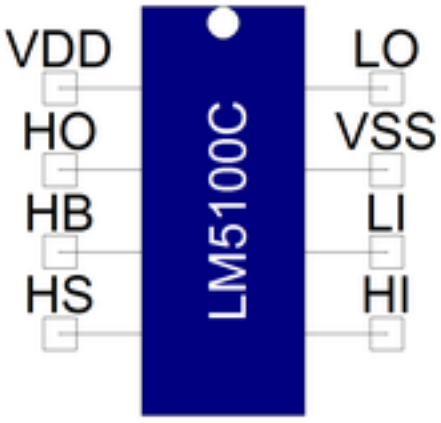

Figure 1. Component symbol

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Description

The *LM5100A/B/C* and *LM5101A/B/C* High Voltage Gate Drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The "A" versions provide a full 3A of gate drive while the "B" and "C" versions provide 2A and 1A respectively. The outputs are independently controlled with CMOS input thresholds (*LM5100A/B/C*) or TTL input thresholds (*LM5101A/B/C*). An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control

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logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin, PSOP-8 pin and the LLP-10 pin packages. The *LM5100C* and *LM5101C* are also available in eMSOP-8 package. The *LM5101A* is also available in LLP-8 pin package.

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Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Currents						
VDD Quiescent Current, LM5100A/B/-C	LI = HI = 0V		0.1	0.2	0.1	mA
VDD Quiescent Current, LM5101A/B/-C	LI = HI = 0V		0.25	0.4	0.25	mA
VDD Operating Current	f = 500 kHz		2.0	3	-	mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2	-	mA
Total HB Operating Current	f = 500 kHz		1.6	3	-	mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.1	10	-	uA
HB to VSS Current, Operating	f = 500 kHz		0.4		-	mA
Input Pins						
Input Voltage Threshold LM5100A/B/-C	Rising Edge	4.5	5.4	6.3	5.4	V
Input Voltage Threshold LM5101A/B/-C	Rising Edge	1.3	1.8	2.3	1.8	V
Input Voltage Hysteresis LM5100A/B/-C			500		500	mV
Input Voltage Hysteresis LM5101A/B/-C			50		50	mV
Input Pull-down Resist-		100	200	400	200	kohm

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Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current Forward Voltage	IVDD-HB = 100 µA		0.52	0.85	0.52	V
High-Current Forward Voltage	IVDD-HB = 100 mA		0.8	1	0.8	V
Dynamic Resistance LM5100A/B/-C, LM5101A/B/-C	IVDD-HB = 100 mA		1.0	1.65	-	ohm

Table 3

PARAMETERS	TEST CONDITIO-NS	MIN	TYP	MA-X	MODE-L	UNIT-S
LO &HO Gate Driver						
Low-Level Out-put Voltage LM5100A/LM51-01A	IHO = ILO = 100 mA		0.12	0.25	0.12	V
Low-Level Out-put Voltage LM5100B/LM51-01B			0.16	0.4	0.16	V
Low-Level Out-put Voltage LM5100C/LM5-101C			0.28	0.65	0.28	V
High-Level Out-	IHO = ILO		0.24	0.45	0.24	V

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	= 100 mA					
High-Level Output Voltage LM5100B/LM5101B	VOH = VDD - LO or		0.28	0.60	0.28	V
High-Level Output Voltage LM5100C/LM5101C	VOH = HB - HO		0.60	1.10	0.60	V
Peak Pullup Current LM5100A/LM5101A	HO, LO = 0V		3		3	A
Peak Pullup Current LM5100B/LM5101B			2		2	A
Peak Pullup Current LM5100C/LM5101C			1		1	A
Peak Pulldown Current LM5100A/LM5101A	HO, LO = 12V		3		3	A
Peak Pulldown Current LM5100B/LM5101B			2		2	A
Peak Pulldown Current LM5100C/LM5101C			1		1	A

Table 4

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Switching Characteristics						
LO Turn-Off Propagation Delay LM5100A/B/C	LI Falling to LO Falling		20	45	20	ns
LO Turn-Off Propagation Delay			22	56	22	ns

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LM5101A/B/C						
LO Turn-On Propagation Delay LM5100A/B/C	LI Rising to LO Rising		20	45	20	ns
LO Turn-On Propagation Delay LM5101A/B/C			26	56	26	ns
HO Turn-Off Propagation Delay LM5100A/B/C	HI Falling to HO Falling		20	45	20	ns
HO Turn-Off Propagation Delay LM5101A/B/C			22	56	22	ns
LO Turn-On Propagation Delay LM5100A/B/C	HI Rising to HO Rising		20	45	20	ns
LO Turn-On Propagation Delay LM5101A/B/C			26	56	26	ns
Delay Matching: LO on & HO off LM5100A/B/C			1		0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Delay Matching: LO off & HO on LM5100A/B/C			1	10	0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Either Output Rise/Fall Time	CL = 1000 pF		8		3	ns
Output Rise Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		430		242	ns
Output Rise Time (3V to 9V) LM5100B/LM51-01B			570		282	ns
Output Rise Time(3V to 9V)			990		606	ns

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LM5100C/LM5-101C						
Output Fall Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		260		121	ns
Output Fall Time (3V to 9V) LM5100B/LM51-01B			430		161	ns
Output Fall Time (3V to 9V) LM5100C/LM5-101C			715		282	ns

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Example circuit :

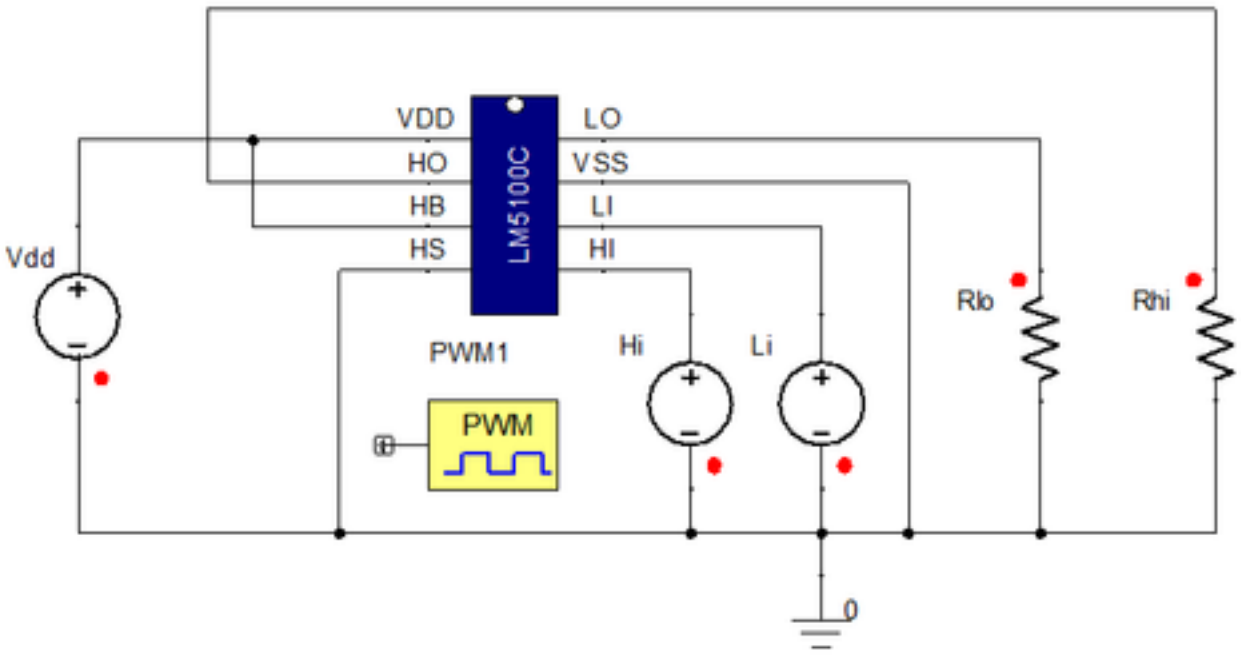

Figure 2. Example Circuit

Simulation results :

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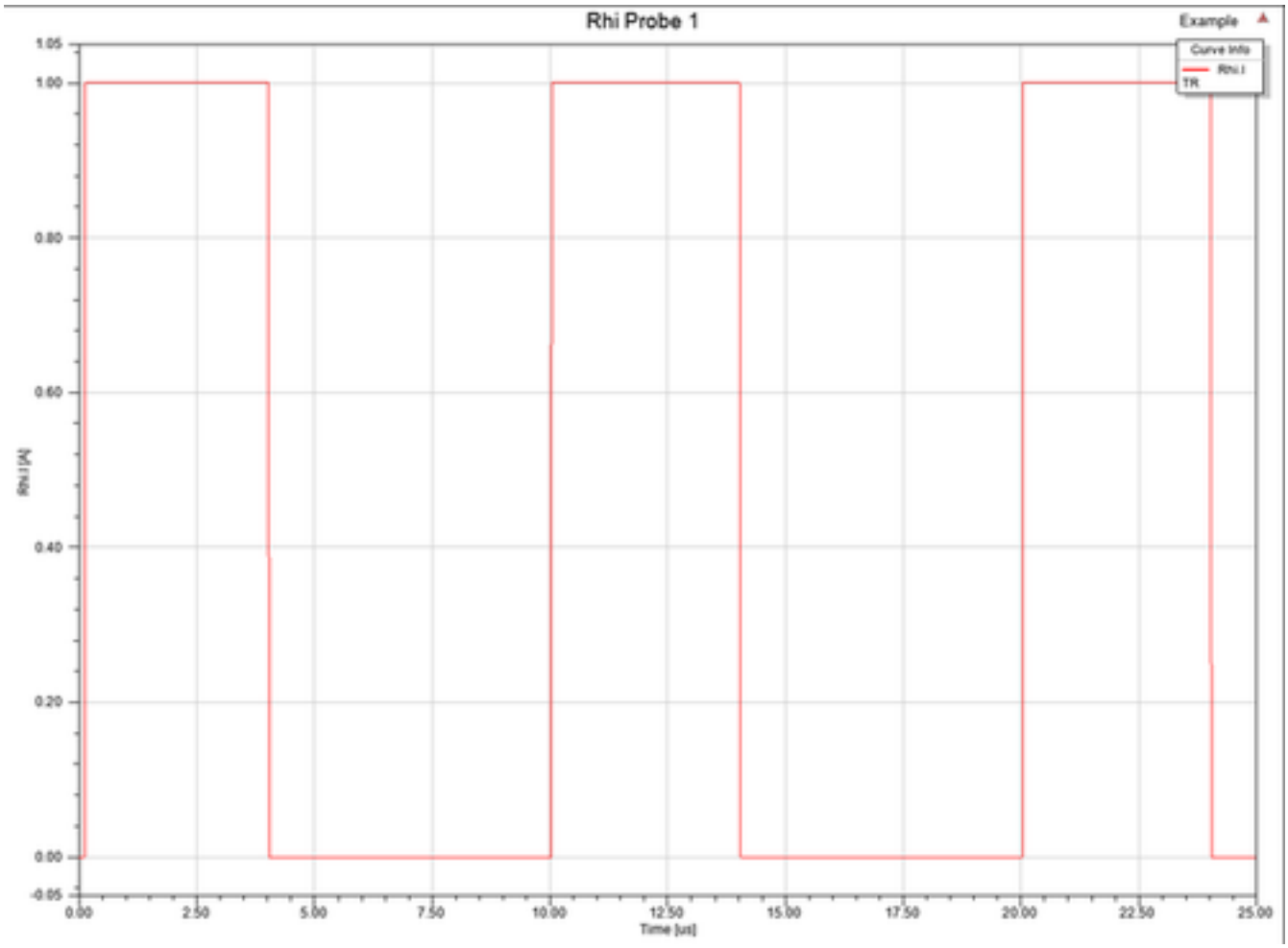

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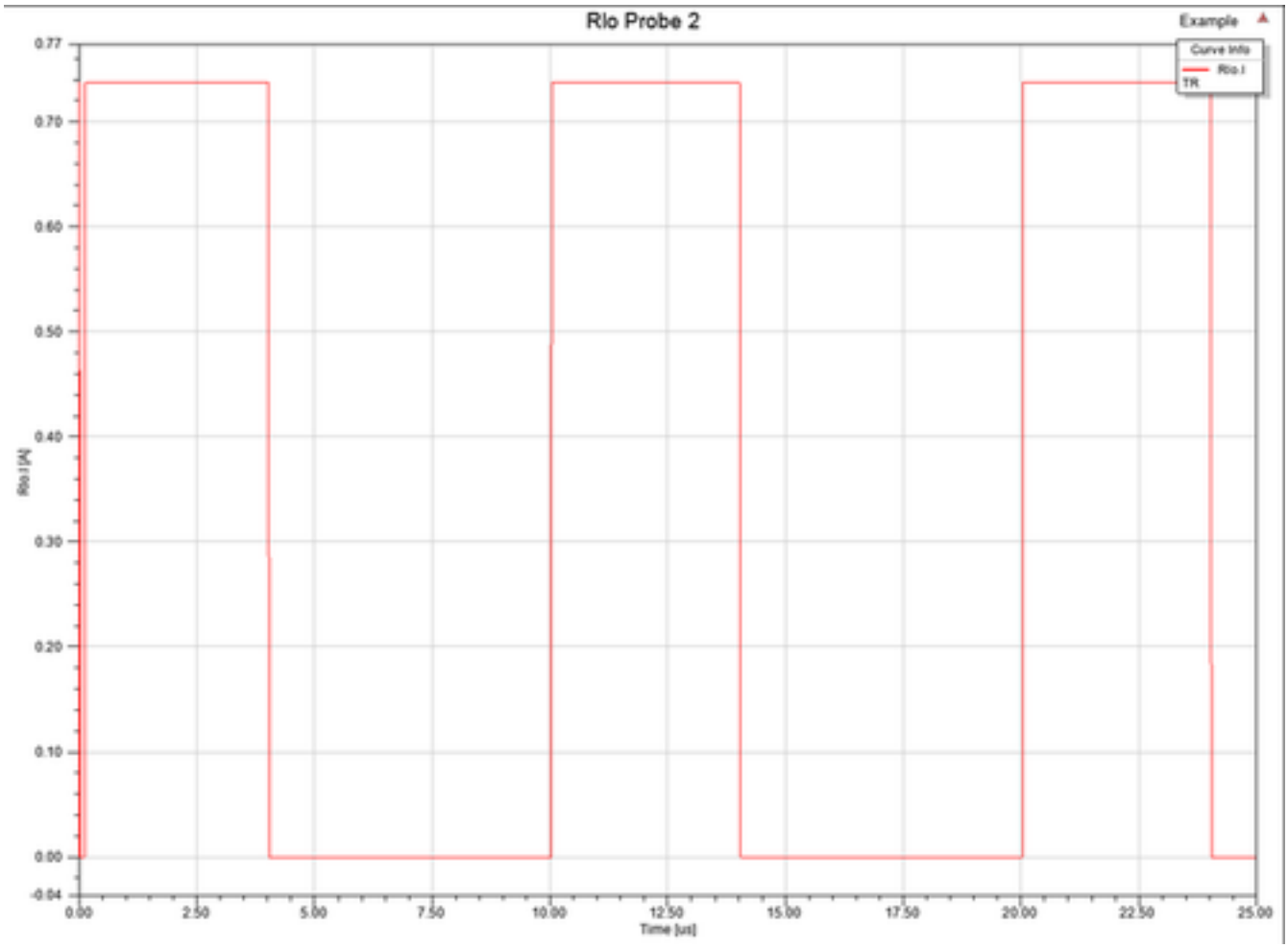

Figure 3. Simulation results

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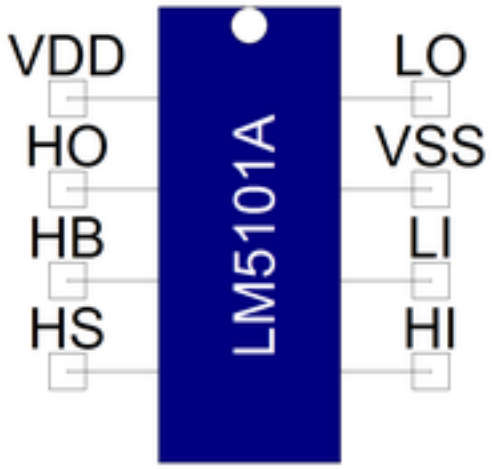
LM5101A: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM5100A/B/C* and *LM5101A/B/C* High Voltage Gate Drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The "A" versions provide a full 3A of gate drive while the "B" and "C" versions provide 2A and 1A respectively. The outputs are independently controlled with CMOS input thresholds (*LM5100A/B/C*) or TTL input thresholds (*LM5101A/B/C*). An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control

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Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

Table 2

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
Supply Currents						
VDD Qui-escent Cur-	LI = HI = 0V		0.1	0.2	0.1	mA

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rent, LM5100A/B/-C						
VDD Quiescent Current, LM5101A/B/-C	LI = HI = 0V		0.25	0.4	0.25	mA
VDD Operating Current	f = 500 kHz		2.0	3		mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2		mA
Total HB Operating Current	f = 500 kHz		1.6	3		mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.1	10		uA
HB to VSS Current, Operating	f = 500 kHz		0.4			mA
Input Pins						
Input Voltage Threshold LM5100A/B/-C	Rising Edge	4.5	5.4	6.3	5.4	V
Input Voltage Threshold LM5101A/B/-C	Rising Edge	1.3	1.8	2.3	1.8	V
Input Voltage Hysteresis LM5100A/B/-C			500		500	mV
Input Voltage Hysteresis LM5101A/B/-C			50		50	mV
Input Pull-down Resistance		100	200	400	200	kohm
Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V

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HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current Forward Voltage	IVDD-HB = 100 µA		0.52	0.85	0.52	V
High-Current Forward Voltage	IVDD-HB = 100 mA		0.8	1	0.8	V
Dynamic Resistance LM5100A/B/-C, LM5101A/B/-C	IVDD-HB = 100 mA		1.0	1.65		ohm

Table 3

PARAMETERS	TEST CONDITIO-NS	MIN	TYP	MA-X	MODE-L	UNIT-S
LO &HO Gate Driver						
Low-Level Out-put Voltage LM5100A/LM51-01A	IHO = ILO = 100 mA		0.12	0.25	0.12	V
Low-Level Out-put Voltage LM5100B/LM51-01B			0.16	0.4	0.16	V
Low-Level Out-put Voltage LM5100C/LM5-101C			0.28	0.65	0.28	V
High-Level Out-put Voltage LM5100A/LM51-01A	IHO = ILO = 100 mA VOH = VDD - LO or VOH = HB - HO		0.24	0.45	0.24	V
High-Level Out-put Voltage LM5100B/LM51-01B			0.28	0.60	0.28	V
High-Level Out-put Voltage			0.60	1.10	0.60	V

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Peak Pullup Current LM5100A/LM5101A	HO, LO = 0V		3		3	A
Peak Pullup Current LM5100B/LM5101B			2		2	A
Peak Pullup Current LM5100C/LM5101C			1		1	A
Peak Pulldown Current LM5100A/LM5101A	HO, LO = 12V		3		3	A
Peak Pulldown Current LM5100B/LM5101B			2		2	A
Peak Pulldown Current LM5100C/LM5101C			1		1	A

Table 4

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Switching Characteristics						
LO Turn-Off Propagation Delay LM5100A/B/C	LI Falling to LO Falling		20	45	20	ns
LO Turn-Off Propagation Delay LM5101A/B/C			22	56	22	ns
LO Turn-On Propagation Delay LM5100A/B/C	LI Rising to LO Rising		20	45	20	ns
LO Turn-On Propagation Delay			26	56	26	ns

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LM5101A/B/C						
HO Turn-Off Propagation Delay LM5100A/B/C	HI Falling to HO Falling		20	45	20	ns
HO Turn-Off Propagation Delay LM5101A/B/C			22	56	22	ns
LO Turn-On Propagation Delay LM5100A/B/C	HI Rising to HO Rising		20	45	20	ns
LO Turn-On Propagation Delay LM5101A/B/C			26	56	26	ns
Delay Matching: LO on & HO off LM5100A/B/C			1		0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Delay Matching: LO off & HO on LM5100A/B/C			1	10	0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Either Output Rise/Fall Time	CL = 1000 pF		8		3	ns
Output Rise Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		430		242	ns
Output Rise Time (3V to 9V) LM5100B/LM51-01B			570		282	ns
Output Rise Time (3V to 9V) LM5100C/LM5-101C			990		606	ns
Output Fall	CL = 0.1 µF		260		121	ns

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Time (3V to 9V) LM5100A/LM51-01A						
Output Fall Time (3V to 9V) LM5100B/LM51-01B			430		161	ns
Output Fall Time (3V to 9V) LM5100C/LM5-101C			715		282	ns

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Examples

Example circuit :

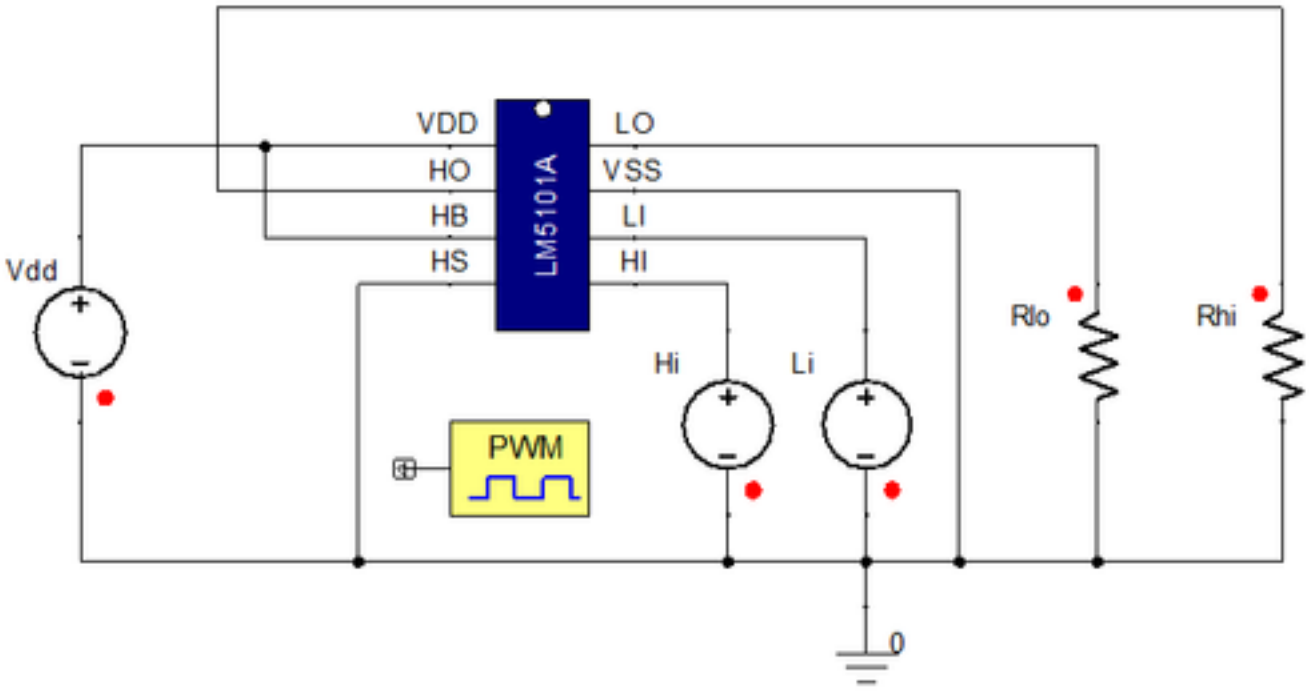

Figure 2. Example Circuit

Simulation results :

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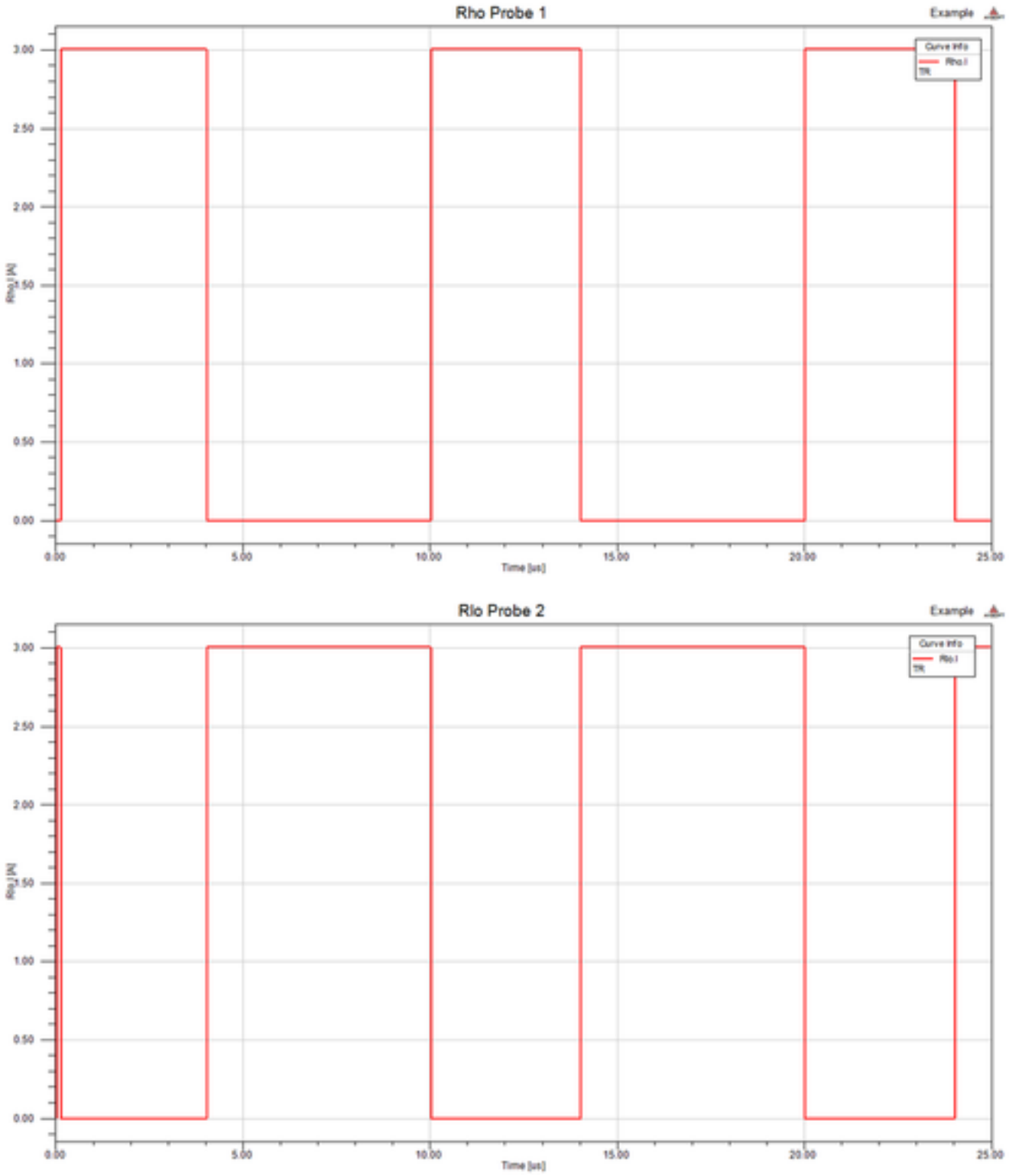

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LM5101B: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

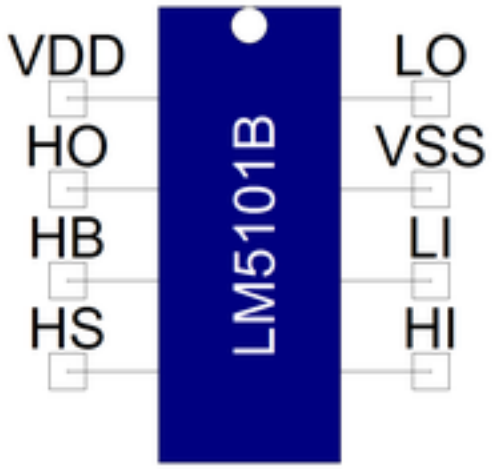

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Table 1

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5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Currents						
VDD Quiescent Current, LM5100A/B/-C	LI = HI = 0V		0.1	0.2	0.1	mA
VDD Quiescent Current, LM5101A/B/-C	LI = HI = 0V		0.25	0.4	0.25	mA
VDD Operating Current	f = 500 kHz		2.0	3		mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2		mA
Total HB Operating Current	f = 500 kHz		1.6	3		mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.1	10		uA
HB to VSS Current, Operating	f = 500 kHz		0.4			mA
Input Pins						
Input Voltage Threshold LM5100A/B/-C	Rising Edge	4.5	5.4	6.3	5.4	V
Input Voltage Threshold LM5101A/B/-C	Rising Edge	1.3	1.8	2.3	1.8	V
Input Voltage Hysteresis LM5100A/B/-C			500		500	mV
Input Voltage Hysteresis LM5101A/B/-C			50		50	mV
Input Pull-down Resist-		100	200	400	200	kohm

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Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current Forward Voltage	IVDD-HB = 100 µA		0.52	0.85	0.52	V
High-Current Forward Voltage	IVDD-HB = 100 mA		0.8	1	0.8	V
Dynamic Resistance LM5100A/B/-C, LM5101A/B/-C	IVDD-HB = 100 mA		1.0	1.65		ohm

Table 3

PARAMETERS	TEST CONDITIO-NS	MIN	TYP	MA-X	MODE-L	UNIT-S
LO &HO Gate Driver						
Low-Level Out-put Voltage LM5100A/LM51-01A	IHO = ILO = 100 mA		0.12	0.25	0.12	V
Low-Level Out-put Voltage LM5100B/LM51-01B			0.16	0.4	0.16	V
Low-Level Out-put Voltage LM5100C/LM5-101C			0.28	0.65	0.28	V
High-Level Out-	IHO = ILO		0.24	0.45	0.24	V

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	= 100 mA					
High-Level Output Voltage LM5100B/LM5101B	VOH = VDD - LO or		0.28	0.60	0.28	V
High-Level Output Voltage LM5100C/LM5101C	VOH = HB - HO		0.60	1.10	0.60	V
Peak Pullup Current LM5100A/LM5101A	HO, LO = 0V		3		3	A
Peak Pullup Current LM5100B/LM5101B			2		2	A
Peak Pullup Current LM5100C/LM5101C			1		1	A
Peak Pulldown Current LM5100A/LM5101A	HO, LO = 12V		3		3	A
Peak Pulldown Current LM5100B/LM5101B			2		2	A
Peak Pulldown Current LM5100C/LM5101C			1		1	A

Table 4

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Switching Characteristics						
LO Turn-Off Propagation Delay LM5100A/B/C	LI Falling to LO Falling		20	45	20	ns
LO Turn-Off Propagation Delay			22	56	22	ns

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LM5101A/B/C						
LO Turn-On Propagation Delay LM5100A/B/C	LI Rising to LO Rising		20	45	20	ns
LO Turn-On Propagation Delay LM5101A/B/C			26	56	26	ns
HO Turn-Off Propagation Delay LM5100A/B/C	HI Falling to HO Falling		20	45	20	ns
HO Turn-Off Propagation Delay LM5101A/B/C			22	56	22	ns
LO Turn-On Propagation Delay LM5100A/B/C	HI Rising to HO Rising		20	45	20	ns
LO Turn-On Propagation Delay LM5101A/B/C			26	56	26	ns
Delay Matching: LO on & HO off LM5100A/B/C			1		0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Delay Matching: LO off & HO on LM5100A/B/C			1	10	0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Either Output Rise/Fall Time	CL = 1000 pF		8		3	ns
Output Rise Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		430		242	ns
Output Rise Time (3V to 9V) LM5100B/LM51-01B			570		282	ns
Output Rise Time(3V to 9V)			990		606	ns

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LM5100C/LM5-101C						
Output Fall Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		260		121	ns
Output Fall Time (3V to 9V) LM5100B/LM51-01B			430		161	ns
Output Fall Time (3V to 9V) LM5100C/LM5-101C			715		282	ns

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Examples

Example circuit :

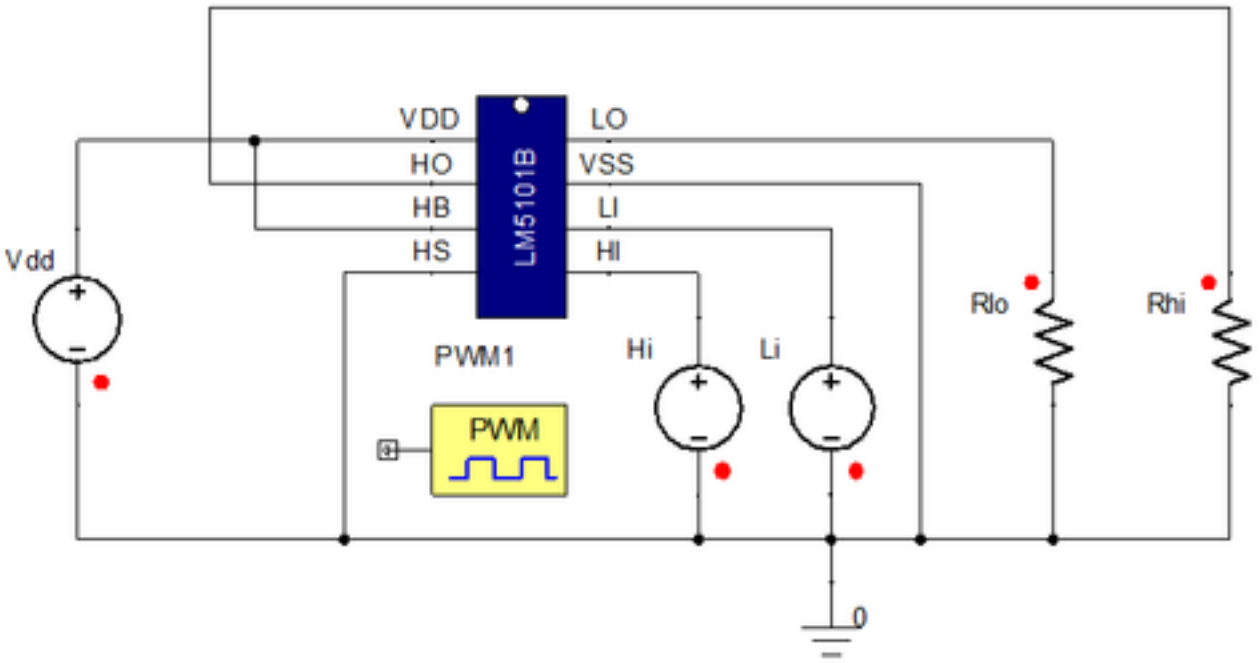

Figure 2. Example Circuit

Simulation results :

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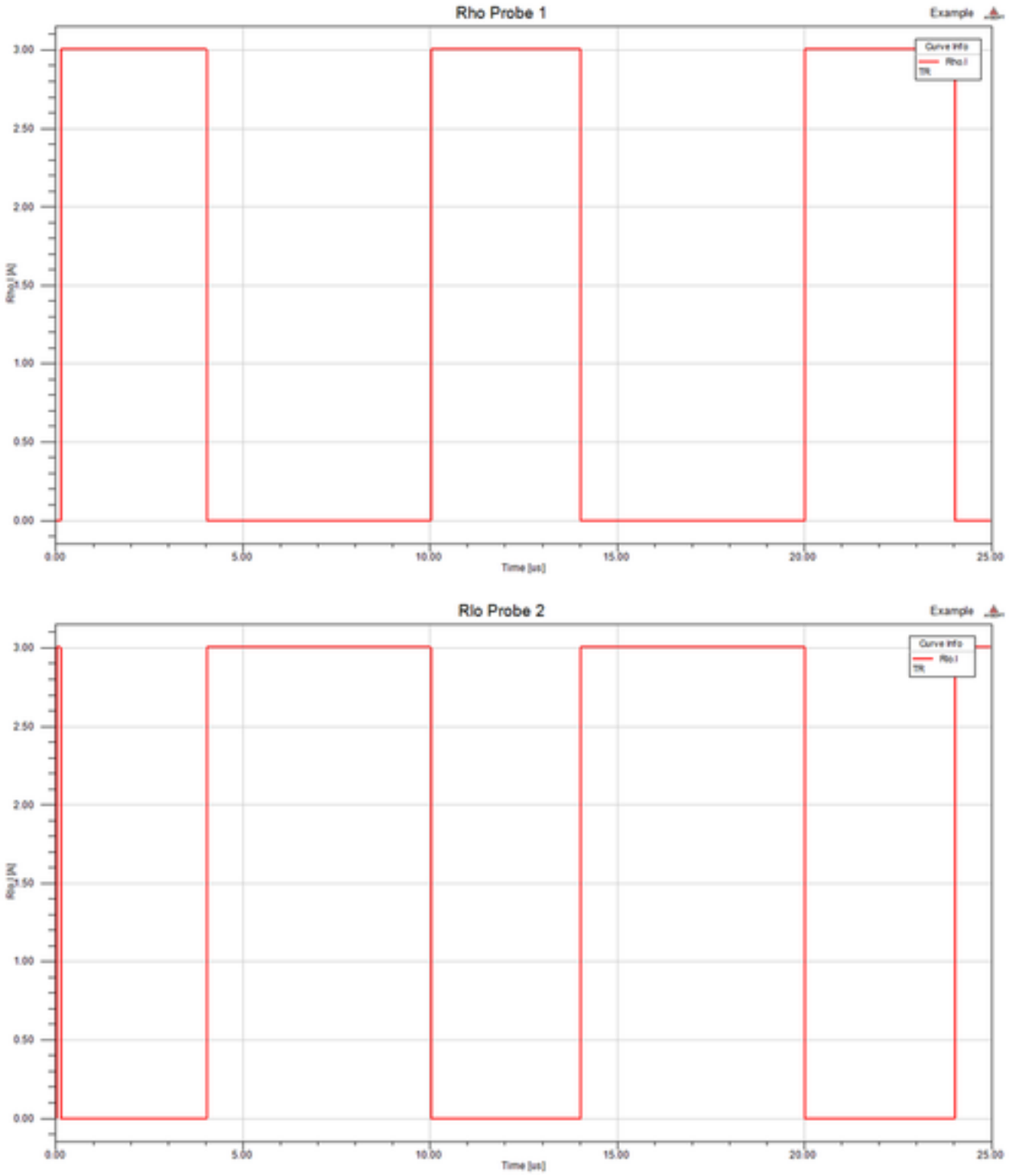

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References

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LM5101C: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

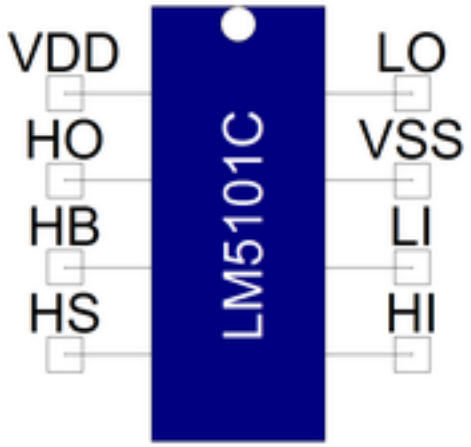

Figure 1. Component symbol

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• Example

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Description

The *LM5100A/B/C* and *LM5101A/B/C* High Voltage Gate Drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The "A" versions provide a full 3A of gate drive while the "B" and "C" versions provide 2A and 1A respectively. The outputs are independently controlled with CMOS input thresholds (*LM5100A/B/C*) or TTL input thresholds (*LM5101A/B/C*). An integrated high voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control

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logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin, PSOP-8 pin and the LLP-10 pin packages. The *LM5100C* and *LM5101C* are also available in eMSOP-8 package. The *LM5101A* is also available in LLP-8 pin package.

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Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

Table 2

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
Supply Currents						
VDD Qui-escent Cur-	LI = HI = 0V		0.1	0.2	0.1	mA

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rent, LM5100A/B/-C						
VDD Quiescent Current, LM5101A/B/-C	LI = HI = 0V		0.25	0.4	0.25	mA
VDD Operating Current	f = 500 kHz		2.0	3	-	mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2	-	mA
Total HB Operating Current	f = 500 kHz		1.6	3	-	mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.1	10	-	uA
HB to VSS Current, Operating	f = 500 kHz		0.4		-	mA
Input Pins						
Input Voltage Threshold LM5100A/B/-C	Rising Edge	4.5	5.4	6.3	5.4	V
Input Voltage Threshold LM5101A/B/-C	Rising Edge	1.3	1.8	2.3	1.8	V
Input Voltage Hysteresis LM5100A/B/-C			500		500	mV
Input Voltage Hysteresis LM5101A/B/-C			50		50	mV
Input Pull-down Resistance		100	200	400	200	kohm
Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V

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HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current Forward Voltage	IVDD-HB = 100 µA		0.52	0.85	0.52	V
High-Current Forward Voltage	IVDD-HB = 100 mA		0.8	1	0.8	V
Dynamic Resistance LM5100A/B/-C, LM5101A/B/-C	IVDD-HB = 100 mA		1.0	1.65	-	ohm

Table 3

PARAMETERS	TEST CONDITIO-NS	MIN	TYP	MA-X	MODE-L	UNIT-S
LO &HO Gate Driver						
Low-Level Out-put Voltage LM5100A/LM51-01A	IHO = ILO = 100 mA		0.12	0.25	0.12	V
Low-Level Out-put Voltage LM5100B/LM51-01B			0.16	0.4	0.16	V
Low-Level Out-put Voltage LM5100C/LM5-101C			0.28	0.65	0.28	V
High-Level Out-put Voltage LM5100A/LM51-01A	IHO = ILO = 100 mA VOH = VDD - LO or VOH = HB - HO		0.24	0.45	0.24	V
High-Level Out-put Voltage LM5100B/LM51-01B			0.28	0.60	0.28	V
High-Level Out-put Voltage			0.60	1.10	0.60	V

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Peak Pullup Current LM5100A/LM5101A	HO, LO = 0V		3		3	A
Peak Pullup Current LM5100B/LM5101B			2		2	A
Peak Pullup Current LM5100C/LM5101C			1		1	A
Peak Pulldown Current LM5100A/LM5101A	HO, LO = 12V		3		3	A
Peak Pulldown Current LM5100B/LM5101B			2		2	A
Peak Pulldown Current LM5100C/LM5101C			1		1	A

Table 4

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Switching Characteristics						
LO Turn-Off Propagation Delay LM5100A/B/C	LI Falling to LO Falling		20	45	20	ns
LO Turn-Off Propagation Delay LM5101A/B/C			22	56	22	ns
LO Turn-On Propagation Delay LM5100A/B/C	LI Rising to LO Rising		20	45	20	ns
LO Turn-On Propagation Delay			26	56	26	ns

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LM5101A/B/C						
HO Turn-Off Propagation Delay LM5100A/B/C	HI Falling to HO Falling		20	45	20	ns
HO Turn-Off Propagation Delay LM5101A/B/C			22	56	22	ns
LO Turn-On Propagation Delay LM5100A/B/C	HI Rising to HO Rising		20	45	20	ns
LO Turn-On Propagation Delay LM5101A/B/C			26	56	26	ns
Delay Matching: LO on & HO off LM5100A/B/C			1		0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Delay Matching: LO off & HO on LM5100A/B/C			1	10	0	ns
Delay Matching: LO on & HO off LM5101A/B/C			4	10	0	ns
Either Output Rise/Fall Time	CL = 1000 pF		8		3	ns
Output Rise Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		430		242	ns
Output Rise Time (3V to 9V) LM5100B/LM51-01B			570		282	ns
Output Rise Time(3V to 9V) LM5100C/LM5-101C			990		606	ns
Output Fall Time (3V to 9V) LM5100A/LM51-01A	CL = 0.1 µF		260		121	ns
Output Fall Time (3V to 9V)			430		161	ns

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LM5100B/LM51-01B						
Output Fall Time (3V to 9V) LM5100C/LM5-101C			715		282	ns

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Examples

Example circuit :

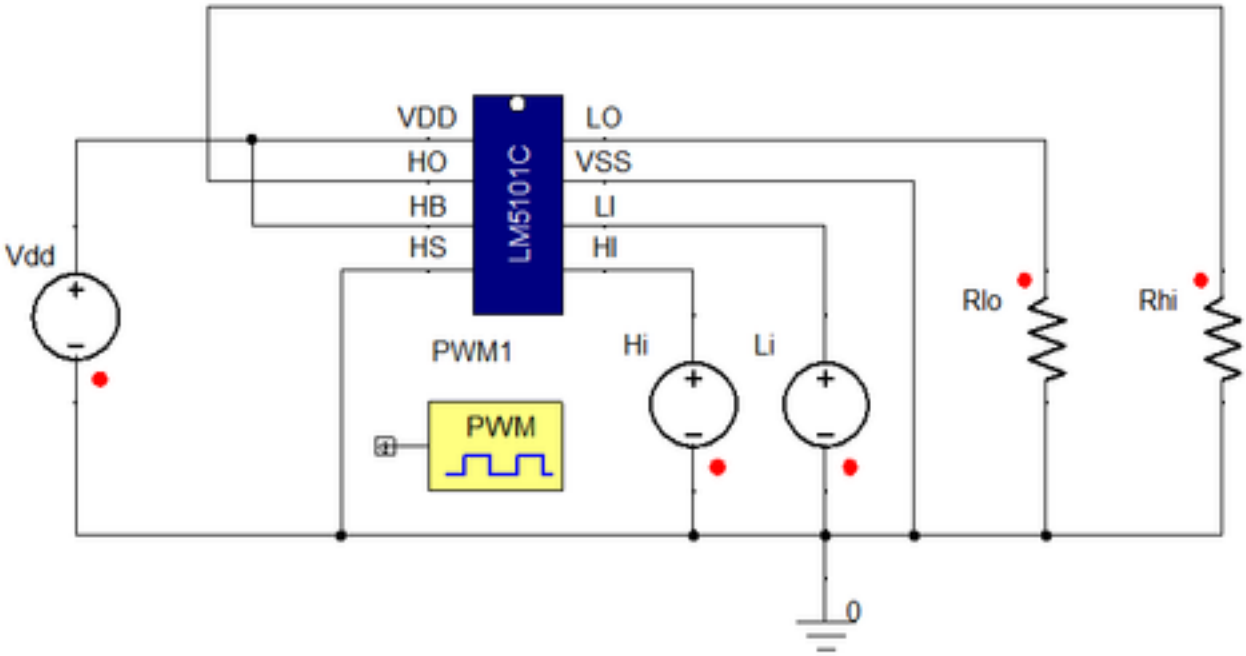

Figure 2. Example Circuit

Simulation results :

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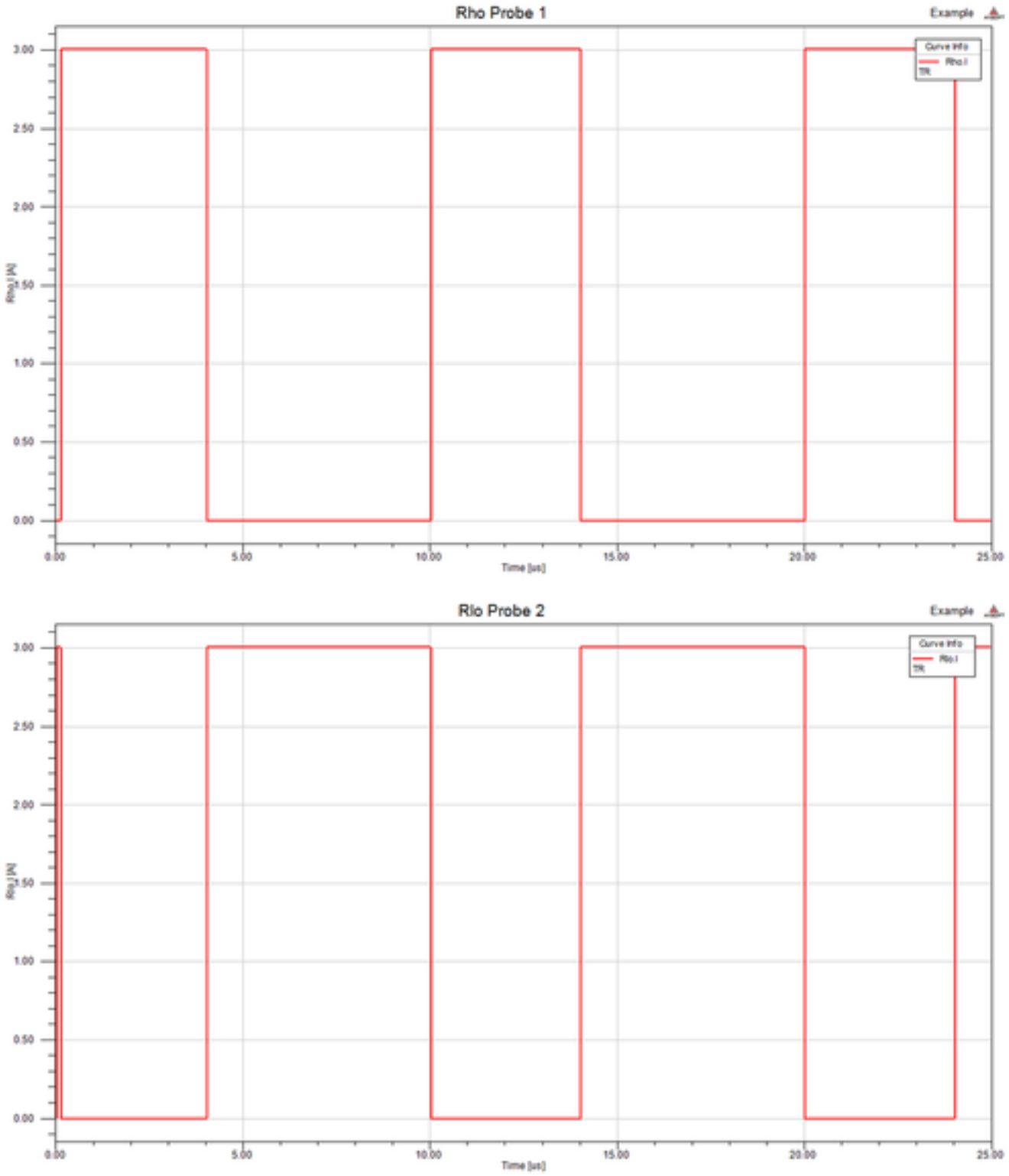

Figure 3. Simulation results

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References

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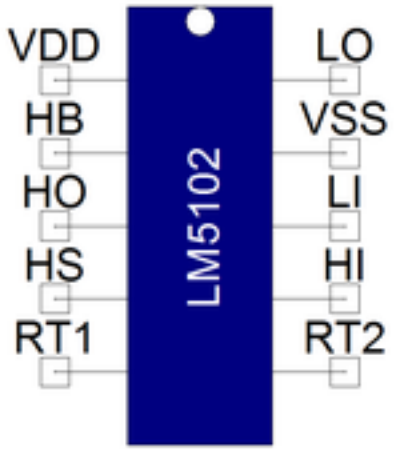
LM5102: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM5102* High Voltage Gate Driver is designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with supply voltages up to 100V. The outputs are independently controlled. The rising edge of each output can be independently delayed with a programming resistor. An integrated high voltage diode is provided to charge the high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from control logic to the high side gate driver.

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Under-voltage lockout is provided on both the low side and the high side power rails. This device is available in the standard MSOP-10 pin and the LLP-10 pin packages.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	RT1	High side output edge delay programming
6	RT2	Low side output edge delay programming
7	HI	High-side driver control input
8	LI	Low-side driver control input
9	VSS	Ground return
10	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Currents						
VDD Quiescent Current	LI = HI = 0V		0.4	0.6	0.4	mA
VDD Operating Current	f = 500 kHz		1.5	3		mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2		mA
Total HB Operating Current	f = 500 kHz		1.3	3		mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.05	10		uA
HB to VSS Current, Operating	f = 500 kHz		0.08			mA
Input Pins						
Low Level Input Voltage Threshold	Rising Edge	0.8	1.8		1.8	V
High Level Input Voltage Threshold			1.8	2.2	1.8	mV
Input Pull-down Resistance		100	200	500	200	kohm
Time Delay Controls						
Nominal Voltage at RT		2.7	3	3.3	3	V
RT Pin Current Limit		0.75	1.5	2.25	1.5	mA
Delay Timer, RT=10 kΩ		58	90	130	90	ns
Delay Timer, RT=100 kΩ		140	200	270	200	ns
Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold			0.5		0.5	V

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HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current Forward Voltage	IVDD-HB = 100 µA		0.60	0.9	.0.6	V
High-Current Forward Voltage	IVDD-HB = 100 mA		0.85	1.1	0.85	V
Dynamic Resistance	IVDD-HB = 100 mA		1.0	1.65		ohm

Table 3

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
LO Gate Driver						
Low-Level Output Voltage	ILO = 100 mA		0.25	0.4	0.25	V
High-Level Output Voltage	ILO = -100 mA, VOHL = VDD - VLO		0.35	0.55	0.35	V
Peak Pullup Current	VHO = 0V		1.6		1.6	A
Peak Pull-down Current	VHO = 12V		1.8		1.8	A
HO Gate Driver						
Low-Level Output Voltage	IHO = 100 mA		0.25	0.4	0.25	V
High-Level Output Voltage	IHO = -100 mA, VOHH = VHB - VHO		0.35	0.55	0.35	V
Peak Pullup Current	VHO = 0V		1.6		1.6	A

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Peak Pull-down Current	VHO = 12V		1.8		1.8	A
Switching Char-acteristics						
Lower Turn-Off Propaga-tion Delay			27	56	27	ns
Upper Turn-Off Propaga-tionDelay			27	56	27	ns
Either Output Rise/Fall Time	CL = 1000 pF		15		8	ns
Either Output Rise/Fall Time (3V to 9V)	CL = 0.1 µF		0.6		230	ns
Bootstrap DiodeTurn-Off Time	IF = 20 mA IR = 200 mA		50			ns

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Examples

Example circuit :

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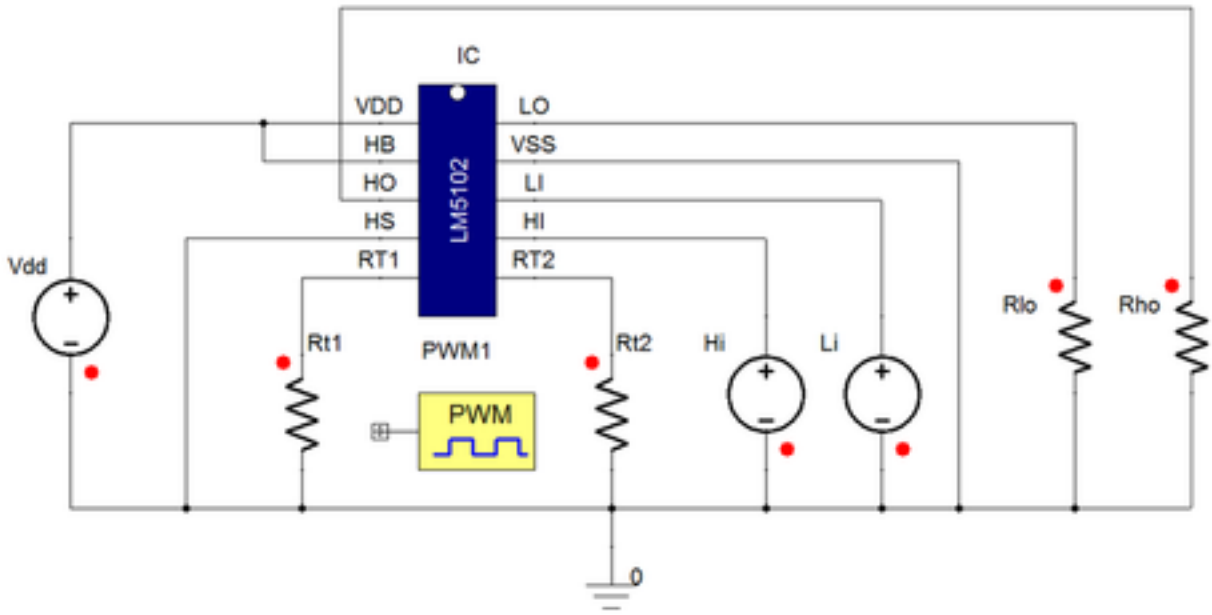
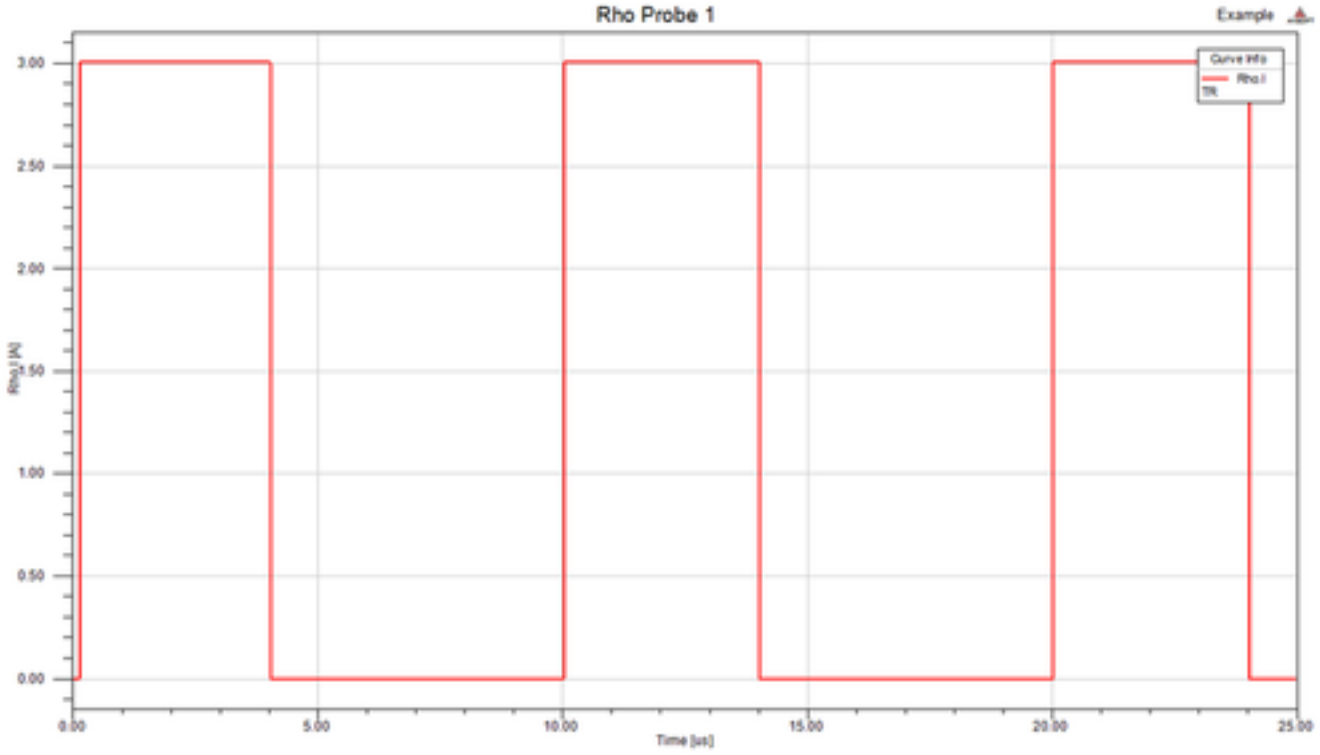


Figure 2. Example Circuit

Simulation results :



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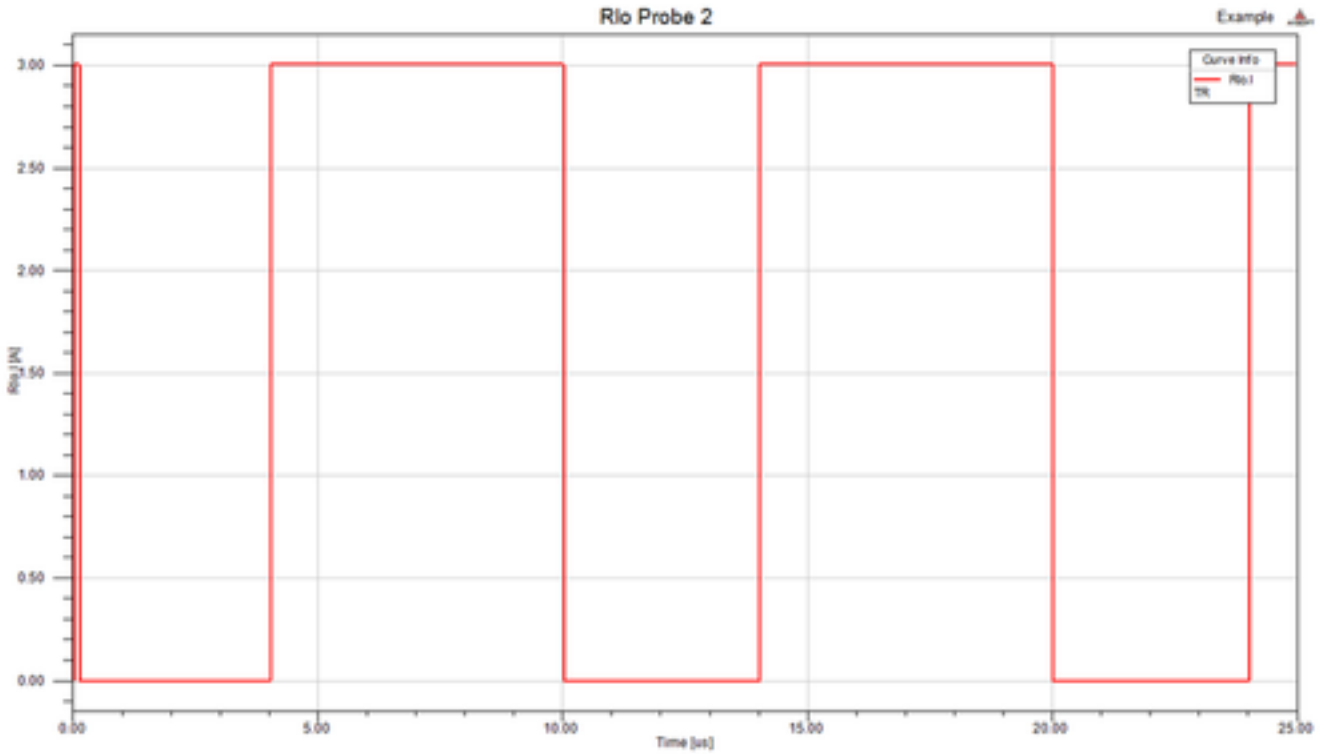

Figure 3. Simulation results

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LM5104: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

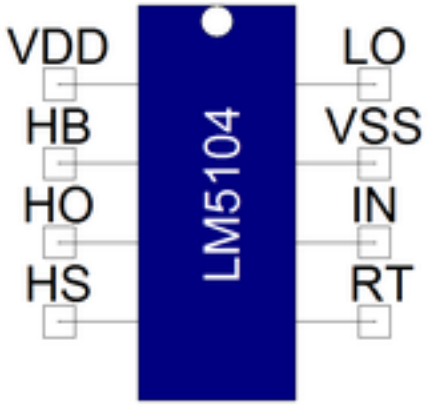

Figure 1. Component symbol

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Description

The *LM5104* High Voltage Gate Driver is designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck configuration. The floating high-side driver is capable of working with supply voltages up to 100V. The high side and low side gate drivers are controlled from a single input. Each change in state is controlled in an adaptive manner to prevent shoot-through issues. In addition to the adaptive transition timing, an additional delay time can be added, proportional to an external setting resistor. An integrated high voltage diode is provided to charge high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control

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logic to the high side gate driver. Undervoltage lockout is provided on both the low side and the high side power rails. This device is available in the standard SOIC-8 pin and the LLP-10 pin packages.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	RT	Deadtime programming pin
6	LI	Control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Currents						
VDD Quiescent Current	LI = HI = 0V		0.4	0.6	0.4	mA

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VDD Operating Current	f = 500 kHz		1.9	3		mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2		mA
Total HB Operating Current	f = 500 kHz		1.3	3		mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.05	10		uA
HB to VSS Current, Operating	f = 500 kHz		0.08			mA
Input Pins						
Low Level Input Voltage Threshold	Rising Edge	0.8	1.8		1.8	V
High Level Input Voltage Threshold			1.8	2.2	1.8	mV
Input Pull-down Resistance		100	200	500	200	kohm
Time Delay Controls						
Nominal Voltage at RT		2.7	3	3.3	3	V
RT Pin Current Limit		0.75	1.5	2.25	1.5	mA
Delay Timer, RT=10 kΩ		58	90	130	90	ns
Delay Timer, RT=100 kΩ		140	200	270	200	ns
Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current	IVDD-HB =		0.60	0.9	.0.6	V

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Forward Voltage	100 µA					
High-Current Forward Voltage	IVDD-HB = 100 mA		0.85	1.1	0.85	V
Dynamic Resistance	IVDD-HB = 100 mA		0.8	1.5		ohm

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Table 3

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
LO Gate Driver						
Low-Level Output Voltage	ILO = 100 mA		0.25	0.4	0.25	V
High-Level Output Voltage	ILO = -100 mA, VOHL = VDD - VLO		0.35	0.55	0.35	V
Peak Pullup Current	VHO = 0V		1.6		1.6	A
Peak Pull-down Current	VHO = 12V		1.8		1.8	A
HO Gate Driver						
Low-Level Output Voltage	IHO = 100 mA		0.25	0.4	0.25	V
High-Level Output Voltage	IHO = -100 mA, VOHH = VHB - VHO		0.35	0.55	0.35	V
Peak Pullup Current	VHO = 0V		1.6		1.6	A
Peak Pull-down Current	VHO = 12V		1.8		1.8	A
Switching Char-acteristics						
Lower Turn-Off Propaga-tion Delay			25	56	25	ns
Upper Turn-Off Propaga-tion Delay			25	56	25	ns
Either Output Rise/Fall Time	CL = 1000 pF		15		8	ns
Either Output Rise/Fall Time (3V to 9V)	CL = 0.1 µF		0.6		230	ns
Bootstrap	IF = 20 mA		50			ns

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Diode Turn-Off Time	IR = 200 mA					

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Example circuit :

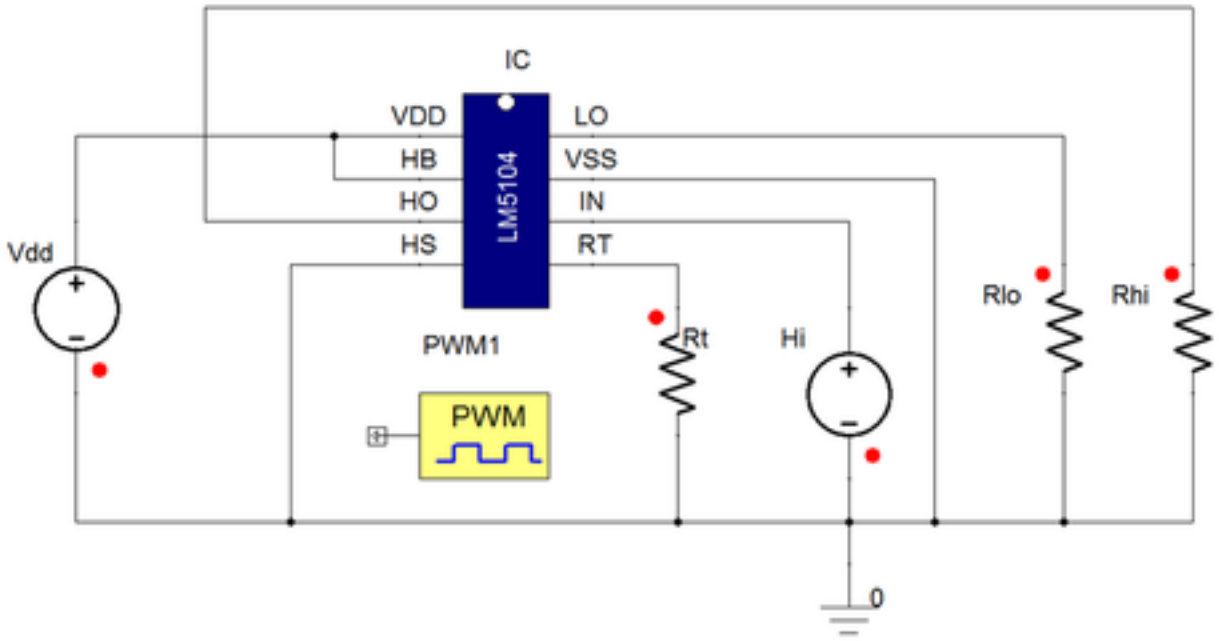

Figure 2. Example Circuit

Simulation results :

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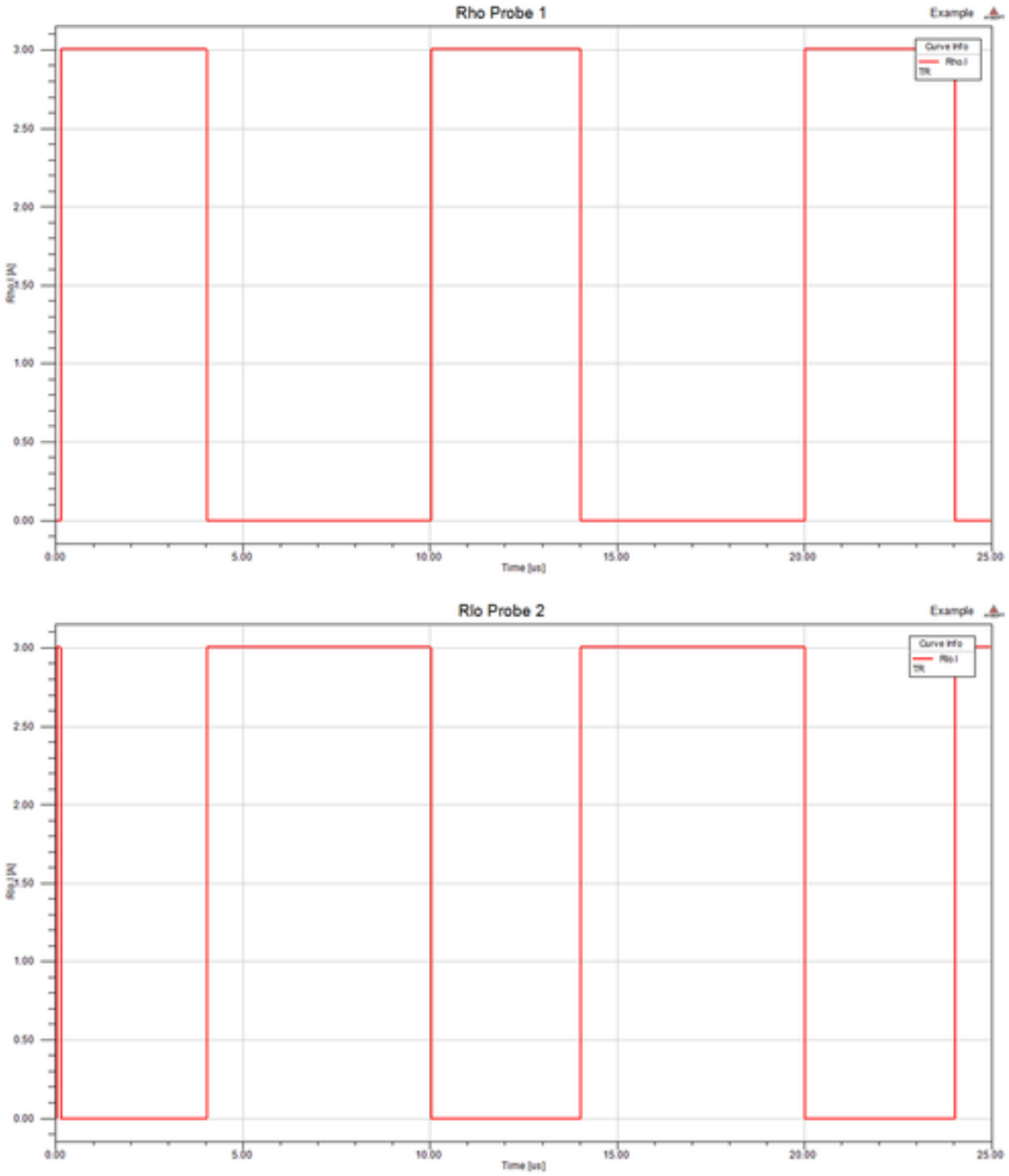

Figure 3. Simulation results

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References

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LM5105: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

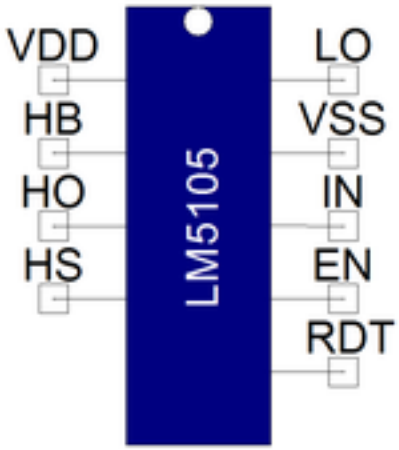

Figure 1. Component symbol

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Description

The *LM5105* is a high voltage gate driver designed to drive both the high side and low side N-Channel MOSFETs in a synchronous buck or half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 100V. The single control input is compatible with TTL signal levels and a single external resistor programs the switching transition dead-time through tightly matched turn-on delay circuits. A high voltage diode is provided to charge the high side gate drive bootstrap capacitor. The robust level shift technology operates at high speed while consuming low power and provides clean output transitions. Under-voltage lockout disables the gate driver when either the low side or the bootstrapped high side supply voltage is

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below the operating threshold. The *LM5105* is offered in the thermally enhanced10-pin LLP plastic package.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	NC	Not Connected
6	RDT	Dead-time programming pin
7	EN	Logic input for driver Disable/Enable
8	IN	Logic input for gate driver
9	VSS	Ground return
10	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Currents						
VDD Quiescent Current	LI = HI = 0V		0.34	0.6	0.4	mA
VDD Operating Current	f = 500 kHz		2.1	3.5		mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2		mA
Total HB Operating Current	f = 500 kHz		1.3	3		mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.05	10		uA
HB to VSS Current, Operating	f = 500 kHz		0.08			mA
Input Pins						
Low Level Input Voltage Threshold	Rising Edge	0.8	1.8		1.8	V
High Level Input Voltage Threshold			1.8	2.2	1.8	mV
Input Pull-down Resistance		100	200	500	200	kohm
Dead-Time Controls						
Nominal Voltage at RT		2.7	3	3.3	3	V
RT Pin Current Limit		0.75	1.5	2.25	1.5	mA
Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB			0.4		0.4	V

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Bootstrap Diode						
Low-Current Forward Voltage	IVDD-HB = 100 µA		0.60	0.9	.0.6	V
High-Current Forward Voltage	IVDD-HB = 100 mA		0.85	1.1	0.85	V
Dynamic Resistance	IVDD-HB = 100 mA		0.8	1.5		ohm

Table 3

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
LO Gate Driver						
Low-Level Output Voltage	ILO = 100 mA		0.25	0.4	0.25	V
High-Level Output Voltage	ILO = -100 mA, VOHL = VDD - VLO		0.35	0.85	0.35	V
Peak Pullup Current	VHO = 0V		1.8		1.8	A
Peak Pull-down Current	VHO = 12V		1.6		1.6	A
HO Gate Driver						
Low-Level Output Voltage	IHO = 100 mA		0.25	0.4	0.25	V
High-Level Output Voltage	IHO = -100 mA, VOHH = VHB - VHO		0.35	0.85	0.35	V
Peak Pullup Current	VHO = 0V		1.8		1.8	A
Peak Pull-down Current	VHO = 12V		1.6		1.6	A
Switching Char-						

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Lower Turn-Off Propagation Delay			26	56	25	ns
Upper Turn-Off Propagation Delay			26	56	25	ns
Lower Turn-On Propagation Delay		485	595	705	595	ns
Upper Turn-On Propagation Delay		485	595	705	595	ns
Lower Turn-On Propagation Delay		75	105	150	105	ns
Upper Turn-On Propagation Delay		75	105	150	105	ns
Enable and Shutdown propagation delay			28		28	ns
Dead-Time LO OFF to HO ON & HO OFF to LO ON	RDT = 100k		570		570	ns
	RDT = 10k		80		80	ns
Dead-Time Matching	RDT = 100k		50		0	ns
Either Output Rise/Fall Time	CL = 1000 pF		15		8	ns
Bootstrap Diode Turn-Off Time	IF = 20 mA IR = 200 mA		50			ns

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Examples

Example circuit :

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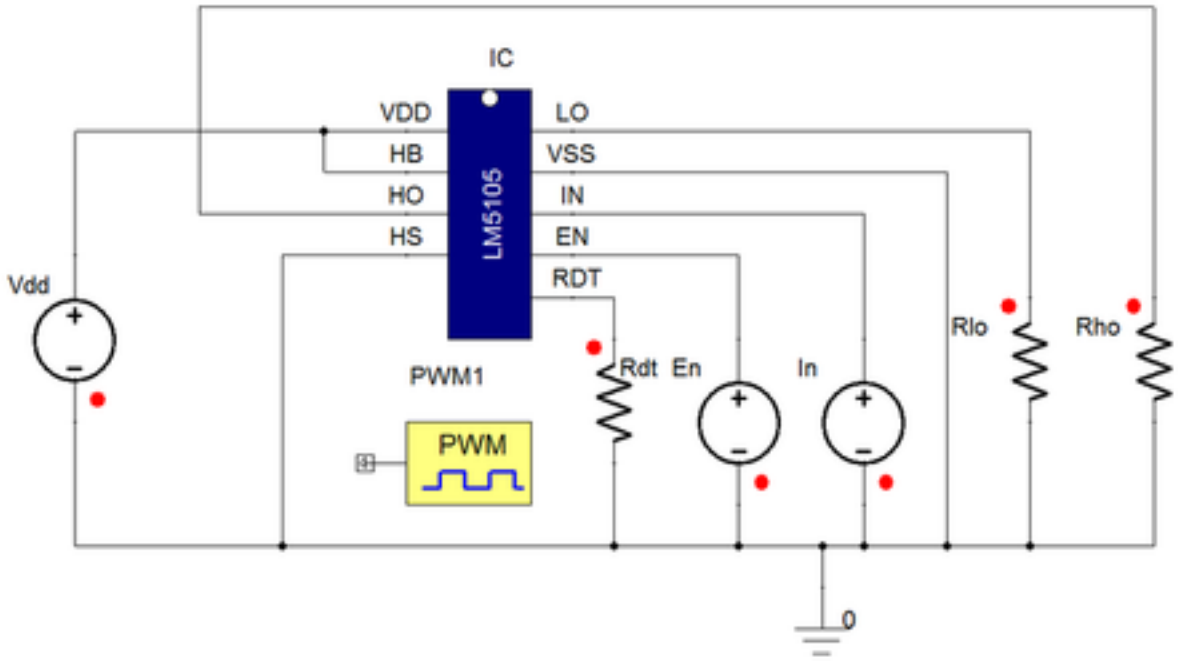
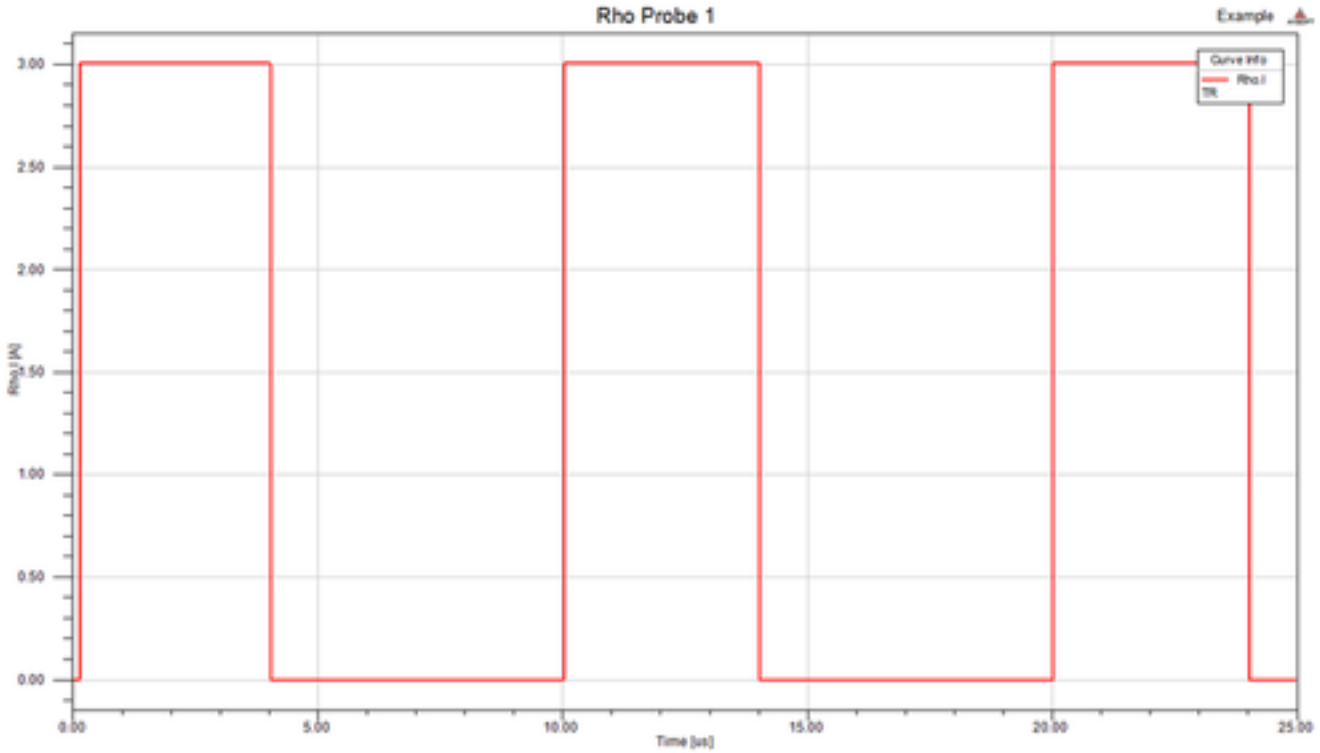


Figure 2. Example Circuit

Simulation results :



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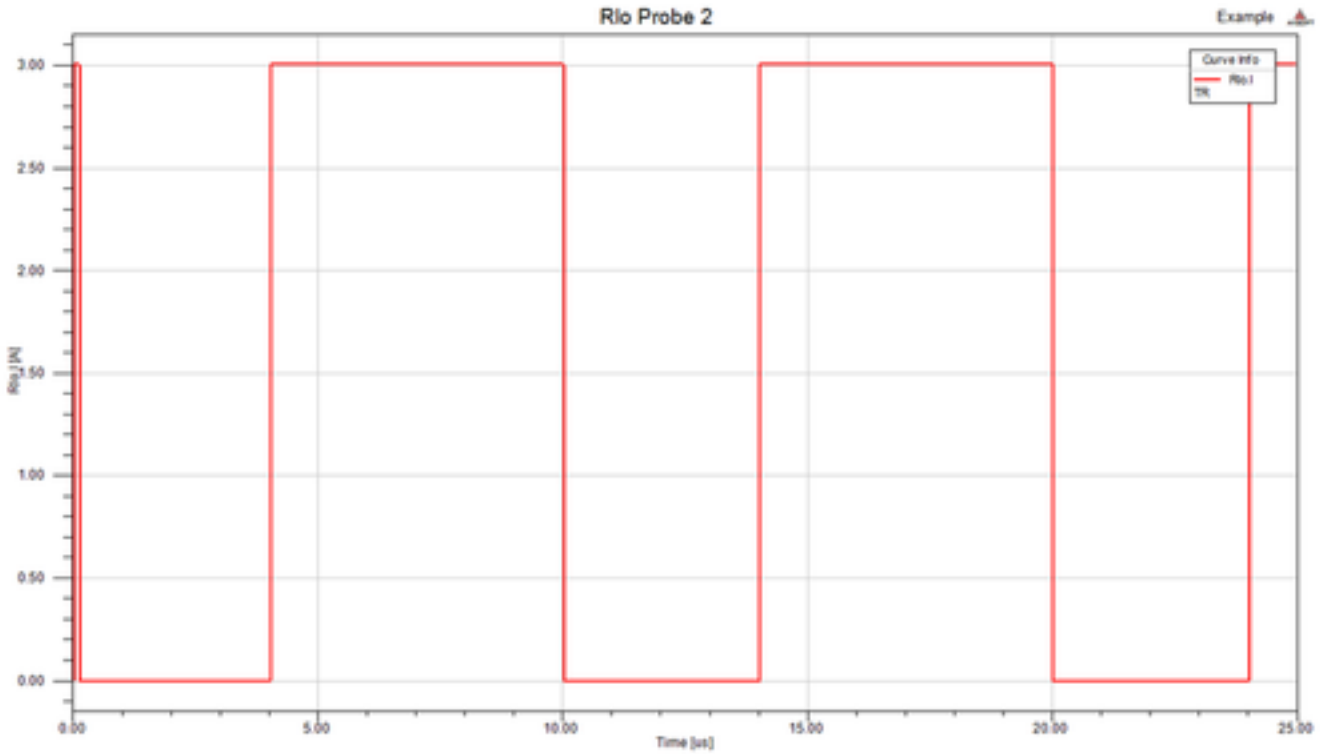

Figure 3. Simulation results

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References

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LM5106: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

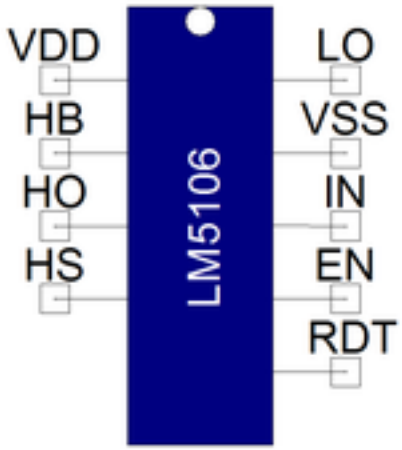

Figure 1. Component symbol

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Description

The *LM5106* is a high voltage gate driver designed to drive both the high side and low side N-Channel MOSFETs in a synchronous buck or half bridge configuration. The floating high side driver is capable of working with rail voltages up to 100V. The single control input is compatible with TTL signal levels and a single external resistor programs the switching transition dead-time through tightly matched turn-on delay circuits. The robust level shift technology operates at high speed while consuming low power and provides clean output transitions. Under-voltage lockout disables the gate driver when either the low side or the bootstrapped high side supply voltage is

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below the operating threshold. The *LM5106* is offered in the MSOP-10 or thermally enhanced 10-pin LLP plastic package.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	NC	Not Connected
6	RDT	Dead-time programming pin
7	EN	Logic input for driver Disable/Enable
8	IN	Logic input for gate driver
9	VSS	Ground return
10	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Currents						
VDD Quiescent Current	LI = HI = 0V		0.34	0.6	0.34	mA
VDD Operating Current	f = 500 kHz		2.1	3.5		mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2		mA
Total HB Operating Current	f = 500 kHz		1.3	3		mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.05	10		uA
HB to VSS Current, Operating	f = 500 kHz		0.08			mA
Input Pins						
Low Level Input Voltage Threshold	Rising Edge	0.8	1.8		1.8	V
High Level Input Voltage Threshold			1.8	2.2	1.8	mV
Input Pull-down Resistance		100	200	500	200	kohm
Dead-Time Controls						
Nominal Voltage at RT		2.7	3	3.3	3	V
RT Pin Current Limit		0.75	1.5	2.25	1.5	mA
Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB			0.4		0.4	V

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Threshold Hysteresis						

Table 3

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
LO Gate Driver						
Low-Level Output Voltage	ILO = 100 mA		0.21	0.4	0.21	V
High-Level Output Voltage	ILO = -100 mA, VOHL = VDD - VLO		0.5	0.85	0.5	V
Peak Pullup Current	VHO = 0V		1.2		1.2	A
Peak Pull-down Current	VHO = 12V		1.8		1.8	A
HO Gate Driver						
Low-Level Output Voltage	IHO = 100 mA		0.21	0.4	0.21	V
High-Level Output Voltage	IHO = -100 mA, VOHH = VHB - VHO		0.5	0.85	0.5	V
Peak Pullup Current	VHO = 0V		1.2		1.2	A
Peak Pull-down Current	VHO = 12V		1.8		1.8	A
Switching Characteristics						
Lower Turn-Off Propagation Delay			32	56	32	ns
Upper Turn-Off Propagation Delay			32	56	32	ns
Lower Turn-On Propagation Delay		400	520	640	542	ns

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Upper Turn-On Propagation Delay		450	570	690	542	ns
Lower Turn-On Propagation Delay		85	115	160	118	ns
Upper Turn-On Propagation Delay		85	115	160	118	ns
Enable and Shutdown propagation delay			36		36	ns
Dead-Time LO OFF to HO ON & HO OFF to LO ON	RDT = 100k		510		510	ns
	RDT = 10k		86		86	ns
Dead-Time Matching	RDT = 100k		50		0	ns
Either Output Rise Time	CL = 1000 pF		15		11.5	ns
Either Output Fall Time	CL = 1000 pF		10		4.8	ns

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Examples

Example circuit :

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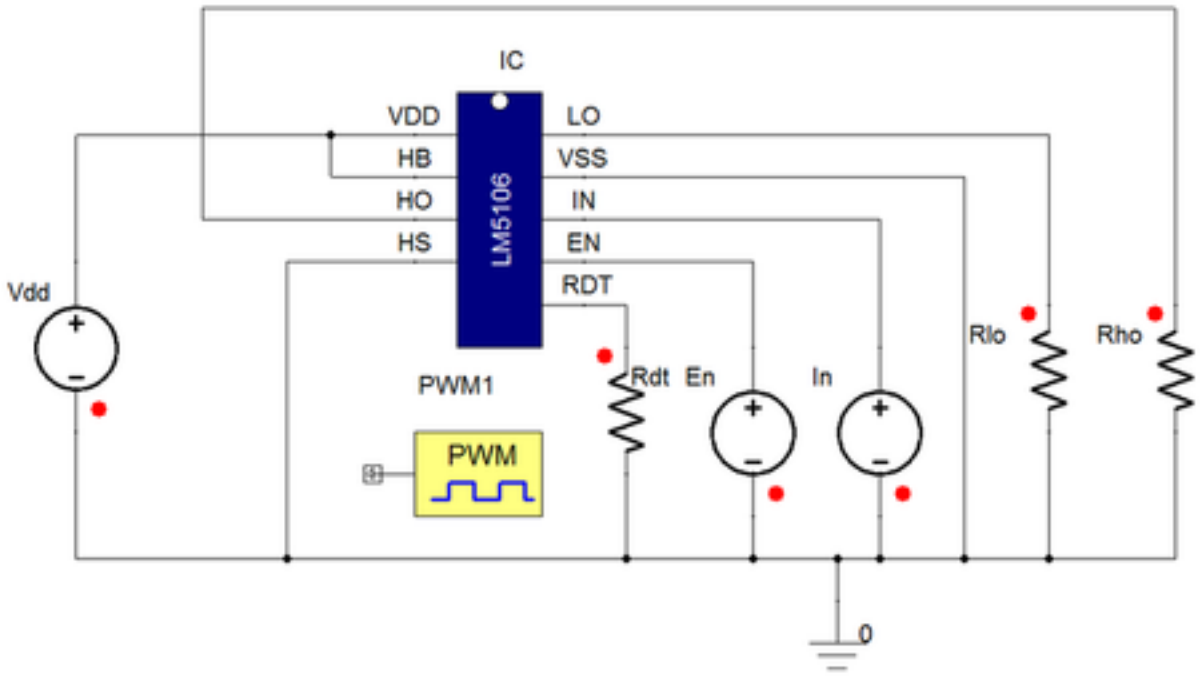
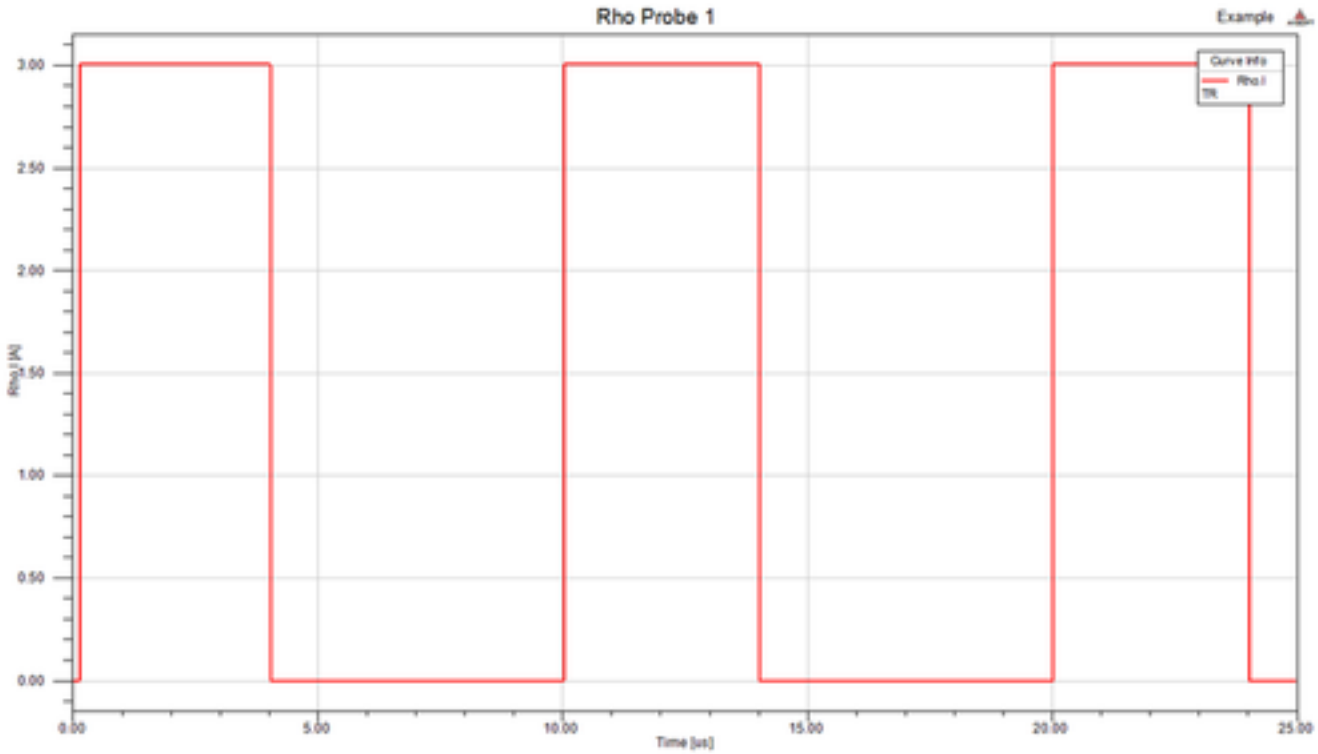


Figure 2. Example Circuit

Simulation results :



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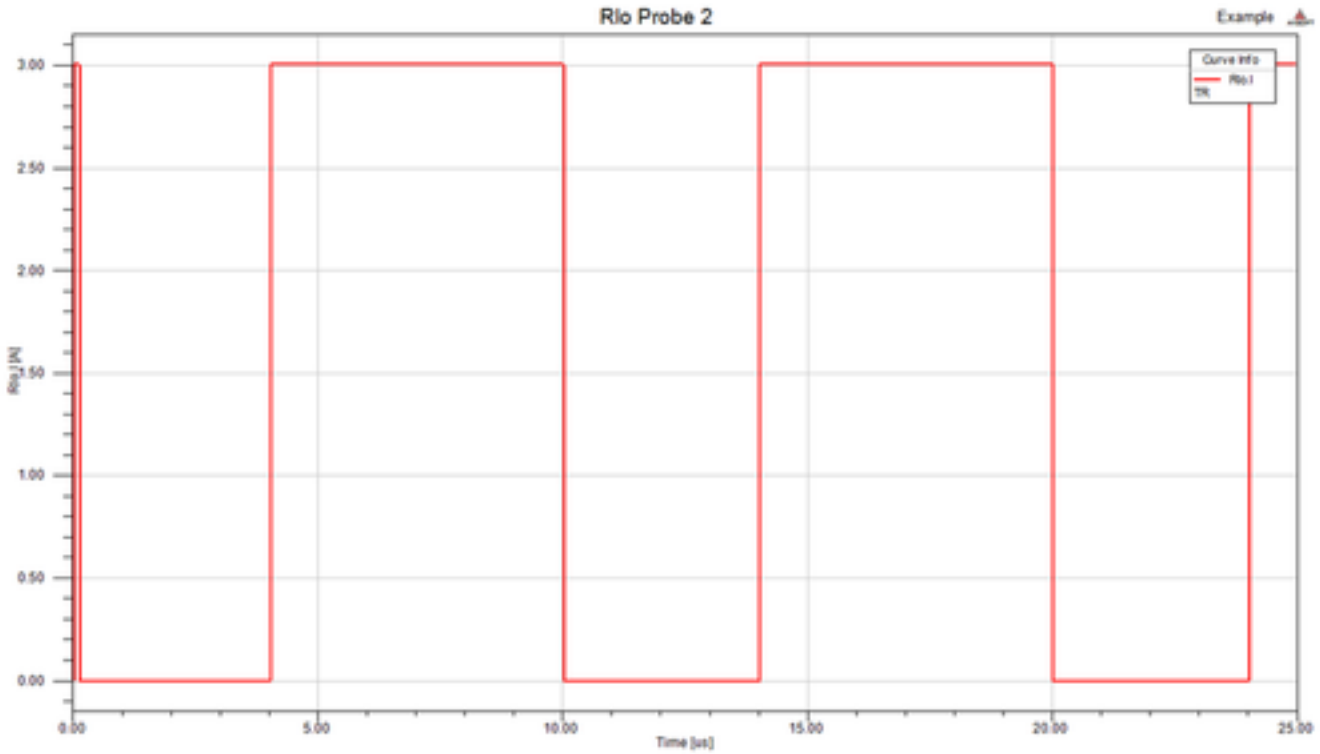

Figure 3. Simulation results

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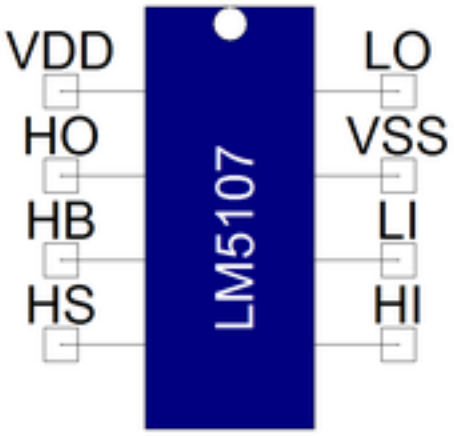
LM5107: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM5107* is a low cost high voltage gate driver, designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 100V. The outputs are independently controlled with TTL compatible input thresholds. An integrated on chip high voltage diode is provided to charge the high side gate drive bootstrap capacitor. A robust level shifter technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high side gate driver. Under-voltage lockout is provided

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on both the low side and the high side power rails. The device is available in the SOIC-8 and the thermally enhanced LLP-8 packages.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Currents						
VDD Quiescent Current	LI = HI = 0V		0.3	0.6	0.3	mA
VDD Operating Current	f = 500 kHz		2.1	3.4		mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2		mA
Total HB Operating Current	f = 500 kHz		1.6	3		mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.1	10		uA
HB to VSS Current, Operating	f = 500 kHz		0.5			mA
Input Pins						
Low Level Input Voltage Threshold	Rising Edge	0.8	1.8		1.8	V
High Level Input Voltage Threshold			1.8	2.2	1.8	mV
Input Pull-down Resistance		100	200	500	200	kohm
Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current Forward	IVDD-HB = 100 µA		0.60	0.9	.0.6	V

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Voltage						
High-Current Forward Voltage	IVDD-HB = 100 mA		0.85	1.1	0.85	V
Dynamic Resistance	IVDD-HB = 100 mA		1.0	1.65		ohm

Table 3

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
LO Gate Driver						
Low-Level Output Voltage	ILO = 100 mA		0.28	0.45	0.28	V
High-Level Output Voltage	ILO = -100 mA, VOHL = VDD - VLO		0.45	0.75	0.45	V
Peak Pullup Current	VHO = 0V		1.3		1.3	A
Peak Pull-down Current	VHO = 12V		1.4		1.4	A
HO Gate Driver						
Low-Level Output Voltage	IHO = 100 mA		0.28	0.45	0.28	V
High-Level Output Voltage	IHO = -100 mA, VOHH = VHB - VHO		0.45	0.75	0.45	V
Peak Pullup Current	VHO = 0V		1.3		1.3	A
Peak Pull-down Current	VHO = 12V		1.4		1.4	A
Switching						

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Char-acteristics						
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			27	56	27	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			27	56	27	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)			29	56	29	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)			29	56	29	ns
Delay Matching: Lower Turn-On and Upper Turn-Off			2	15	2	ns
Delay Matching: Lower Turn-Off and Upper Turn-On			2	15	2	ns
Either Output Rise/Fall Time	CL = 1000 pF		15		6.4	ns
Either Output Rise/Fall Time (3V to 9V)	CL = 0.1 µF		50		494	ns
Bootstrap Diode Turn-Off Time	IF = 20 mA IR = 200 mA		105			ns

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Examples

Example circuit :

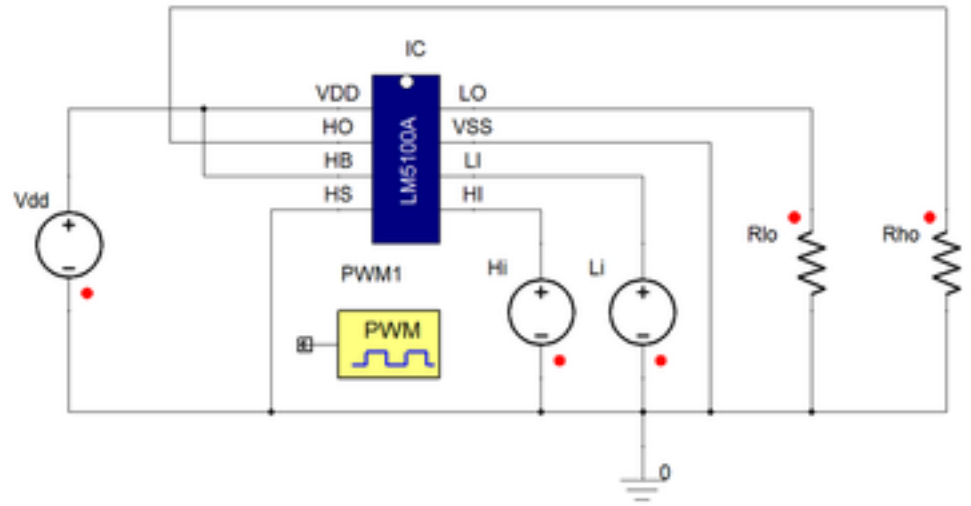
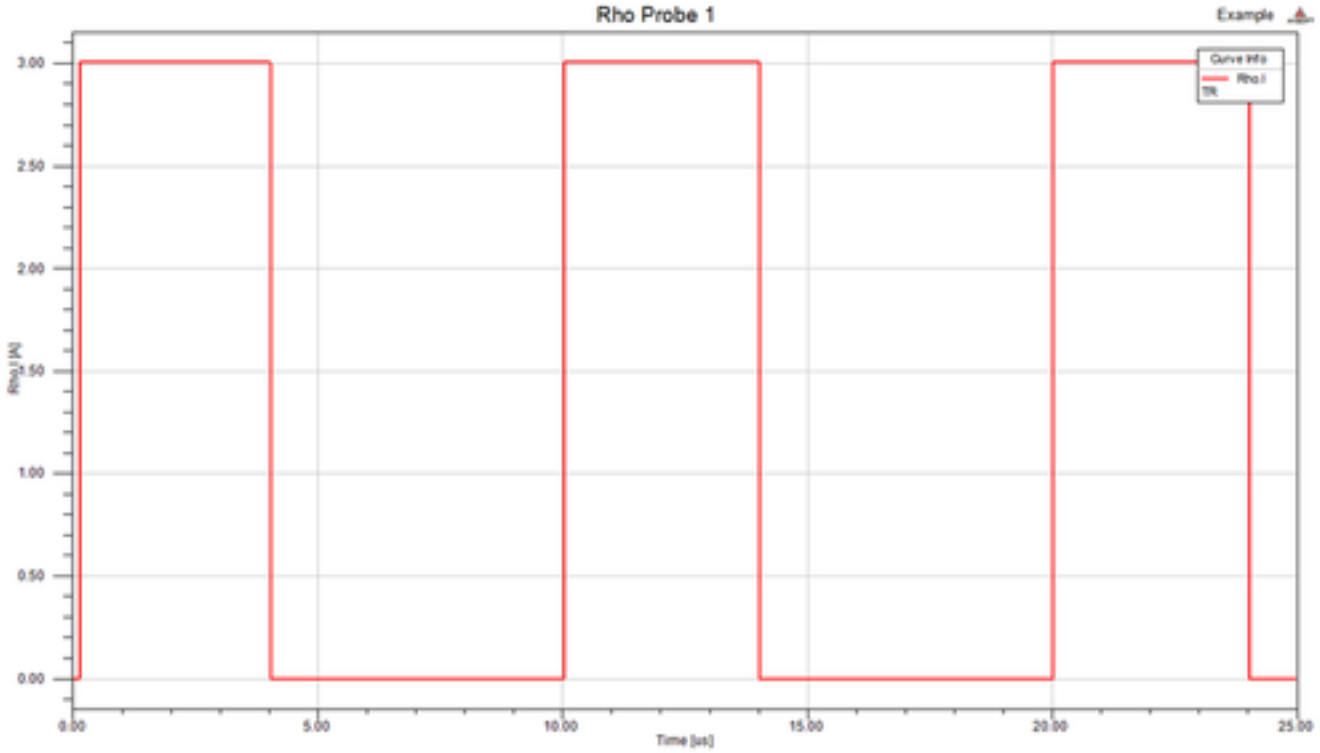


Figure 2. Example Circuit

Simulation results :



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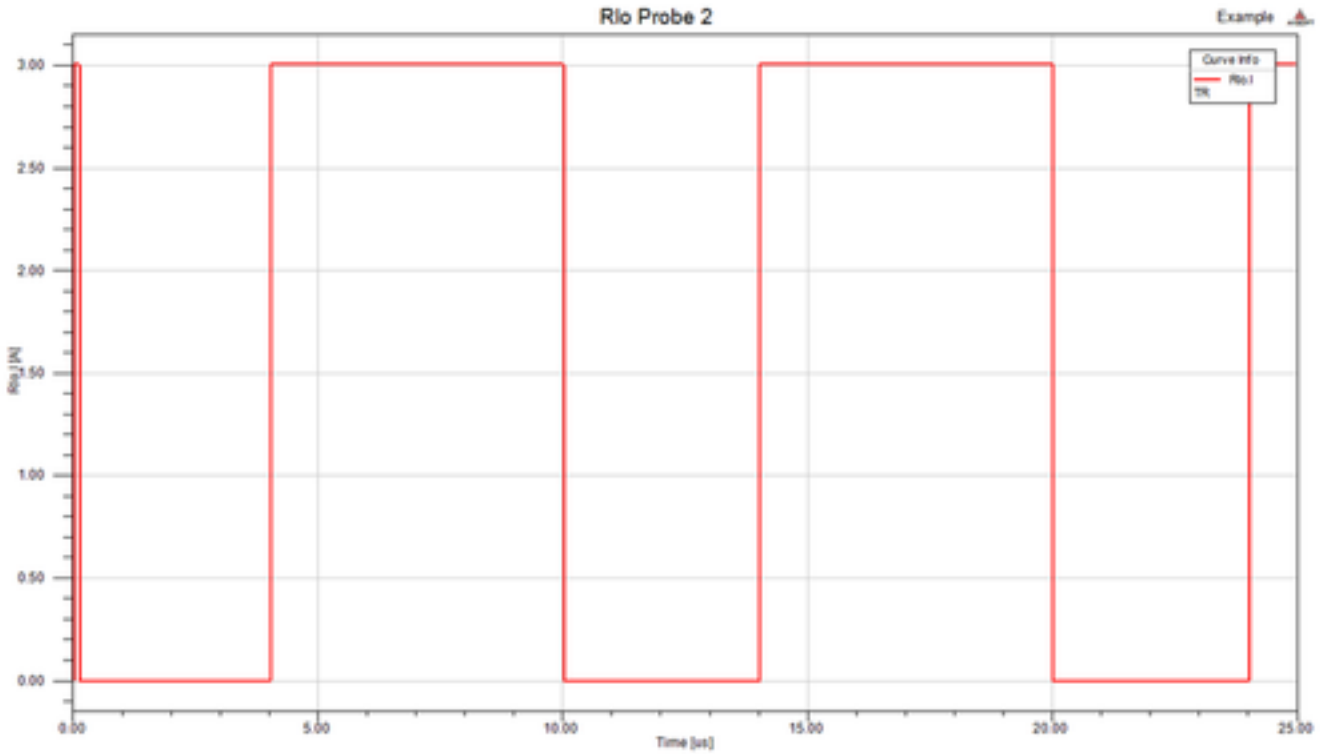

Figure 3. Simulation results

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References

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LM5109A: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

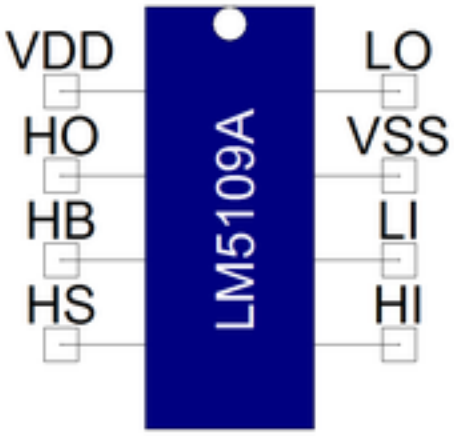

Figure 1. Component symbol

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Description

The *LM5109A* is a cost effective, high voltage gate driver designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 90V. The outputs are independently controlled with TTL compatible input thresholds. The robust level shift technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high-side gate driver. Under-voltage lockout is provided on both the lowside and the high-side power rails. The device is available in the SOIC-8 and the thermally enhanced LLP-8 packages.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Currents						
VDD Quiescent Current	LI = HI = 0V		0.3	0.6	0.3	mA
VDD Operating Current	f = 500 kHz		1.8	2.9	-	mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2	-	mA
Total HB Operating Current	f = 500 kHz		1.4	2.8	-	mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.1	10	-	uA
HB to VSS Current, Operating	f = 500 kHz		0.5		-	mA
Input Pins						
Low Level Input Voltage Threshold	Rising Edge	0.8	1.8		1.8	V
High Level Input Voltage Threshold			1.8	2.2	1.8	mV
Input Pull-down Resistance		100	200	500	200	kohm
Under Voltage Protection						
VDD Rising Threshold		6.0	6.7	7.4	6.7	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V

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Table 3

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
LO Gate Driver						
Low-Level Output Voltage	ILO = 100 mA		0.28	0.45	0.28	V
High-Level Output Voltage	ILO = -100 mA, VOHL = VDD - VLO		0.45	0.75	0.45	V
Peak Pullup Current	VHO = 0V		1.3		1.3	A
Peak Pull-down Current	VHO = 12V		1.4		1.4	A
HO Gate Driver						
Low-Level Output Voltage	IHO = 100 mA		0.28	0.45	0.28	V
High-Level Output Voltage	IHO = -100 mA, VOHH = VHB - VHO		0.45	0.75	0.45	V
Peak Pullup Current	VHO = 0V		1.3		1.3	A
Peak Pull-down Current	VHO = 12V		1.4		1.4	A
Switching Char-acteristics						
Lower Turn-Off Propaga-tion Delay (LI Falling to LO Falling)			30	56	30	ns
Upper Turn-Off Propaga-tion Delay (HI Falling to HO Falling)			30	56	30	ns
Lower Turn-On Propaga-tion Delay			32	56	32	ns

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(LI Rising to LO Rising)						
Upper Turn-On Propagation Delay (HI Rising to HO Rising)			32	56	32	ns
Delay Matching: Lower Turn-On and Upper Turn-Off			2	15	2	ns
Delay Matching: Lower Turn-Off and Upper Turn-On			2	15	2	ns
Either Output Rise/Fall Time	CL = 1000 pF		15		6.4	ns
Either Output Rise/Fall Time (3V to 9V)	CL = 0.1 µF		50		494	ns

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Example circuit :

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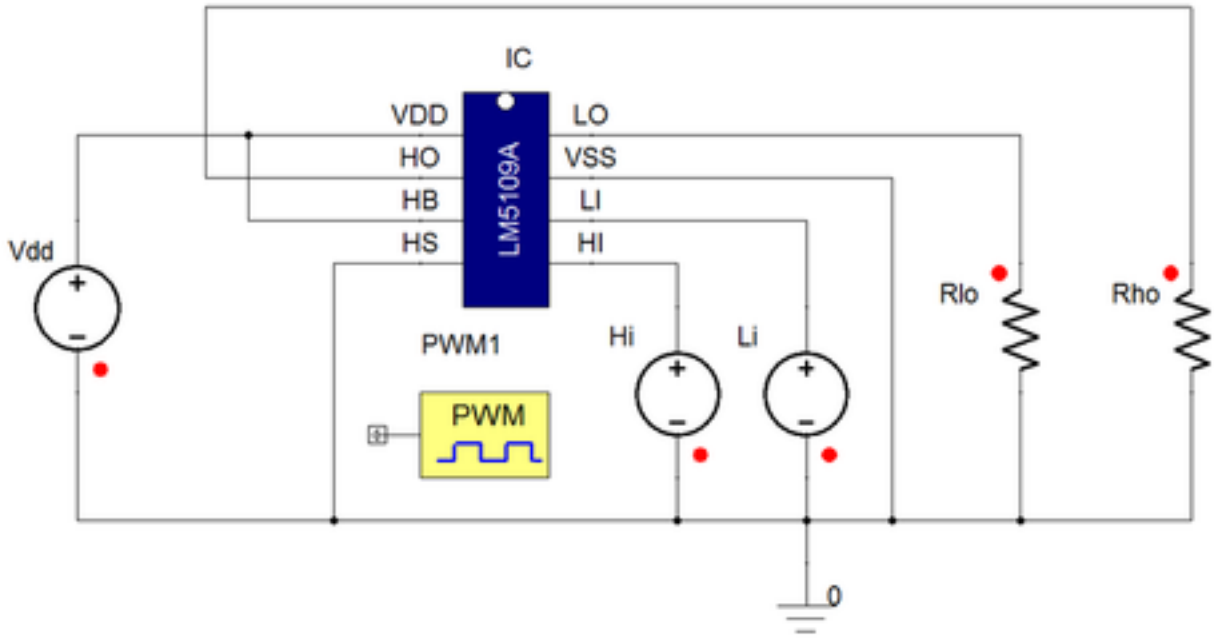
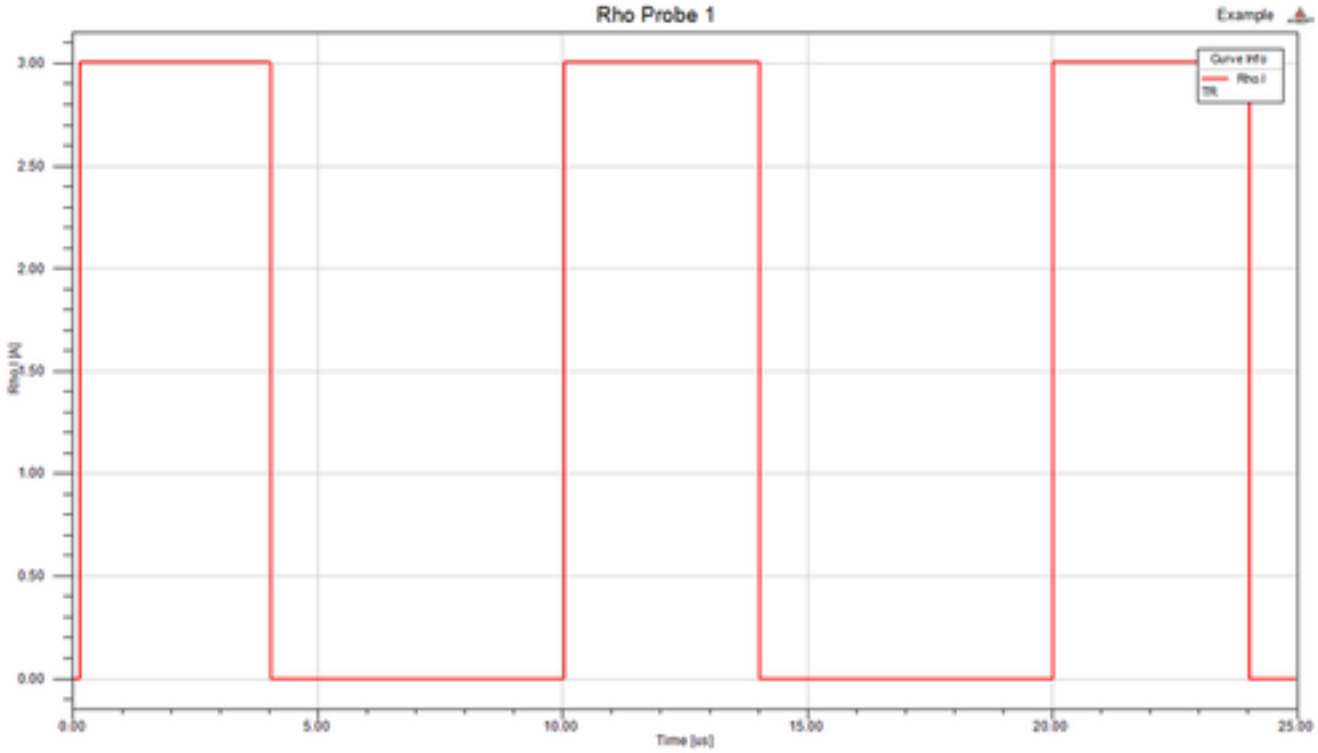


Figure 2. Example Circuit

Simulation results :



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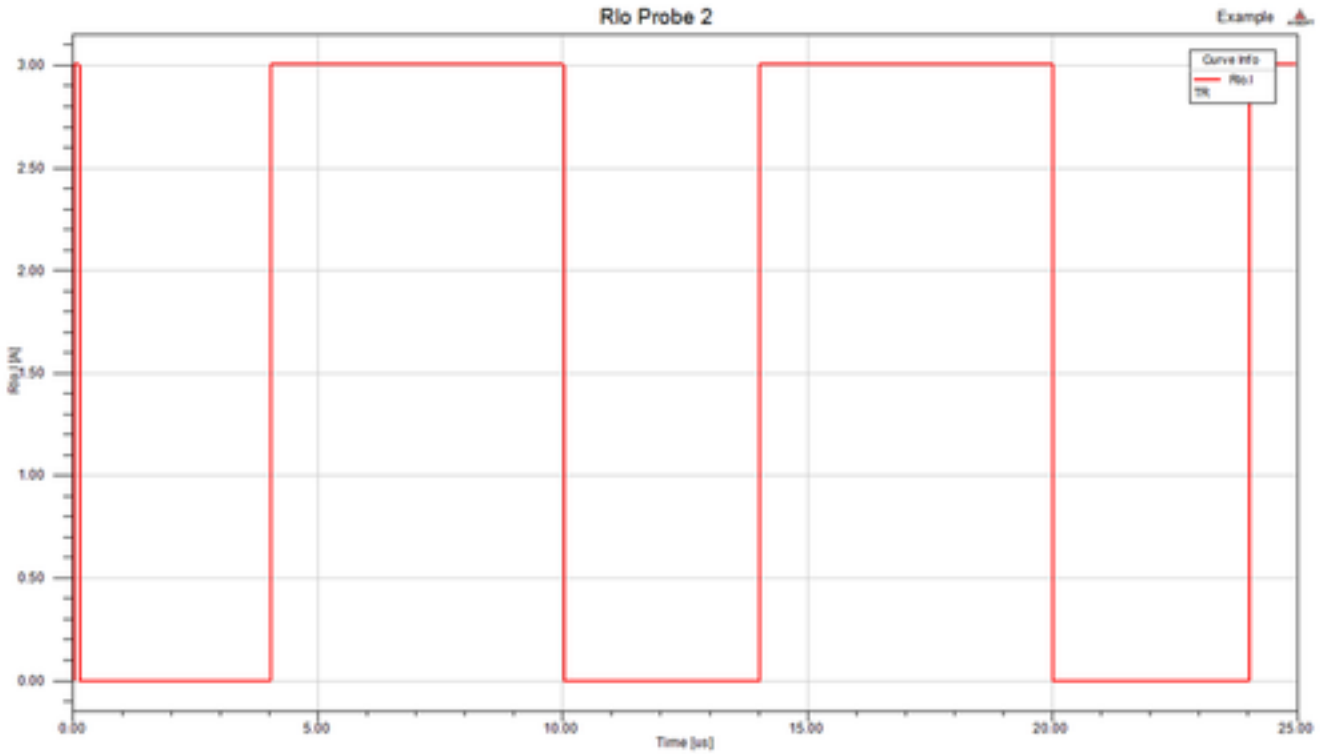

Figure 3. Simulation results

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References

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LM5109B: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

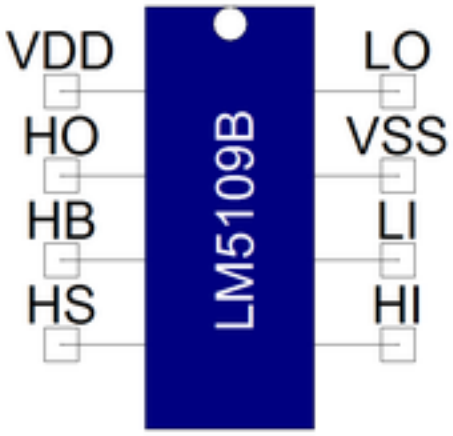

Figure 1. Component symbol

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Description

The *LM5109B* is a cost effective, high voltage gate driver designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 90V. The outputs are independently controlled with TTL compatible input thresholds. The robust level shift technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails. The device is available in the SOIC-8 and the thermally enhanced LLP-8 packages.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HO	High-side gate driver output
4	HS	High-side MOSFET source connection
5	HI	High-side driver control input
6	LI	Low-side driver control input
7	VSS	Ground return
8	LO	Low-side gate driver output

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Currents						
VDD Quiescent Current	LI = HI = 0V		0.3	0.6	0.3	mA
VDD Operating Current	f = 500 kHz		1.8	2.9	-	mA
Total HB Quiescent Current	LI = HI = 0V		0.06	0.2	-	mA
Total HB Operating Current	f = 500 kHz		1.4	2.8	-	mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.1	10	-	uA
HB to VSS Current, Operating	f = 500 kHz		0.5		-	mA
Input Pins						
Low Level Input Voltage Threshold	Rising Edge	0.8	1.8		1.8	V
High Level Input Voltage Threshold			1.8	2.2	1.8	mV
Input Pull-down Resistance		100	200	500	200	kohm
Under Voltage Protection						
VDD Rising Threshold		6.0	6.7	7.4	6.7	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V

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Table 3

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
LO Gate Driver						
Low-Level Output Voltage	ILO = 100 mA		0.38	0.65	0.38	V
High-Level Output Voltage	ILO = -100 mA, VOHL = VDD - VLO		0.72	1.2	0.72	V
Peak Pullup Current	VHO = 0V		1.0		1.0	A
Peak Pull-down Current	VHO = 12V		1.0		1.0	A
HO Gate Driver						
Low-Level Output Voltage	IHO = 100 mA		0.38	0.65	0.38	V
High-Level Output Voltage	IHO = -100 mA, VOHH = VHB - VHO		0.72	1.2	0.72	V
Peak Pullup Current	VHO = 0V		1.0		1.0	A
Peak Pull-down Current	VHO = 12V		1.0		1.0	A
Switching Char-acteristics						
Lower Turn-Off Propaga-tion Delay (LI Falling to LO Falling)			30	56	30	ns
Upper Turn-Off Propaga-tion Delay (HI Falling to HO Falling)			30	56	30	ns
Lower Turn-On Propaga-tion Delay			32	56	32	ns

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(LI Rising to LO Rising)						
Upper Turn-On Propagation Delay (HI Rising to HO Rising)			32	56	32	ns
Delay Matching: Lower Turn-On and Upper Turn-Off			2	15	2	ns
Delay Matching: Lower Turn-Off and Upper Turn-On			2	15	2	ns
Either Output Rise/Fall Time	CL = 1000 pF		15		8.7	ns
Either Output Rise/Fall Time (3V to 9V)	CL = 0.1 µF		50		791	ns

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Example circuit :

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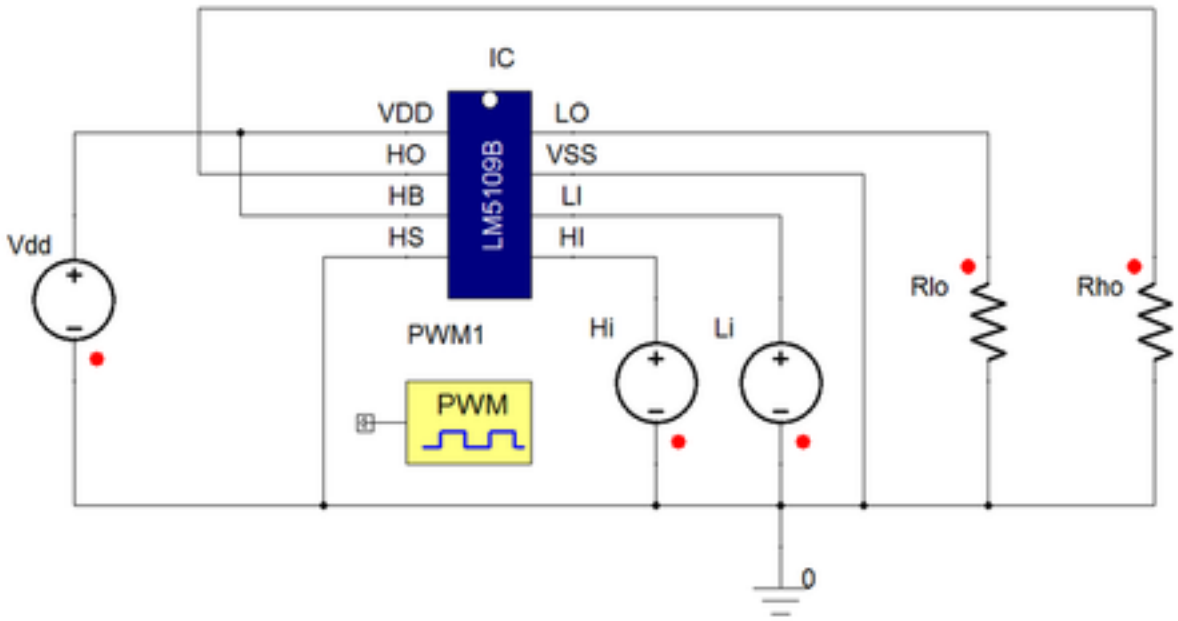
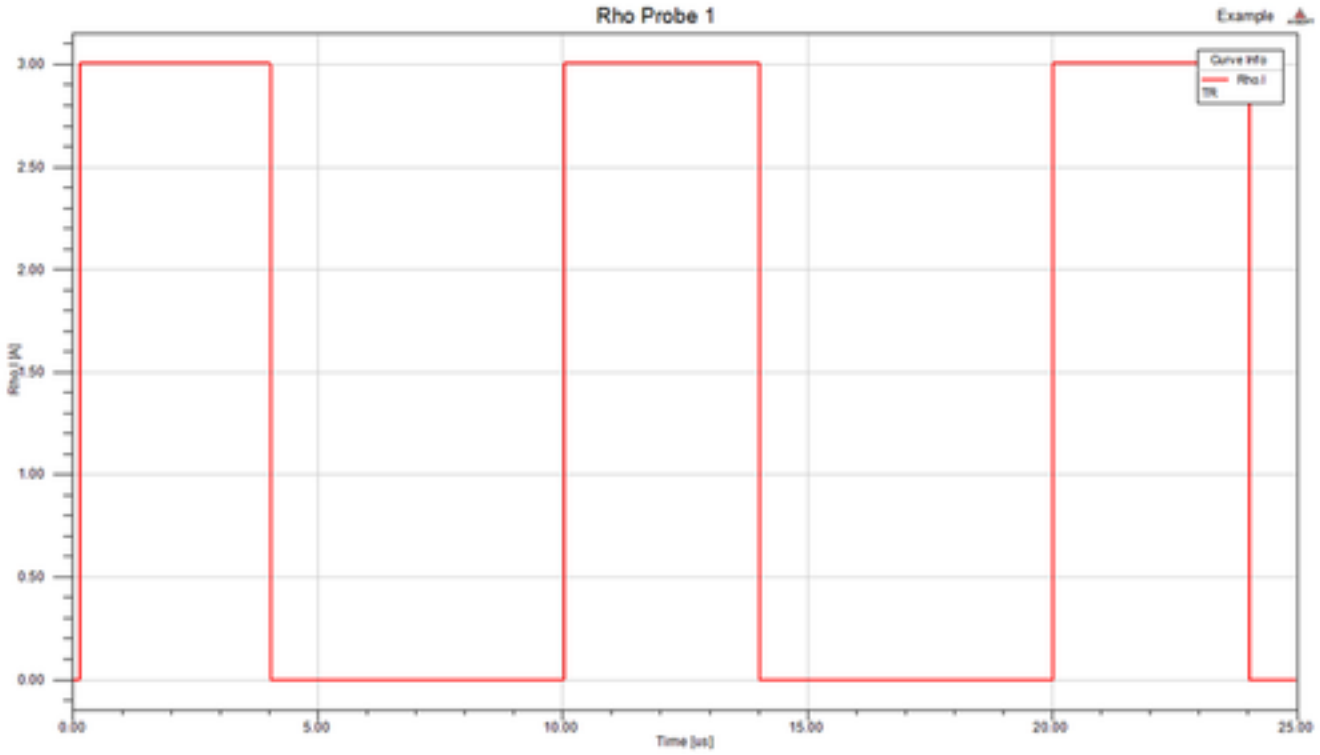


Figure 2. Example Circuit

Simulation results :



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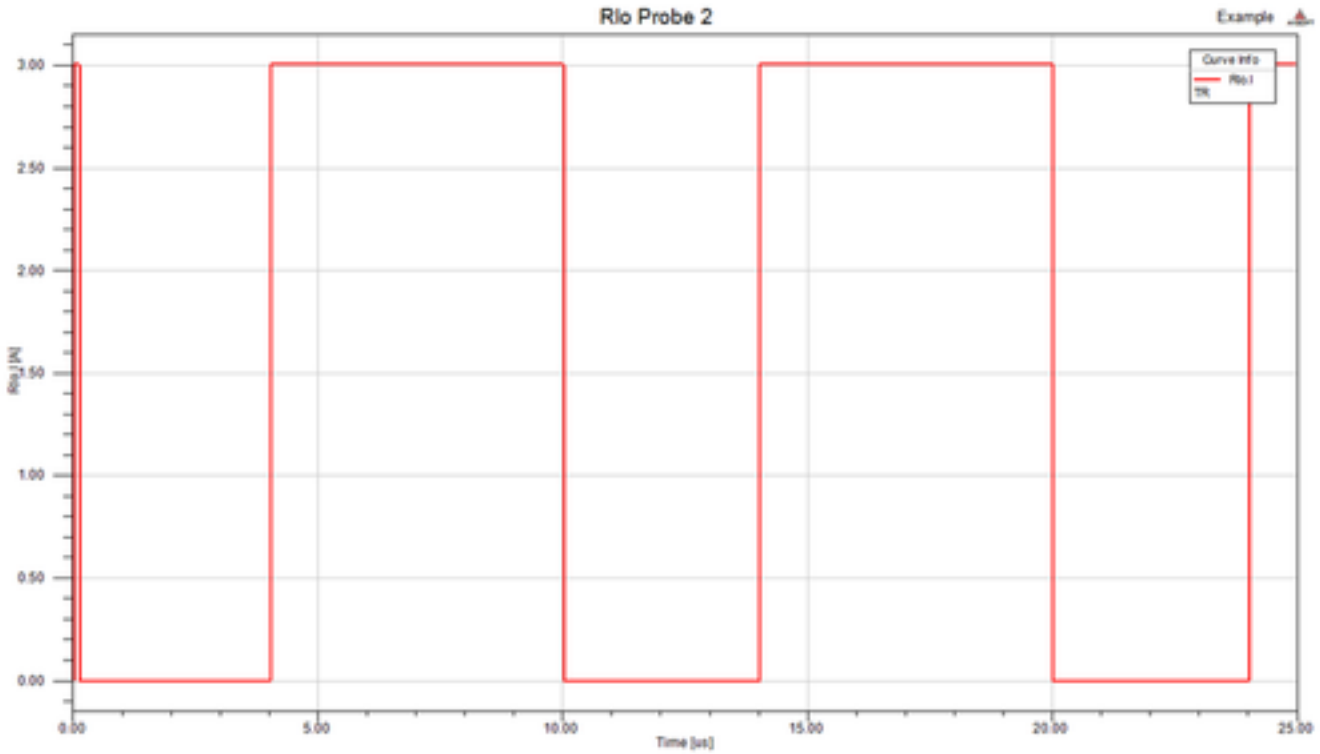

Figure 3. Simulation results

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LM5110: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

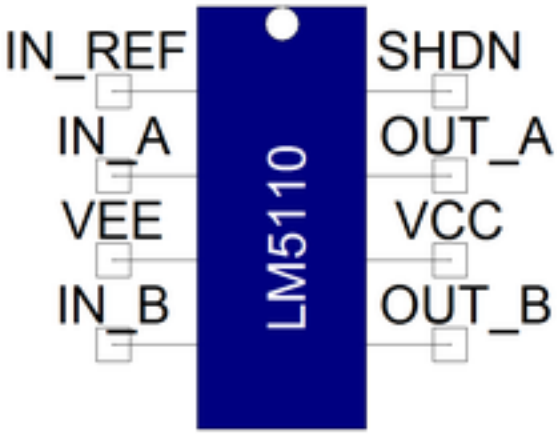

Figure 1. Component symbol

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Description

The *LM5110* Dual Gate Driver replaces industry standard gate drivers with improved peak output current and efficiency. Each "compound" output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 5A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Separate input and output ground pins provide Negative Drive Capability allowing the user to drive MOSFET gates with positive and negative VGS voltages. The gate driver control inputs are referenced to a dedicated input ground (IN_REF). The gate driver outputs swing from VCC to the output ground VEE which can be negative with

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respect to IN_REF. The ability to hold MOSFET gates off with a negative VGS voltage reduces losses when driving low threshold voltage MOSFETs often used as synchronous rectifiers. When driving with conventional positive only gate voltage, the IN_REF and VEE pins are connected together and referenced to a common ground. Under-voltage lockout protection and a shutdown input pin are also provided. The drivers can be operated in parallel with inputs and outputs connected to double the drive current capability. This device is available in the SOIC-8 and the thermally-enhanced LLP-10 packages.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	IN_REF	Ground reference for control inputs
2	INA	'A' side control input
3	Vee	Power ground of the driver outputs
4	INB	'B' side control input
5	OUTB	Output for the 'B' side driver.
6	Vcc	Positive supply
7	OUTA	Output for the 'A' side driver.
8	SD	Shutdown input pin.

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

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V_{CC} Operating Range	V_{CC}–IN_ REF and V_{CC}–V_{EE}	3.5		14	-	V
V_{CC} Under Voltage Lock-out (rising)	V_{CC}–IN_ REF	2.3	2.9	3.5	2.9	V
V_{CC} Under Voltage Lock-out Hys-teresis			230		230	mV
V_{CC} Supply Current			1	2	1	mA
V_{CC} Shutdown Current	nSHDN = 0V		18	25	18	uA
Control Input						
Logic High			1.75	2.2	1.75	V
Logic Low		0.8	1.35		1.35	V
Input Hys-teresis			400		400	mV
Input CurrentLow	IN_A=IN_ B=V_{CC}	-1	0.1	1	0.1	uA
Input Current High	IN_A=IN_ B=V_{CC}	10	18	25	0.1	uA
Shutdown Input						
Pull-up Cur-rent	nSHDN = 0 V		-18	-25	-18	uA
Shutdown Threshold	nSHDN rising	0.8	1.5	2.2	1.5	V
Shutdown Hysteresis			165		165	mV
Output Drivers						
Output Resist-ance High			30	50	30	ohm
Output Resist-anceLow			1.4	2.5	1.4	ohm
Peak SourceCur-rent			3		3	A
Peak SinkCurrent			5		5	A
Switching Characteristics						
Propagation Delay Time Low to High, IN rising	C_{LOAD} = 2 nF		25	40	25	ns

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Propagation Delay Time High to Low, IN falling	C_{LOAD} = 2 nF		25	40	25	ns
Rise Time	C_{LOAD} = 2 nF		14	25	138	ns
Fall Time	C_{LOAD} = 2 nF		12	25	6.4	ns

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Example circuit :

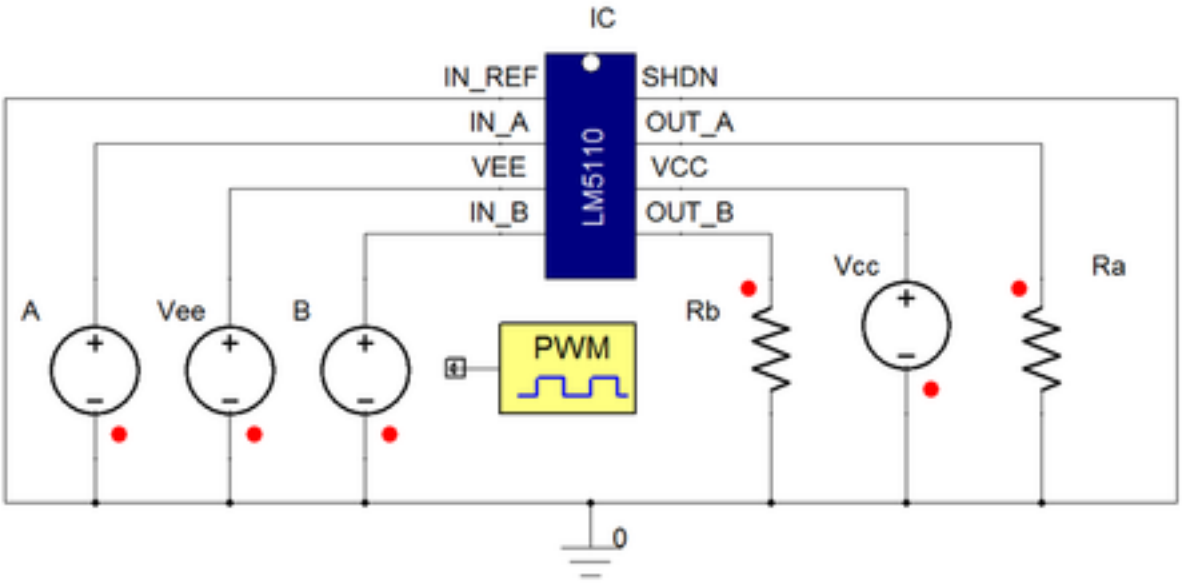

Figure 2. Example Circuit

Simulation results :

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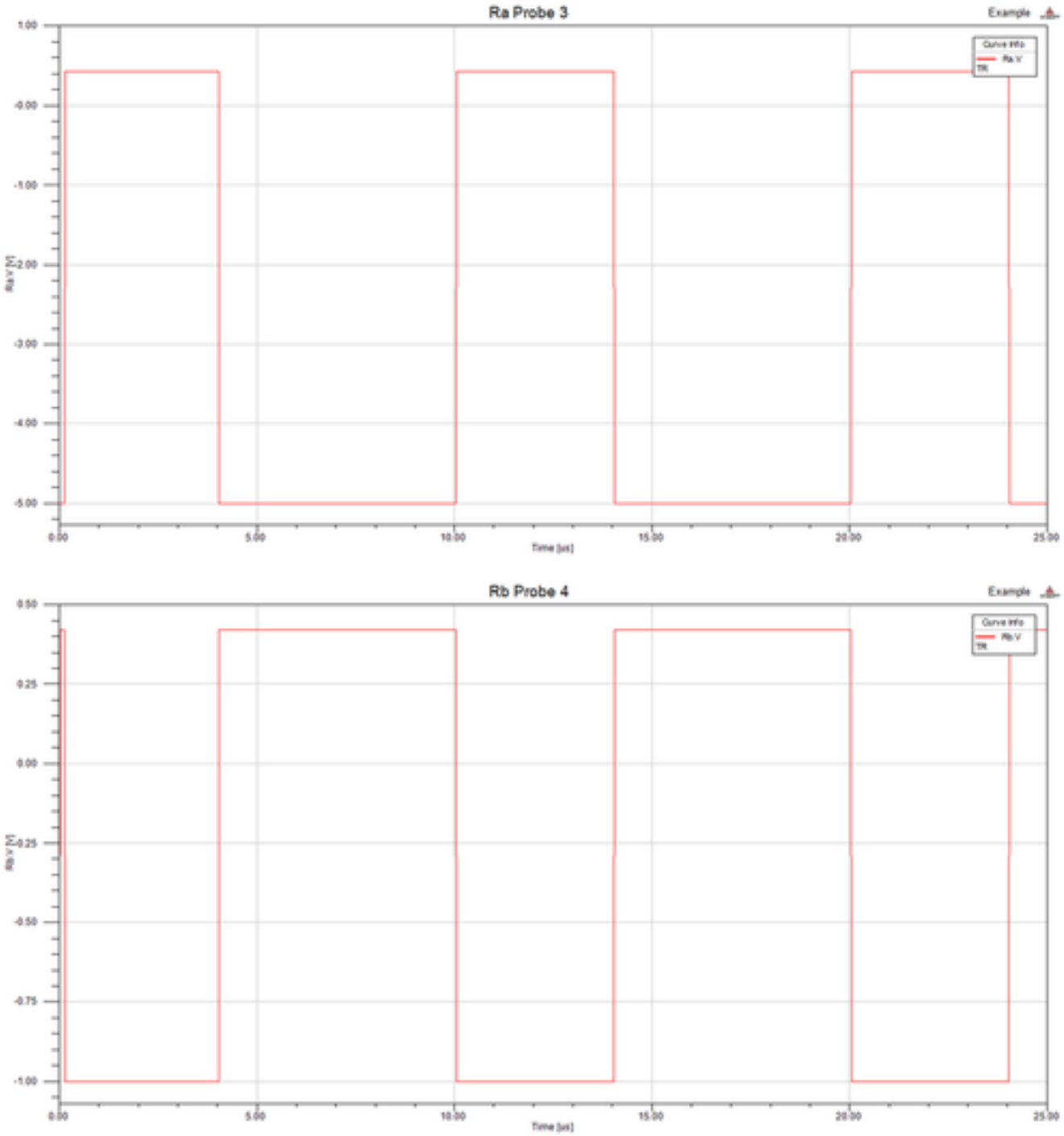

Figure 3. Simulation results

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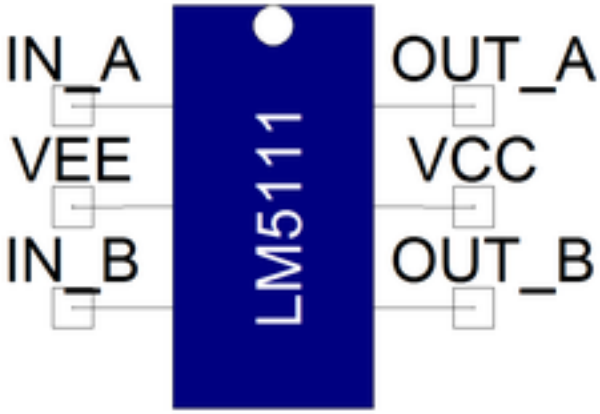
LM5111: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM5111* Dual Gate Driver replaces industry standard gate drivers with improved peak output current and efficiency. Each "compound" output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 5A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is also provided. The drivers can be operated in parallel with inputs and outputs connected to double the drive current capability. This device is available in the SOIC-8 package or the thermally enhanced MSOP8-EP package.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	INA	'A' side control input
2	VEE	Power ground of the driver outputs
3	INB	'B' side control input
4	OUTB	Output for the 'B' side driver.
5	VEE	Positive supply
6	OUTA	Output for the 'A' side driver.

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
V_{CC} Operating Range	V_{CC}–IN_REF and V_{CC}–V_{EE}	3.5		14	-	V
V_{CC} Under Voltage Lock-out (rising)	V_{CC}–IN_REF	2.3	2.9	3.5	2.9	V
V_{CC} Under Voltage Lock-out Hysteresis			230		230	mV
V_{CC} Supply			1	2	1	mA

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Current						
Control Input						
Logic High		2.2	Â	Â	1.75	V
Logic Low		Â	Â	0.8	1.35	V
Input Hysteresis			400		400	mV
Input Current Low	IN_A=IN_B=V_{CC}	-1	0.1	1	0.1	uA
Input Current High	IN_A=IN_B=V_{CC}	10	18	25	0.1	uA
Shutdown Input						
Pull-up Current	nSHDN = 0 V		-18	-25	-18	uA
Shutdown Threshold	nSHDN rising	0.8	1.5	2.2	1.5	V
Shutdown Hysteresis			165		165	mV
Output Drivers						
Output Resistance High			30	50	30	ohm
Output Resistance Low			1.4	2.5	1.4	ohm
Peak Source Current			3		3	A
Peak Sink Current			5		5	A
Switching Characteristics						
Propagation Delay Time Low to High, IN rising	C_{LOAD} = 2 nF		25	40	25	ns
Propagation Delay Time High to Low, IN falling	C_{LOAD} = 2 nF		25	40	25	ns
Rise Time	C_{LOAD} = 2 nF		14	25	138	ns
Fall Time	C_{LOAD} = 2 nF		12	25	6.4	ns

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Example circuit :

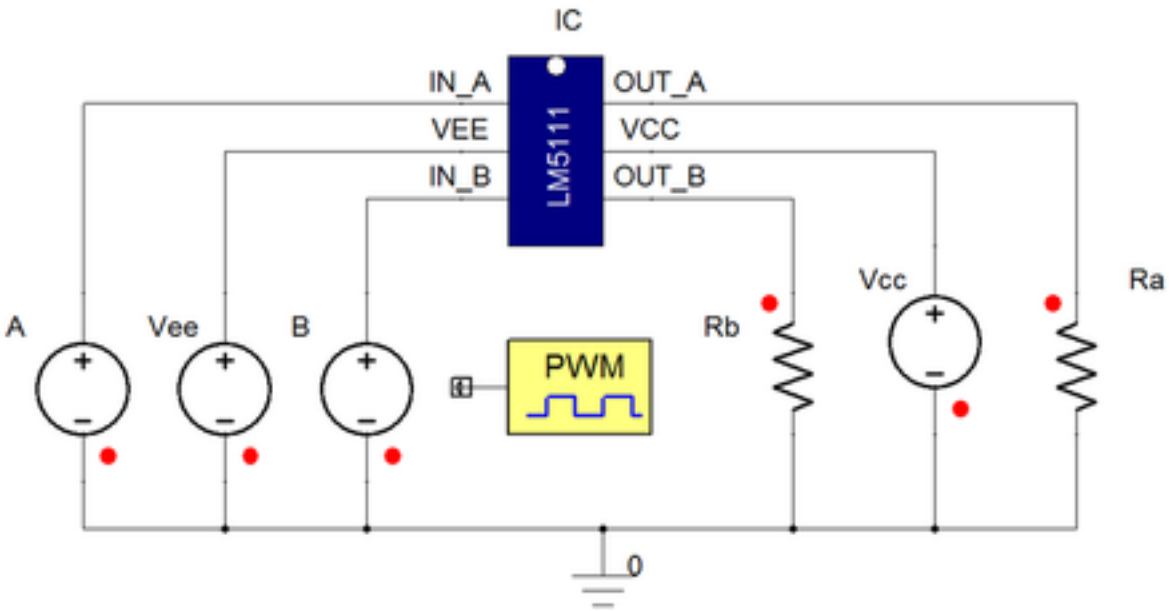

Figure 2. Example Circuit

Simulation results :

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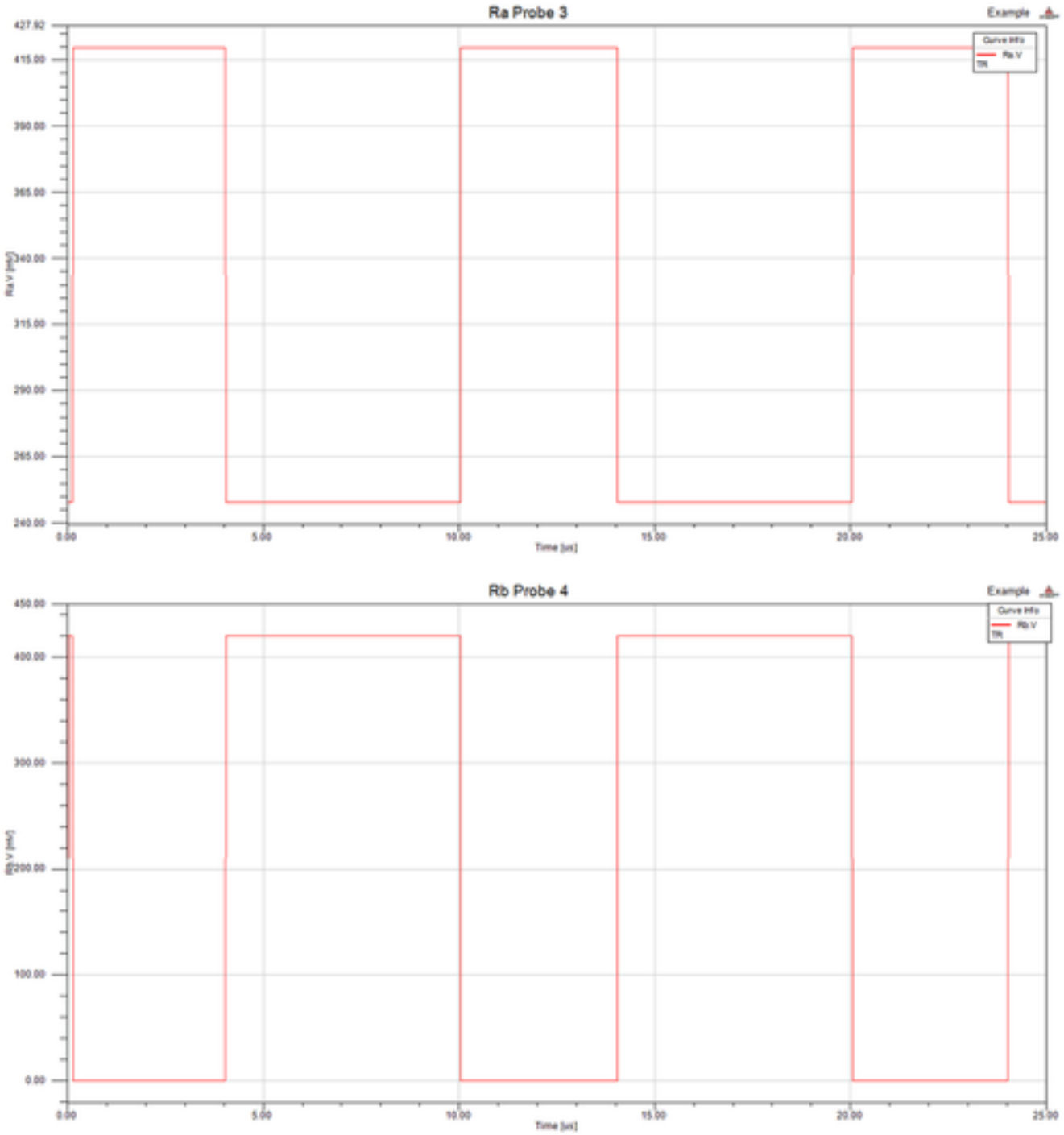

Figure 3. Simulation results

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LM5112: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

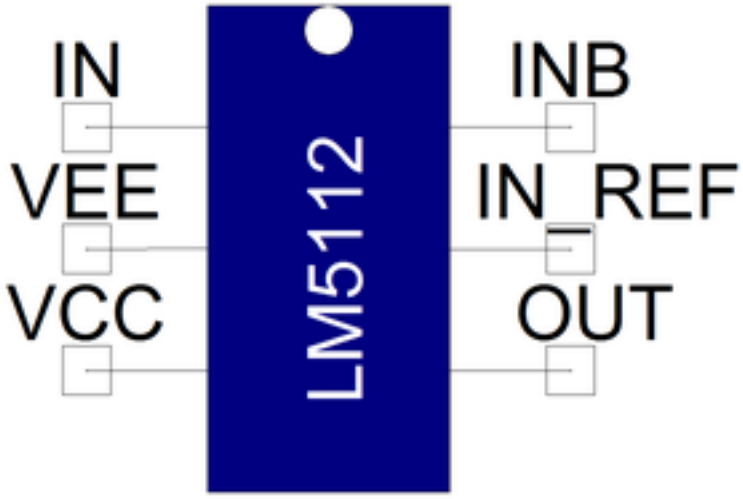

Figure 1. Component symbol

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Description

The *LM5112* MOSFET gate driver provides high peak gate drive current in the tiny LLP-6 package (SOT23 equivalent footprint) or an 8-Lead exposed-pad MSOP package, with improved power dissipation required for high frequency operation. The compound output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 7A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is provided to prevent damage to the MOSFET due to insufficient gate turn-on voltage. The

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LM5112 provides both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive with a single device type.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	IN	Non-inverting input pin
2	VEE	Power ground for driver outputs
3	VCC	Positive Supply voltage input
4	OUT	Gate drive output
5	IN_REF	Ground reference for control inputs
6	INB	Inverting input pin

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Parameters

Comparison between model and real component.

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Table 2

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
Supply						
V_{CC} Operating Range	V_{CC}–IN_ REF and V_{CC}–V_{EE}	3.5		14	12	V
V_{CC} Under Voltage Lock-out (rising)	V_{CC}–IN_ REF	2.3	2.9	3.5	2.9	V
V_{CC} Under Voltage Lock-out Hys-teresis			230		230	mV
V_{CC} Supply Current			1	2	1	mA
Control Inputs						
Logic High		2.3	Â	Â	-	V
Logic Low		Â	Â	0.8	-	V
High Threshold		1.3	1.75	2.3	1.75	
Low Threshold		0.8	1.35	2.0	1.35	
Input Hys-teresis			400		400	mV
Input Current Low	IN = INB = 0V	-1	0.1	1	0.1	uA
Input Current High	IN = INB = VCC	-1	0.1	1	0.1	uA
Shutdown Input						
Pull-up Cur-rent	nSHDN = 0 V		-18	-25	-18	uA
Shutdown Threshold	nSHDN rising	0.8	1.5	2.2	1.5	V
Shutdown Hysteresis			165		165	mV
Output Drivers						
Output Resist-ance High			30	50	30	ohm
Output Resist-ance Low			1.4	2.5	1.4	ohm
Peak Source Current			3		3	ohm
Peak Sink			7		7	ohm

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Current						
Switching Characteristics						
Propagation Delay Time Low to High, IN rising	C_{LOAD} = 2 nF		25	40	25	ns
Propagation Delay Time High to Low, IN falling	C_{LOAD} = 2 nF		25	40	25	ns
Rise Time	C_{LOAD} = 2 nF		14		138	ns
Fall Time	C_{LOAD} = 2 nF		12		6.4	ns

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Example circuit :

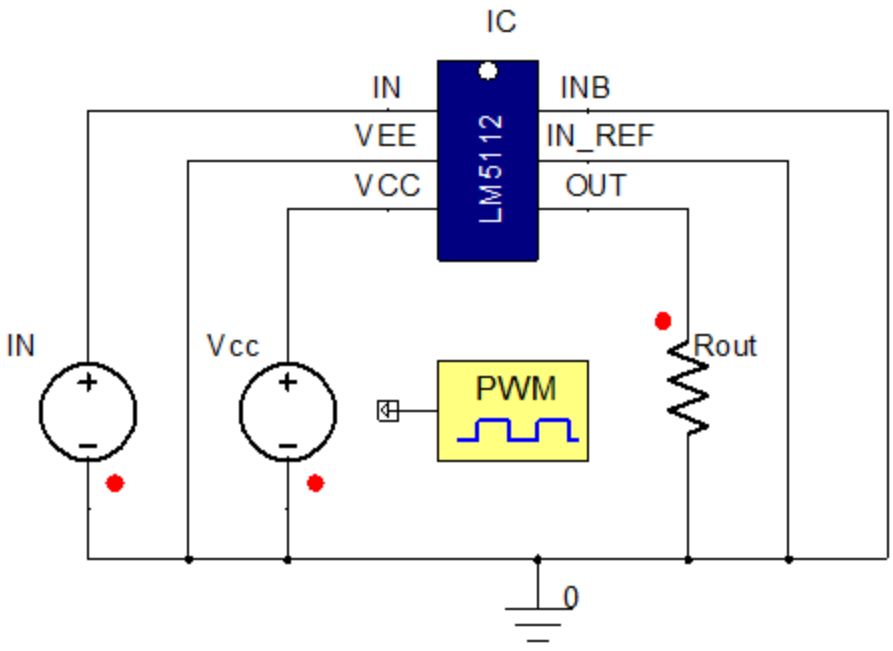

Figure 2. Example Circuit

Simulation results :

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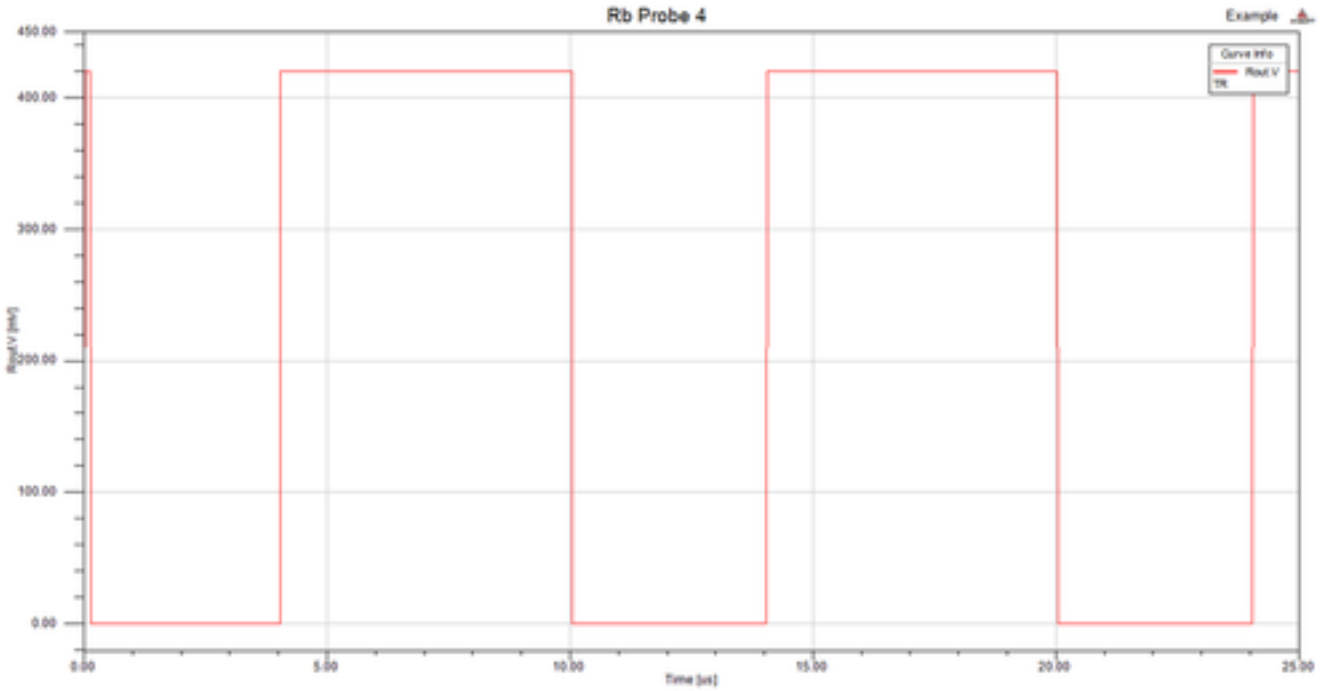

Figure 3. Simulation results

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References

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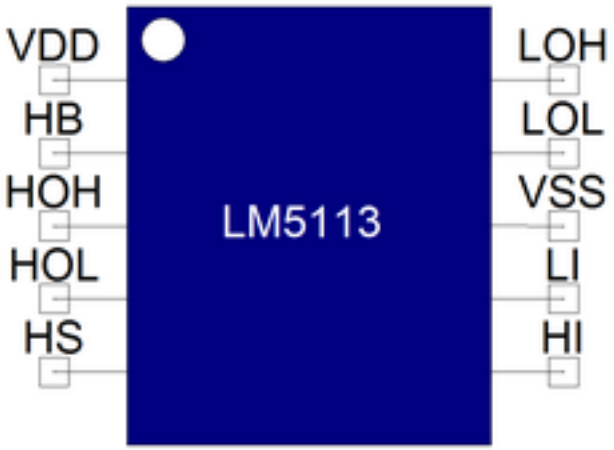
LM5113: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM5113* is designed to drive both the high-side and the low-side enhancement mode Gallium Nitride (GaN) FETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of driving a high-side enhancement mode GaN FET operating up to 100V. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.2V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The inputs of the *LM5113* are TTL logic compatible, and can withstand input voltages up to 14V regardless of the VDD voltage. The *LM5113* has split gate outputs, providing flexibility to adjust the turn-on and turn-off strength independently. In addition,

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the strong sink capability of the *LM5113* maintains the gate in the low state, preventing unintended turn-on during switching. The *LM5113* can operate up to several MHz. The *LM5113* is available in a standard LLP-10 pin package and a 12-bump micro SMD package. The LLP-10 pin package contains an exposed pad to aid power dissipation. The micro SMD package offers a compact footprint and minimized package inductance.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	5V Positive gate drive supply
2	HB	High-side gate driver bootstrap rail
3	HOH	High-side gate driver turn-on output
4	HOL	High-side gate driver turn-off output
5	HS	High-side GaN FET source connection
6	HI	High-side driver control input
7	LI	Low-side driver control input
8	VSS	Ground return
9	LOL	Low-side gate driver sink-current output
10	LOH	Low-side gate driver source current output

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Parameters

Comparison between model and real component.

Table 2

PARAMETE-RS	TEST CONDITIO-	MIN	TYP	MAX	MODE-L	UNIT-S

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

	NS					
Supply Currents						
VDD Quiescent Current	LI = HI = 0V		0.07	0.1	0.07	mA
VDD Operating Current	f = 500 kHz		2	3	-	mA
Total HB Quiescent Current	LI = HI = 0V		0.08	0.1	-	mA
Total HB Operating Current	f = 500 kHz		1.5	2.5	-	mA
HB to VSS Current, Quiescent	HS = HB = 100V		0.1	8	-	uA
HB to VSS Current, Operating	f = 500 kHz		0.4	1.0	-	mA
Input Pins						
Low Level Input Voltage Threshold	Rising Edge	1.89	2.06	2.18	2.06	V
High Level Input Voltage Threshold		1.48	1.66	1.76	1.66	mV
Input Pull-down Resistance		100	200	300	200	kohm
Under Voltage Protection						
VDD Rising Threshold		6.0	6.9	7.4	6.9	V
VDD Threshold Hysteresis			0.5		0.5	V
HB Rising Threshold		5.7	6.6	7.1	6.6	V
HB Threshold Hysteresis			0.4		0.4	V
Bootstrap Diode						
Low-Current Forward Voltage	IVDD-HB = 100 µA		0.60	0.9	.0.6	V
High-Current Forward	IVDD-HB = 100 mA		0.85	1.1	0.85	V

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Dynamic Resistance	IVDD-HB = 100 mA		1.0	1.65	-	ohm
HB-HS Clamp		4.7	5.2	5.45	5.2	V

Table 3

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
LO Gate Driver & HO Gate Driver						
Low-Level Output Voltage	IHOL = ILOL = 100 mA		0.06	0.10	0.06	V
High-Level Output Voltage	IHOH = ILOH = 100 mA		0.21	0.31	0.21	V
Peak SourceCur-rent	HOH, LOH = 0V		1.2		1.2	A
Peak SinkCurrent	VHO = 12V		5		5	A
High-Level Output Leak-ageCurrent	HOH, LOH = 0V			1.5	0	uA
Low-Level Output Leak-ageCurrent	HOL, LOL = 5V			1.5	0	uA
Switching Characteristics						
LO Turn-Off Propagation Delay	LI Fallingto LOL Falling		26.5	45	26.5	ns
LO Turn-OnPropaga-tionDelay	LI Risingto LOH Rising		28	45	28	ns
HO Turn-Off Propagation Delay	HI Fallingto HOL Falling		26.5	45	26.5	ns

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HO Turn-OnPropaga-tionDelay	HI Risingto HOH Rising		28	45	28	ns
Delay Match-ing: LO on & HO off	CL = 1000 pF		1.5	8	0	ns
Delay Match-ing: LO off & HO on			1.5	8	0	ns
HO Rise Time 0.5V - 4.5V	CL = 1000 pF		7		4.6	ns
LO Rise Time 0.5V - 4.5V	CL = 1000 pF		7		4.6	ns
HO Fall Time 0.5V - 4.5V	CL = 1000 pF		1.5		1.31	ns
LO Fall Time 0.5V - 4.5V	CL = 1000 pF		1.5		1.31	ns
Minimum Input Pulse Width that Changes the Output			10		-	ns
Bootstrap DiodeTurn-Off Time	IF = 100mA IR = 100mA		50		-	ns

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Example circuit :

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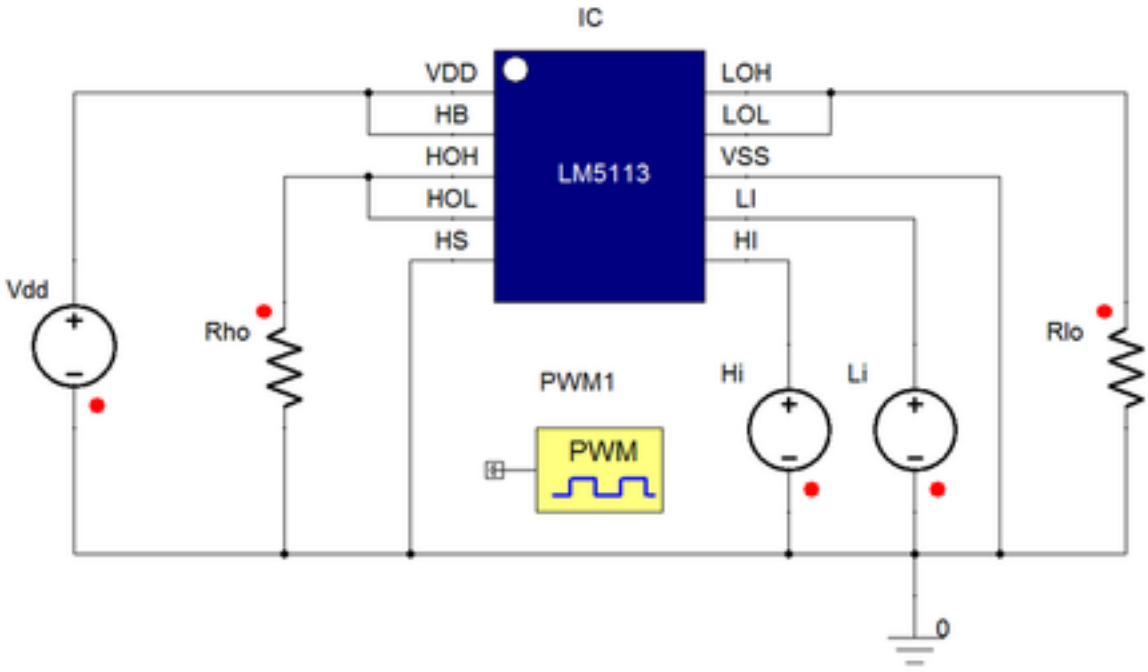
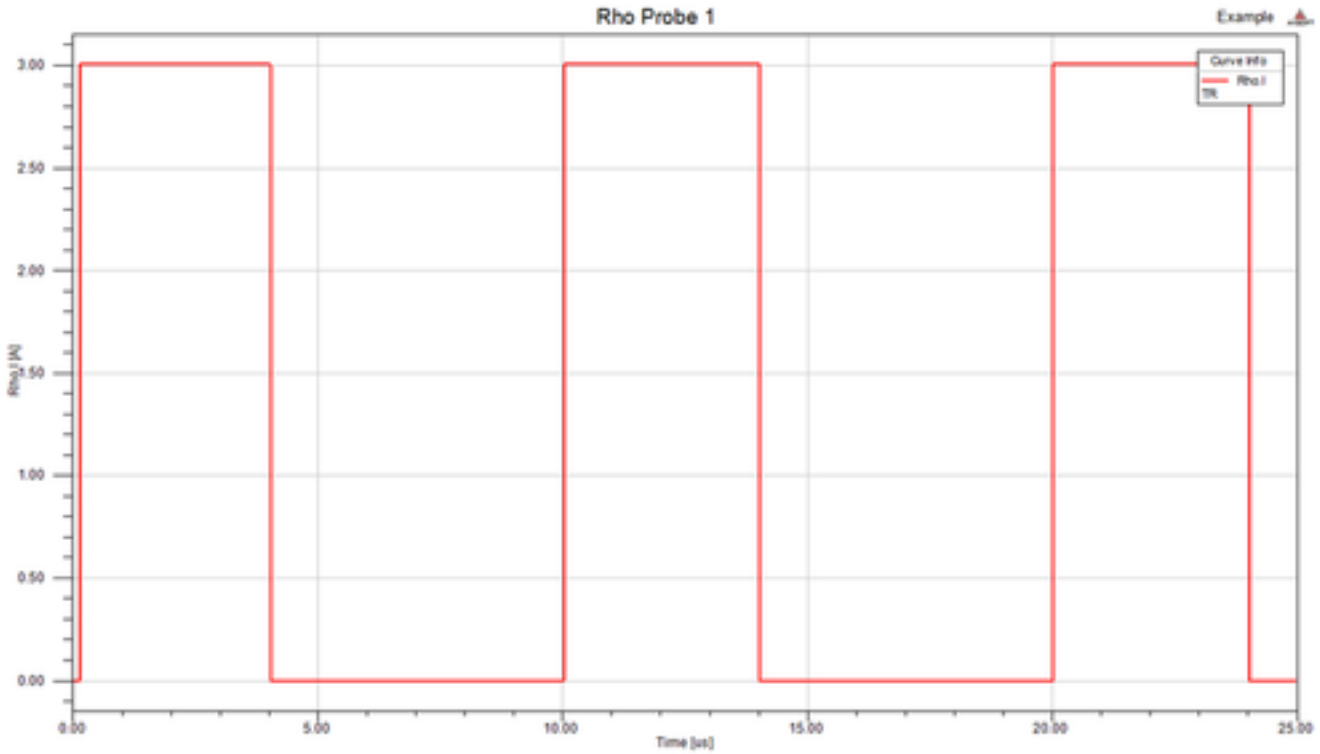


Figure 2. Example Circuit

Simulation results :



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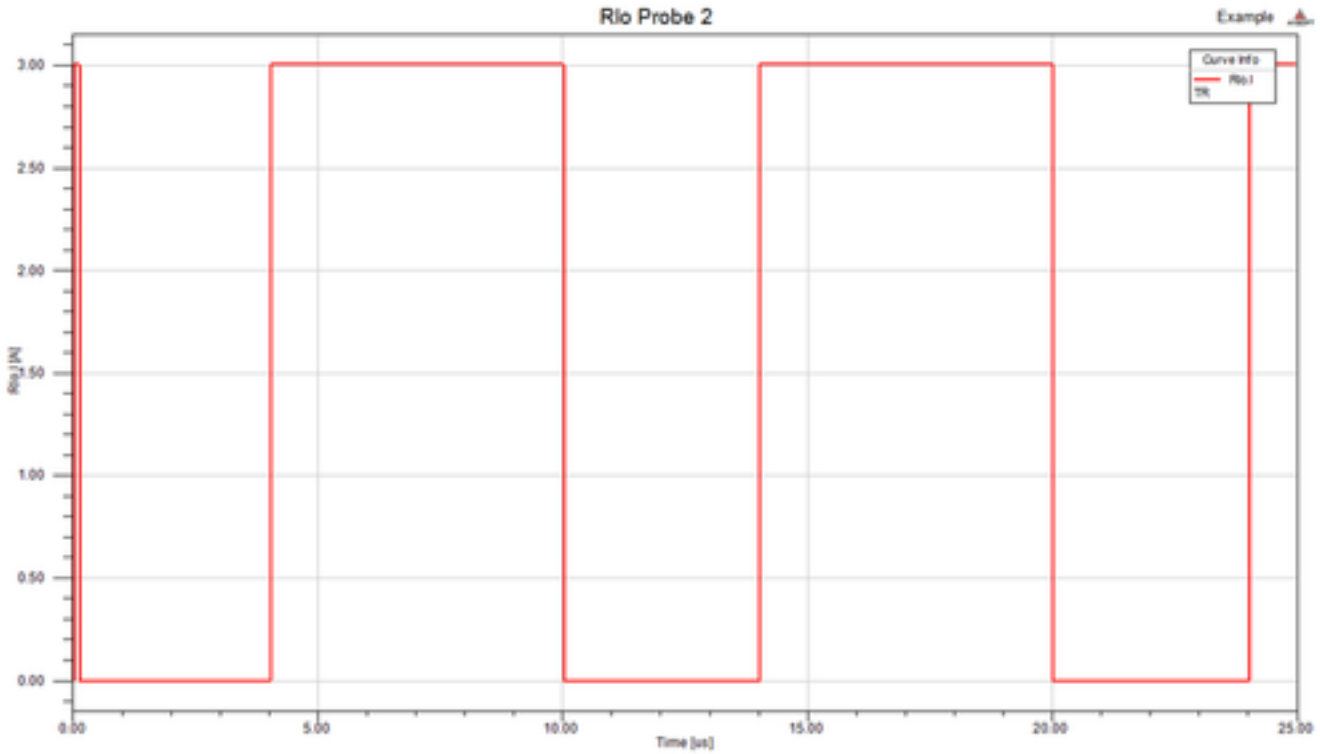

Figure 3. Simulation results

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References

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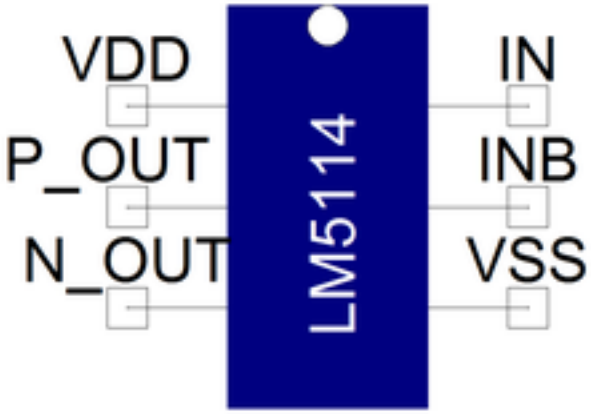
LM5114: Texas Instrument

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM5114* is designed to drive low-side MOSFETs in boost type configurations or to drive secondary synchronous MOSFETs in isolated topologies. With strong sink current capability, the *LM5114* can drive multiple FETs in parallel. The *LM5114* also has the features necessary to drive low-side enhancement mode Gallium Nitride (GaN) FETs. The *LM5114* provides inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive in a single device type. The inputs of the *LM5114* are TTL Logic compatible and withstand the input voltages up to 14V regardless of the VDD voltage. The *LM5114* has split gate outputs, providing flexibility to adjust the turn-on and turn-off strength independently. The *LM5114* has fast

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switching speed and minimized propagation delays, facilitating high frequency operation. The *LM5114* is available in SOT-23 6- pin package and LLP-6 package with an exposed pad to aid thermal dissipation.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Gate drive supply
2	P_OUT	Source-current output
3	N_OUT	Sink-current output
4	VSS	Ground
5	INB	Inverting logic input
6	IN	Non-invertinglogic input

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Power Supply						
V_{CC} Operating Range		4.0		12.6	12	V
VDD Under-voltage Lock-out	VDD Rising	3.25	3.6	4.00	3.6	V
VDD Under-voltage Lock-out Hysteresis			0.4		0.4	V
VDD Under-voltage lock-out to Output delay time	VDD Rising		300		300	ns
VDD Quiescent Current	IN = INB = VDD		0.95	1.9	0.95	mA
N-CHANNEL OUTPUT						
Driver Output Resistance - Pulling Down	VDD = 10V, I_{N-OUT} = -100mA		0.23		0.23	ohm
	VDD = 4.5V, I_{N-OUT} = -100mA		0.24		0.23	ohm
Power-off Pull Down Resistance	VDD = 0V, I_{N-OUT} = -10mA		3.3		3.3	ohm
Power-off Pull Down Clamp Voltage	VDD = 0V, I_{N-OUT} = -10mA		0.85		0.85	V
Output Leakage Current	N_OUT = VDD		6.85	20	0	uA
Peak Sink Current	C_L = 10,000pF		7.6		7.6	A
P-CHANNEL OUTPUT						
Driver Output Resistance - Pulling Up	VDD = 10V, I_{P-OUT} = 50mA		2.0	3.0	2.0	ohm

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	VDD = 4.5V, I_{P-OUT} = 50mA		2.20	3.30	2.0	ohm
Output Leakage Current	P_OUT = 0		0.00-1	10	0	uA
Peak Source Current	CL = 10,000pF		1.3		1.3	A
LOGIC INPUT						
Logic 1 Input Voltage		2.4			1.75	V
Logic 0 Input Voltage				0.8	1.05	V
Logic-Input Hysteresis			0.68		0.7	V
Logic-Input Current	INB = VDD or 0		0.00-1	10	0.001	uA

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Table 3

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
SWITCHING CHARACTERISTICS FOR VDD = +10V						
Rise Time	C_L = 1000pF		8		4.6	ns
	C_L = 5000pF		45		23	ns
	C_L = 10,000pF		82		46	ns
Fall Time	C_L = 1000pF		3.2		0.7	ns
	C_L = 5000pF		7.5		3.4	ns
	C_L = 10,000pF		12.5		6.8	ns
Turn-On Propagation Delay	C_L = 1000pF	6	12	25	12	ns
Turn-Off Propagation Delay	C_L = 1000pF	6	12	25	12	ns
Break-before-make Time			2.5		-	ns
SWITCHING CHARACTERISTICS FOR VDD = +10V						
Rise Time	C_L = 1000pF		12		4.6	ns
	C_L = 5000pF		41		23	ns
	C_L = 10,000pF		74		46	ns
Fall Time	C_L = 1000pF		3.0		0.7	ns
	C_L = 5000pF		7.0		3.4	ns
	C_L = 10,000pF		11.3		6.8	ns
Turn-On Propagation Delay	C_L = 1000pF	8	14	27	12	ns
Turn-Off Propagation Delay	C_L = 1000pF	8	14	27	12	ns
Break-before-make Time			4.2		-	ns

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Example circuit :

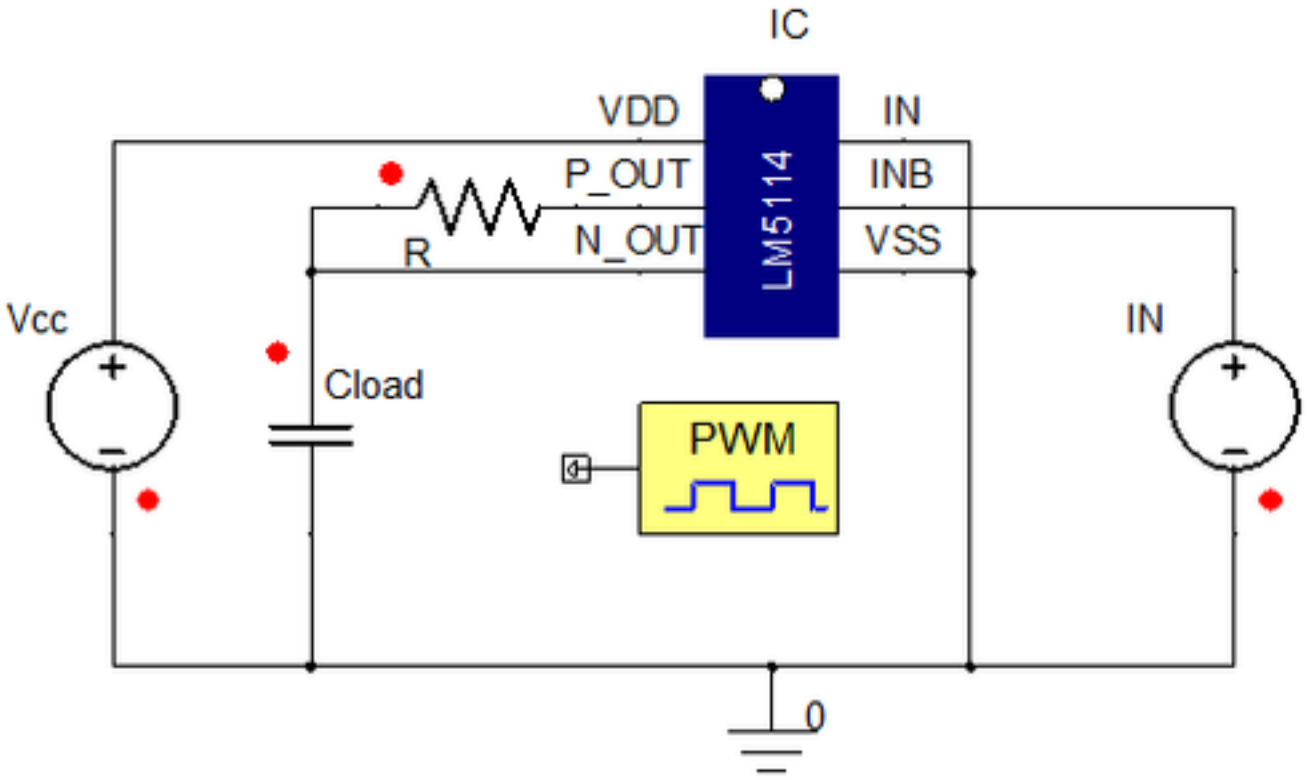

Figure 2. Example Circuit

Simulation results :

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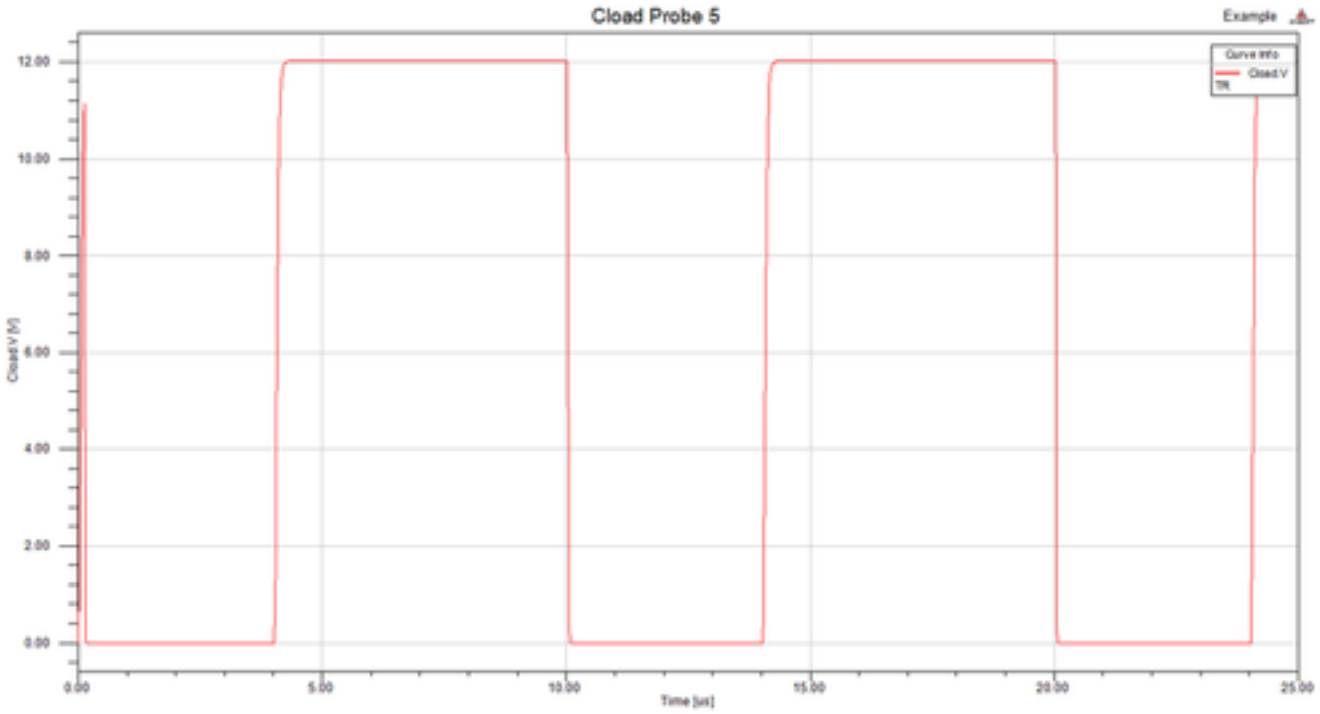

Figure 3. Simulation results

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References

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RIC7113A4: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

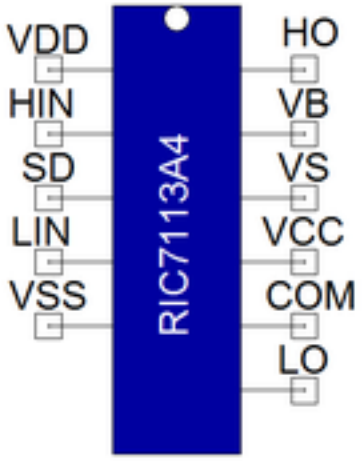

Figure 1. Component symbol

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Description

The International Rectifier *RIC7113A4* is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels.

Switching delays depend on Vdd voltage (its values appear in the "comparison between model and real component" section).

There are three parts clearly differentiated: the input part, in which control voltages are measured. State machines control the switches of the output signals and implements the real switching delays. And the switches simulate the totem-pole outputs.

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Conservative Pins

Table 1

Symbol	Description
VDO	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic ground
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

Product summary:

Table 2

V_{OFFSET}	400V max.
$I_{O+/-}$	2A / 2A

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V_{OUT}	10 - 20V
Ton/off (typ.)	120 & 100 ns
Delay Matching (typ.)	5 ns

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Parameters

Comparison between model and real component.

Apart from the parameters appeared in the product summary section, which the model matches with, there are some others parameters implemented as well:

Table 3

PARAMETER	DEFINITION		RIC7113A4	MODEL	UNITS
	Static Electrical Characteristics				
V_{IH}	Logic "1" input voltage	VDD = 5V	3.3	3.33	V
		VDD = 10V	6.8	6.66	
		VDD = 15V	10	10	
		VDD = 20V	13.3	13.33	
V_{IL}	Logic "0" input voltage	VDD = 5V	1.8	1.91	V
		VDD = 10V	3.8	3.85	
		VDD = 15V	6.0	5.77	
		VDD = 20V	8.3	7.69	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		9.7	9.7	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		9.4	9.4	V
V_{CCUV+}	V_{cc} supply under-voltage positive going threshold		9.6	9.6	V
V_{CCUV-}	V_{cc} supply under-voltage negative		9.4	9.4	V

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	going threshold			

Because of the pull down resistors connected to the input pins implemented inside the IC model, the input impedance is 100 kOhm (Zin=100kΩ) instead of infinite (as expected on an ideal model). Output impedance is zero (Zo=0). Temperature influence parameters as well as bias and leakage currents have not been implemented.

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In this circuit the IC provides the control signals of a half-bridge inverter with a resistive load, using a capacitive voltage divider to get high and low sides.A lower frequency pulse voltage source is connected to SD pin to check the behavior of the logic input for shutdown. Vcc is 15V.

Example circuit :

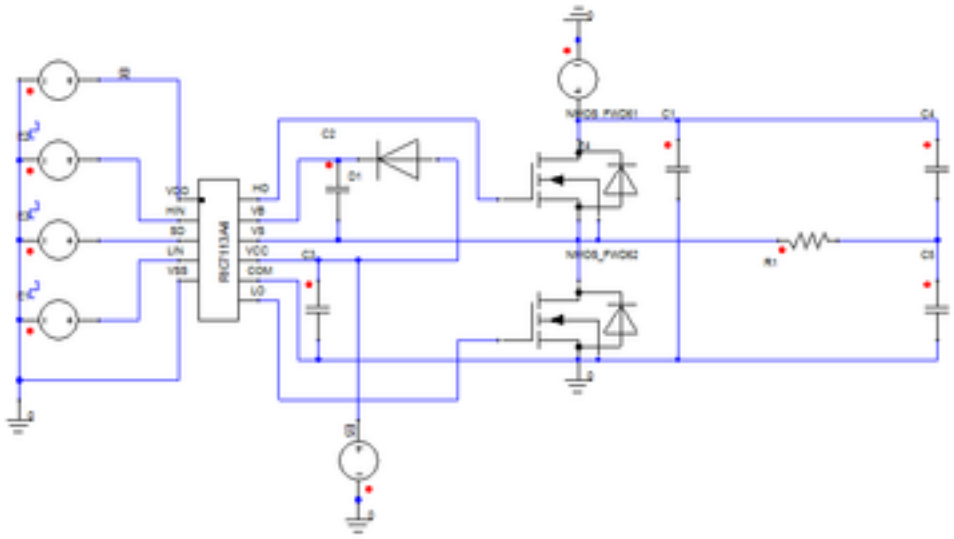

Figure 2. Example Circuit

Simulation results :

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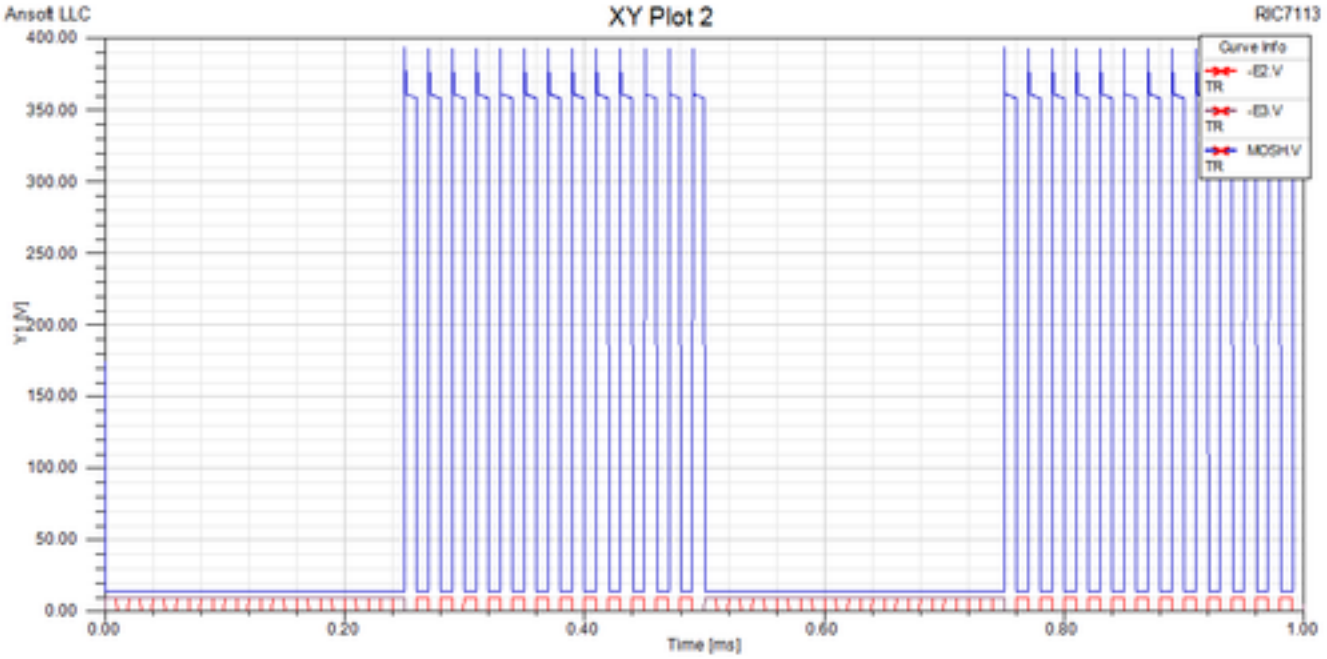
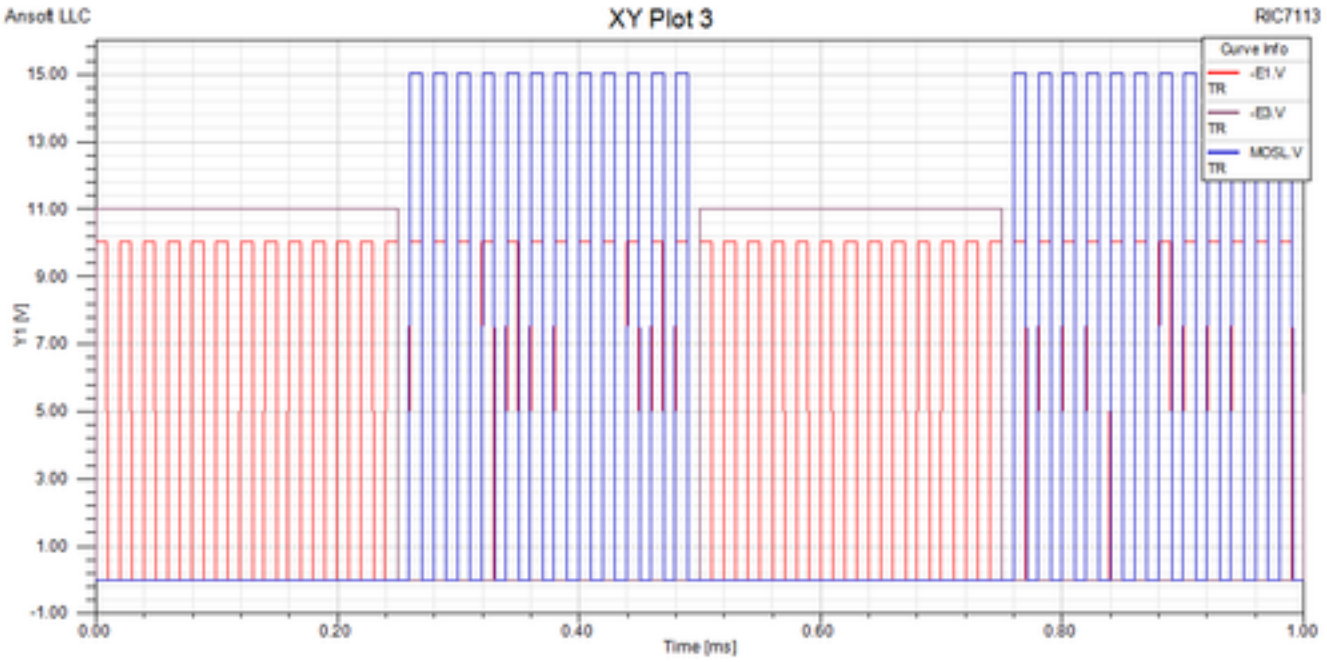


Blue: high side MOSFET gate voltage

Red: high side input voltage

Brown: shutdown input voltage



Blue: low side MOSFET gate voltage

Red: shutdown input voltage

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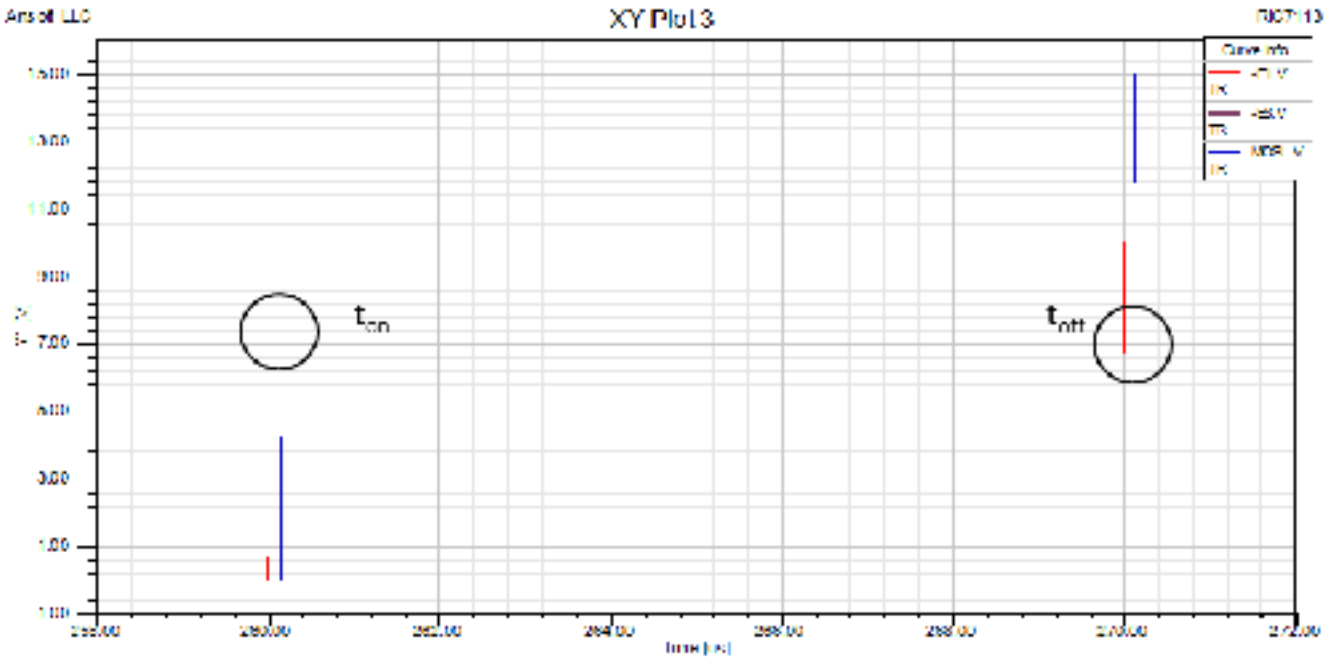
Brown: low side input voltage

Figure 3. Simulation results

When SD (shutdown) is high, output HO and LO voltages fall to their low value.

Detail of timing implementation:



Blue: low side MOSFET gate voltage

Red: shutdown input voltage

Brown: low side input voltage

Figure 4. Detail of timing implementation

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References

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UCC27200A: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

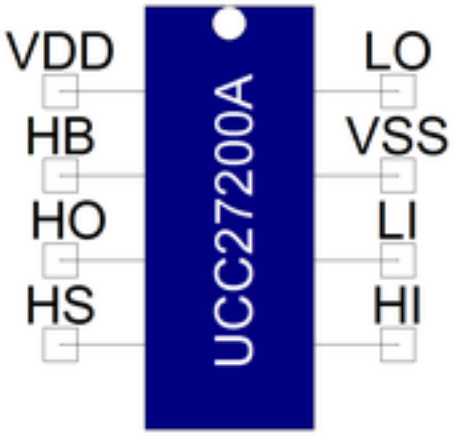

Figure 1. Component symbol

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Description

The *UCC27200A/1A* family of high frequency N-Channel MOSFET drivers include a 120-V bootstrap diode and high-side/low-side driver with independent inputs for maximum control flexibility. This allows for N-Channel MOSFET control in half-bridge, full-bridge, two-switch forward and active clamp forward converters. The low-side and the high-side gate drivers are independently controlled and matched to 1-ns between the turn-on and turn-off of each other. The *UCC27200A/1A* are based on the popular UCC27200/1 drivers, but offer some enhancements. In order to improve performance in noisy power supply environments the *UCC27200A/1A* has an

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enhanced ESD input structure and also has the ability to withstand a maximum of -18 V on its HS pin.

The model consists in state machines, voltmeters and sources. The states machines model the logic of the output stage, the delays and the UVLO protection. The output stage is modeled by controlled current sources. This current sources behaves as resistance until 3A current output is reached then the current is maintained constant at 3A.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Positive supply to the lower gate driver. De-couple this pin to VSS (GND). Typical decoupling capacitor range is 0.22 µF to1.0 µF.
2	HB	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF, the value is dependant on the gate charge of the high-side MOSFET however.
3	HO	High-side output. Connect to the gate of the high-side power MOSFET.
4	HS	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
5	HI	High side driver input
6	LI	Low side driver input
7	VSS	Negative supply terminal for the device which is generally grounded.
8	LO	Low-side output. Connect to the gate of the low-side power MOSFET.

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply currents						
VDD quiescent current			0.4	0.8		mA
VDD operating current			2.5	4		mA
Boot voltage quiescent current			0.4	0.8		mA
Boot voltage operating current			2.4	4		mA
HB to VSS quiescent current			0.0005	1		uA
HB to VSS operating current			0.1			mA
Inputs						
Input rising threshold			5.8	8	5.8	V
Input falling threshold		3	5.4		5.4	V
Input voltage hysteresis			0.4		0.4	V
Input voltage threshold			1.7	2.5	1.7	V
Input voltage threshold		0.8	1.6		1.6	V
Input voltage Hysteresis			100		100	mV
Input pull-down resistance		100	200	350	200	kohm
Undervoltage Protection (UVLO)						
VDD rising threshold		6.2	7.1	7.8	7.1	V
VDD threshold hysteresis			0.5		0.5	V
VHB rising threshold		5.8	6.7	7.2	6.7	V
VHB			0.4		0.4	V

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threshold hysteresis						
Bootstrap Diode						
Low-current forward voltage	I=100ua		0.65	0.85	0.65	V
High-current forward voltage	I=100ma		0.85	1.1	0.85	V
Dynamic resistance, ΔVF/ΔI			0.6	1.0	2	Ohm
HO and LO Gate Driver						
Low level output voltage	I=100ma		0.18	0.4	0.18	V
High level output voltage	I=-100ma		0.25	0.4	0.25	V
Peak pull-up current	V= 0V		3		3	A
Peak pull-down current	V= 12V		3		3	A
Propagation Delays						
VLI falling to VLO falling			20	45	20	ns
VHI falling to VHO falling			20	50	20	ns
VLI rising to VLO rising			20	45	20	ns
VHI rising to VHO rising			20	50	20	ns
Delay Matching						
LI ON, HI OFF			1	7	0	ns
LI OFF, HI ON			1	7	0	ns
Output Rise and Fall Time						
Rise time			8			ns
Fall time			7			ns

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Input/Output Quantities

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Examples

Example circuit :

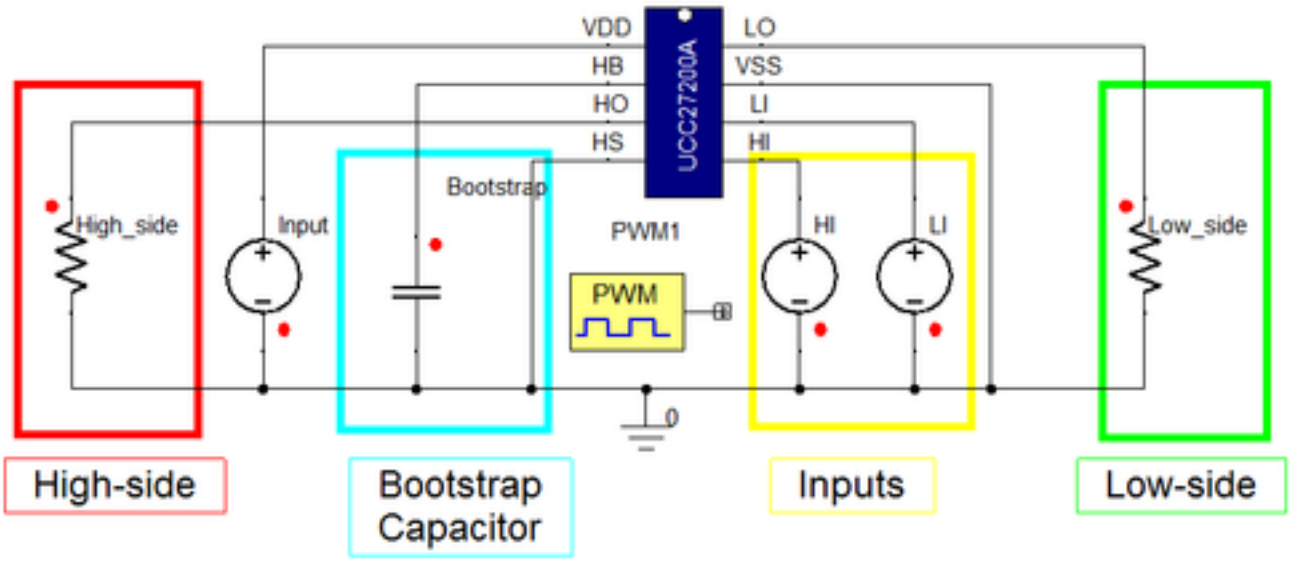
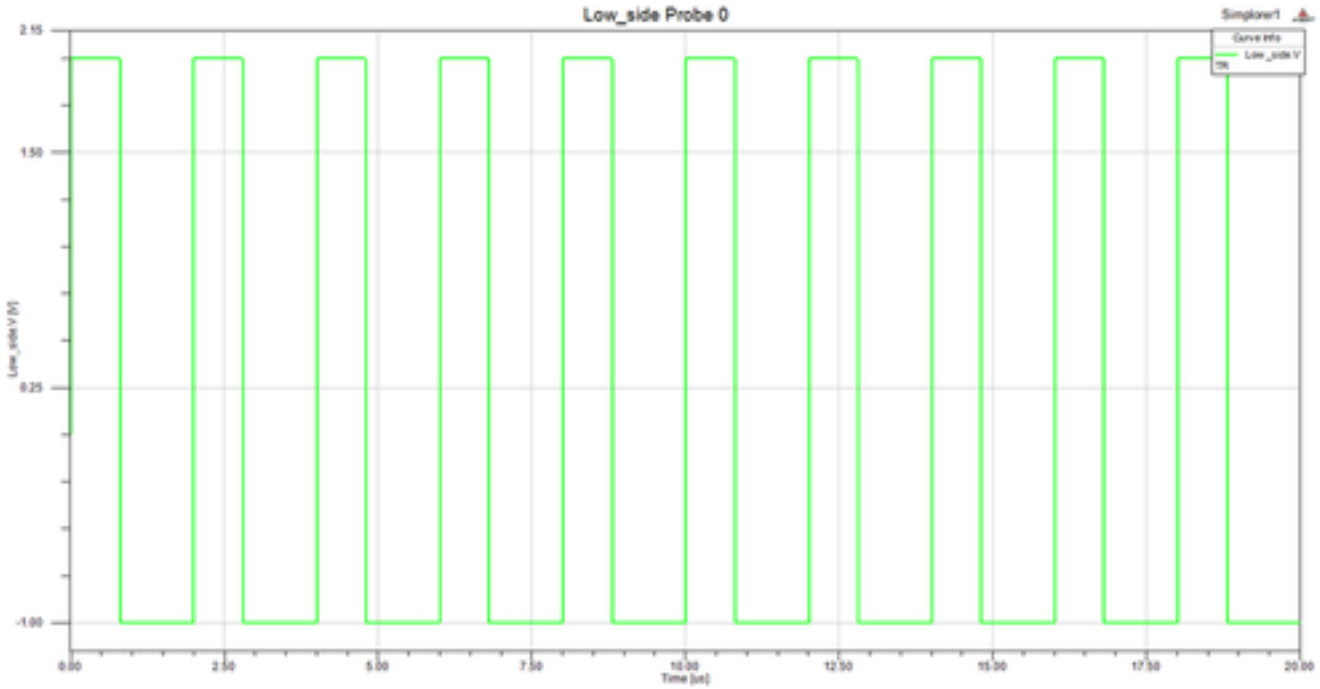


Figure 2. Example Circuit

Simulation results :



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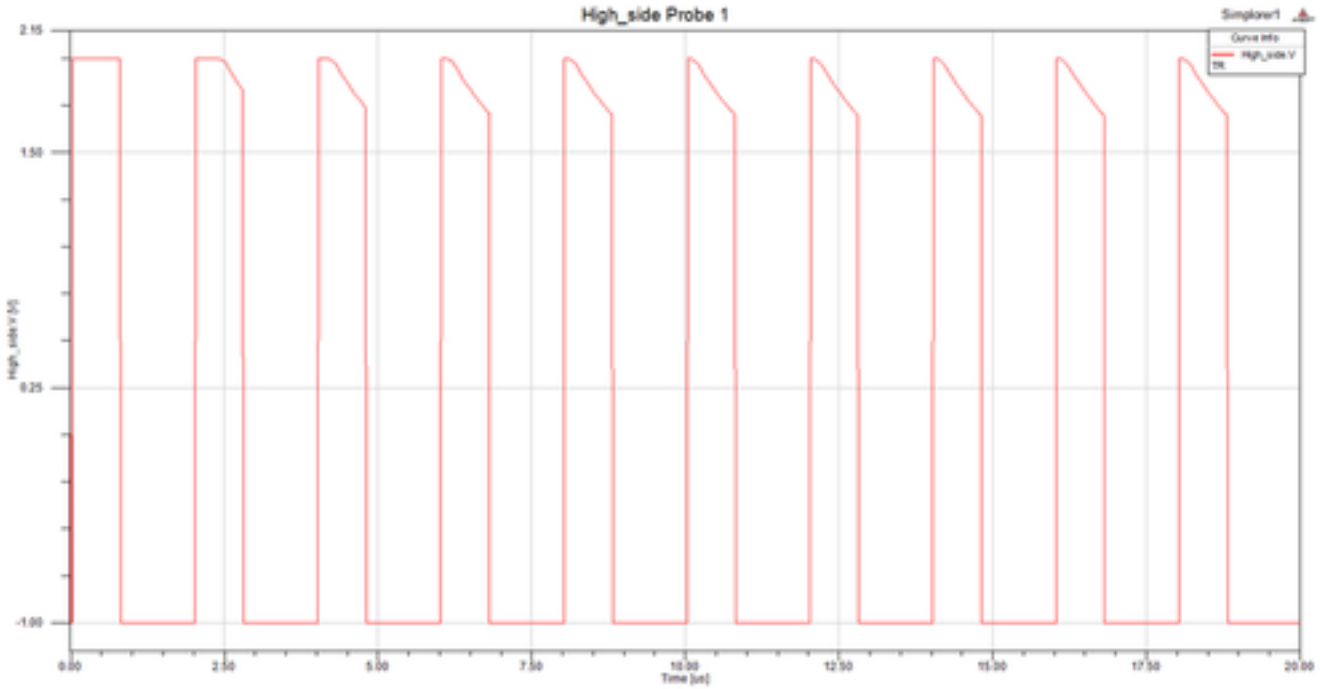

Figure 3. Simulation results

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References

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UCC27517: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

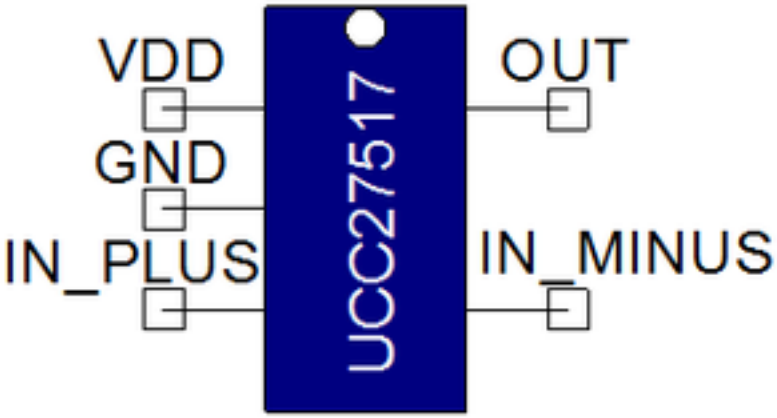

Figure 1. Component symbol

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Description

The *UCC27517* single-channel, high-speed, low-side gate driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, *UCC27517* is capable of sourcing and sinking high, peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 13 ns.

The *UCC27517* provides 4-A source, 4-A sink (symmetrical drive) peak-drive current capability at VDD = 12 V.

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The *UCC27517* is designed to operate over a wide VDD range of 4.5 V to 18 V and wide temperature range of -40°C to 140°C. Internal Under Voltage Lockout (UVLO) circuitry on VDD pin holds output low outside VDD operating range. The capability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging wide band-gap power switching devices such as GaN power semiconductor devices.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VDD	Bias supply input.
2	GND	Ground. All signals referenced to this pin.
3	IN+	Non-inverting input. When the driver is used in inverting configuration connect IN+ to VDD in order to enable output, OUT held LOW if IN+ is unbiased or floating
4	IN-	Inverting input. When the driver is used in non-inverting configuration connect IN- to GND in order to enable output, OUT held LOW if IN- is unbiased or floating
5	OUT	Sourcing/Sinking current output of driver.

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Bias currents						
Startup current	IN+=VDD IN-=GND	40	100	160	0	uA
	IN+=IN-=GND or IN+=IN-=VDD	25	75	145	0	uA
	IN+ = GND IN- = VDD	20	60	115	0	uA
Under voltage lockout (UVLO)						
Supply start threshold		3.91	4.20	4.5	4.2	V
Minimum operating voltage after supply start		3.45	3.9	4.35	3.9	V
Supply voltage hysteresis		0.2	0.3	0.5	0.3	V
Inputs						
Input signal high threshold			2.2	2.4	2.2	V
Input signal low threshold		1.0	1.2		1.2	V
Input signal hysteresis			1.0		1	V
Source/Sink source						
Source/sink peak current	CLOADD=0.22µF FSW = 1kHz		-4 / +4		x	A
Outputs						
High output voltage	VDD = 12 V IOUT = -10 mA		50	90	50	mV
	VDD = 4.5 V		60	130	50	mV

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	IOUT = -10 mA					
Low output voltage	VDD = 12 V IOUT = -10 mA		5	10	5	mV
	VDD = 4.5 V IOUT = -10 mA		6	12	5	mV
Output pull-up resistance	VDD = 12 V IOUT = -10 mA		5.0	7.5	5.0	ohm
	VDD = 4.5 V IOUT = -10 mA		5.0	11.0	5.0	ohm
Output pull-down resistance	VDD = 12 V IOUT = -10 mA		0.5	1.0	0.5	ohm
	VDD = 4.5 V IOUT = -10 mA		0.6	1.2	0.5	ohm

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Table 3

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
Bias cur-rents						
Rise time	VDD = 12 V CLOAD-D=1.8nF		8	12	19	ns
	VDD = 4.5 V CLOAD-D=1.8nF		16	22	19	ns
Fall time	VDD = 12 V CLOAD-D=1.8nF		7	11	2	ns
	VDD = 4.5 V CLOAD-D=1.8nF		7	11	2	ns
IN+ to output propagation delay	VDD = 12 V CLOAD-D=1.8nF	4	13	23	13	ns
	VDD = 4.5 V CLOAD-D=1.8nF	4	15	26	13	ns
IN- to output propagation delay	VDD = 12 V CLOAD-D=1.8nF	4	13	23	13	ns
	VDD = 4.5 V CLOAD-D=1.8nF	4	19	30	13	ns

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Examples

Example circuit :

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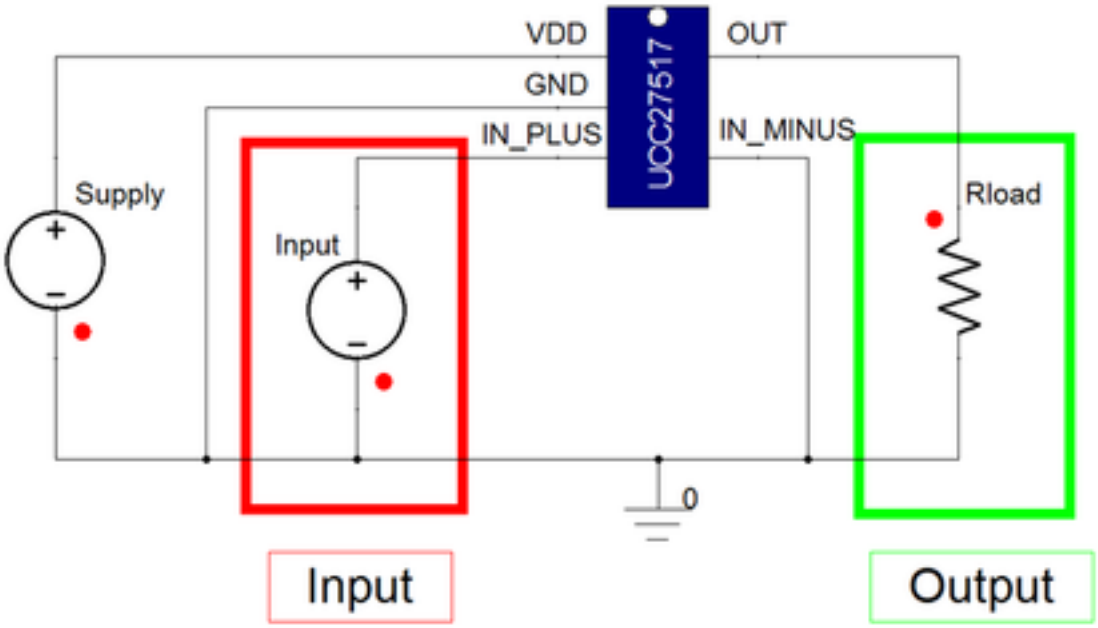

Figure 2. Example Circuit

Simulation results :

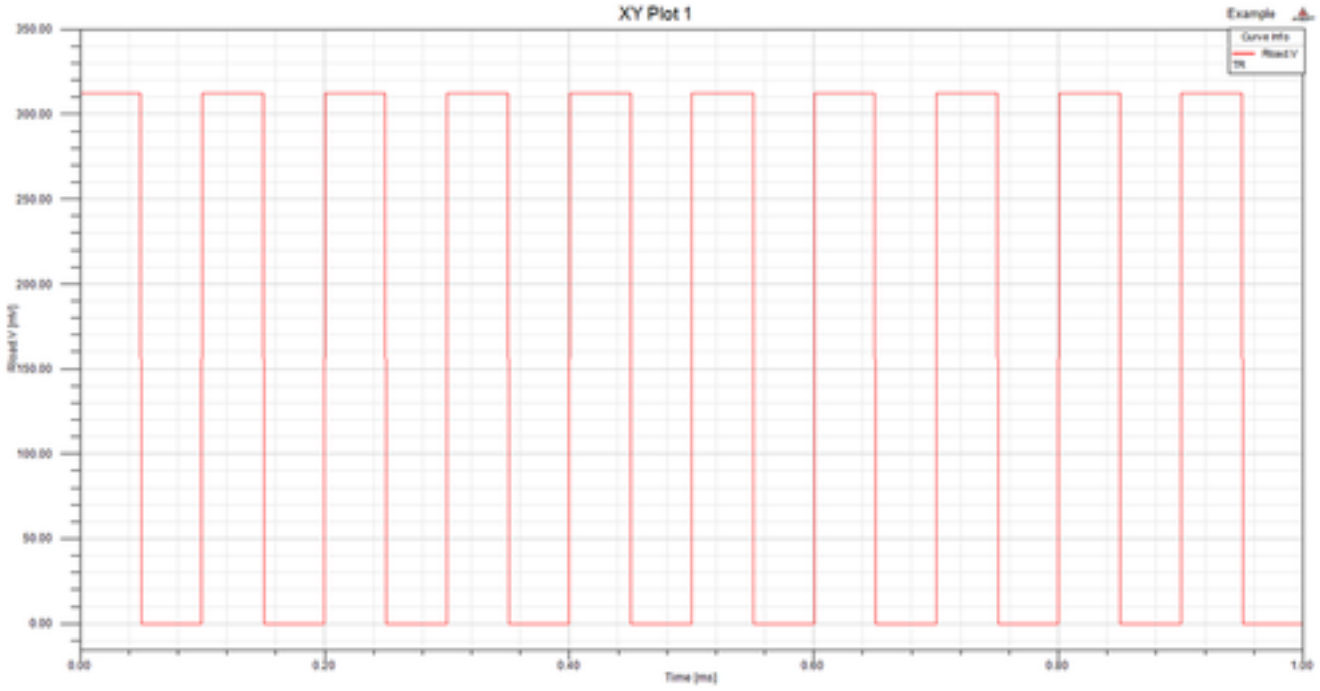

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Figure 3. Simulation results

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References

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High Side Switches

The High Side Switches consist of the following types of models:

- IPS6011
- IPS6021
- IPS6031
- IPS6041

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IPS6011: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

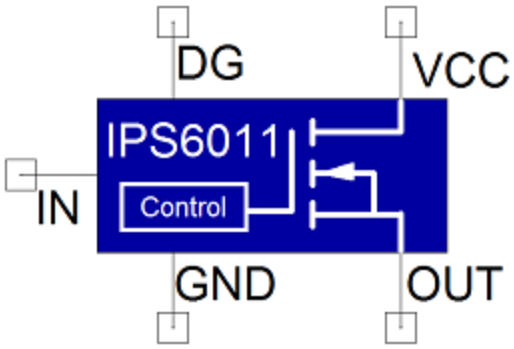

Figure 1. Component symbol

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Description

The *IPS6011* is a five terminal Intelligent Power Switch (IPS) for use in a high side configuration. It features short circuit, inductive load capability and diagnostic feedback. The output current is limited to the Ilimit value. A diagnostic pin provides different voltage levels for each fault condition. The double level shifter circuitry will allow large offsets between the logic and load ground.

The model has four parts. The first one models the input voltage limitation and measures it.

The left-up one models the diagnosis voltage with an ideal switch and a zener diode. The main part models the MOSFET with an ideal switch and a variable impedance which allows to model the Rdson and the current limit. The last part is a state machine which controls the main switching and its delays.

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Conservative Pins

Table 1

Symbol	Description
IN	Control signal
VCC	MOSFET drain
OUT	MOSFET source
DG	Diagnostic signal
GND	Logic ground

Product summary:

Table 2

Rds (on)	14mΩ (max.)
Vclamp	39V
I Limit	60A (typ.)
Open load	3V / 2.4A

Table 3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdon	Turn-on delay time		30	60	µs
Tr1	Rise time to Vout=Vcc-5V		25	50	
Tr2	Rise time to Vout=0.9 x		40	100	

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Tdoff	Turn-off delay time		70	140	
Tf	Fall time to Vout=0.1 x Vcc		30	80	
F max.	Max. switch-ing frequency			0.3	kHz

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Parameters

Comparison between model and real component.

The model matches the real model parameters concerning switching delays (ton and toff), maximum current, voltage clamp and conduction resistance as they appear in the product summary section.

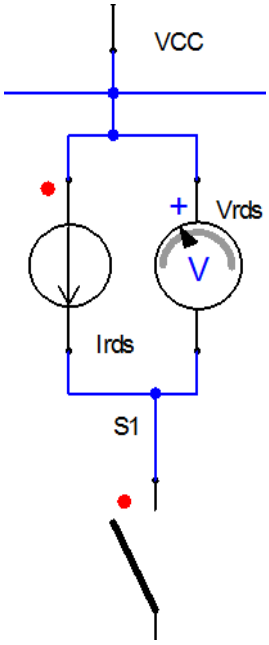

Figure 2. Partial View of the Block Diagram

Conduction resistance has been modeled with a current source in parallel with a voltmeter. This way we can achieve resistive impedance until the output current reaches the Ilimit value (60 A) from which the current is constant and equal to this value:

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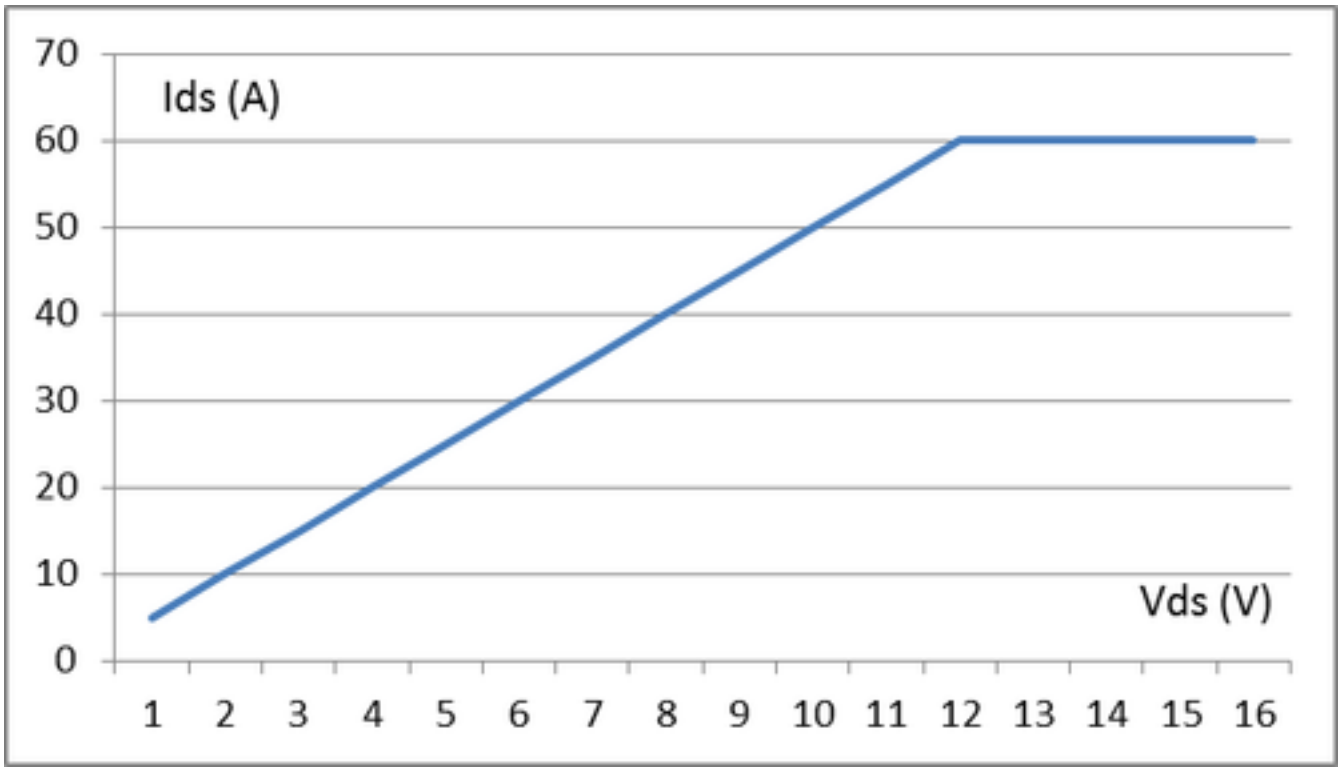

Figure 3. Conduction Resistance Curve

Input impedance is 150 kOhm. Input voltage is limited to 6 V by a zener diode. Temperature influence parameters have not been implemented.

Static Electrical Characteristics:

Tj=25°C, Vcc=14V (unless otherwise specified)

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Table 4

Symbol	Parameter	IPS6011	MODEL	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	11	14	mΩ	Vin=5V, Iout=20A
	ON state resistance Tj=150°C	19.5	14		Vin=5V, Iout=20A
	ON state resistance Tj=25°C, Vcc=6V	12	14		Vin=5V, Iout=20A
	ON state resistance during reverse battery	15	14		Vcc-Gnd=14V
Vcc op.	Operating voltage range with short circuit protection	6-24	X		
V clamp 1	Vcc to Out clamp voltage 1	39	39		Iout=50mA
V clamp 2	Vcc to Out clamp voltage 2	40	40	V	Iout=16A
Icc Off	Supply currentwhen Off	4	X	µA	Vin=0V, Vout=0V
Icc On	Supply currentwhen On	2.2	X	mA	Vin=5V
Vih	Input high threshold voltage	2.5	2.5		
Vil	Input low threshold voltage	2	2		
In hyst.	Input hysteresis	0.5	X	V	
Iin On	Input current when	40	80	µA	Vin=5V

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	device is On				
Idg	Dg leakagecur-rent	0.1	0		Vdg=5V
Vdg	Low level DG voltage	0.25	0.25	V	Idg=1.6mA

X: not implemented

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Examples

Example circuit :

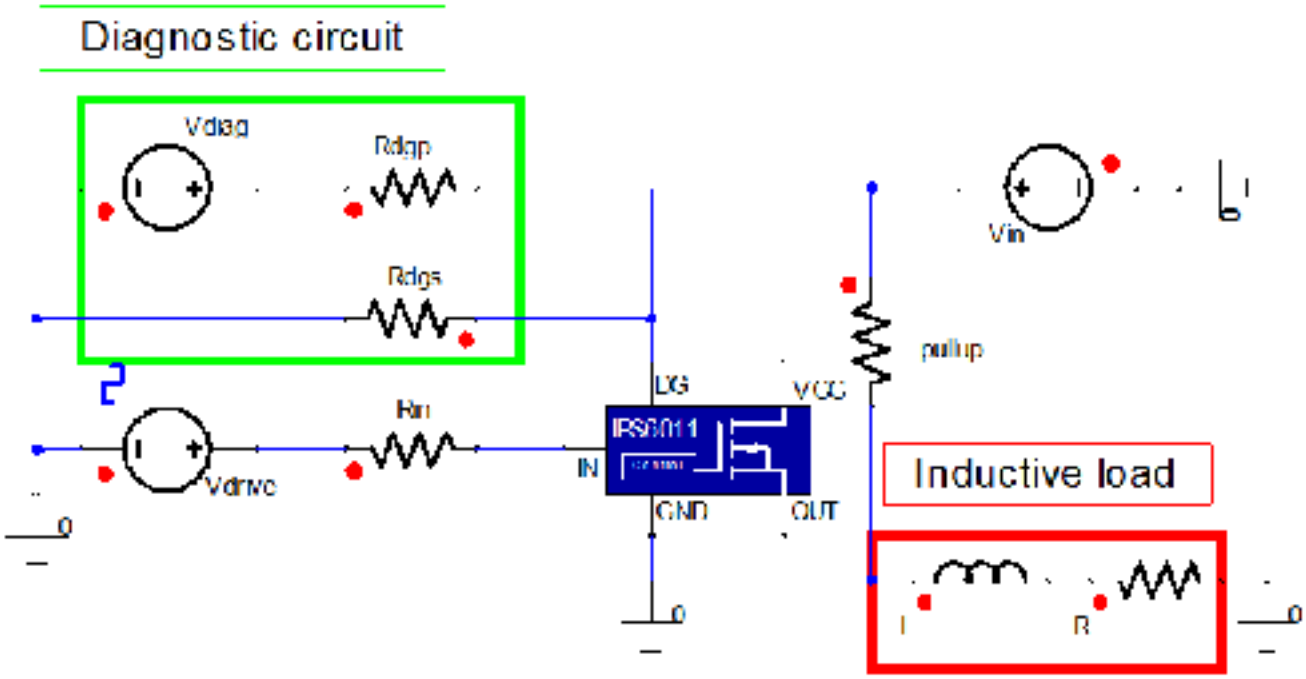

Figure 4. Example Circuit

This low side switch is used here to feed an inductive load. This kind of load allows us to check the steady operation and the current limitation system.

Simulation results :

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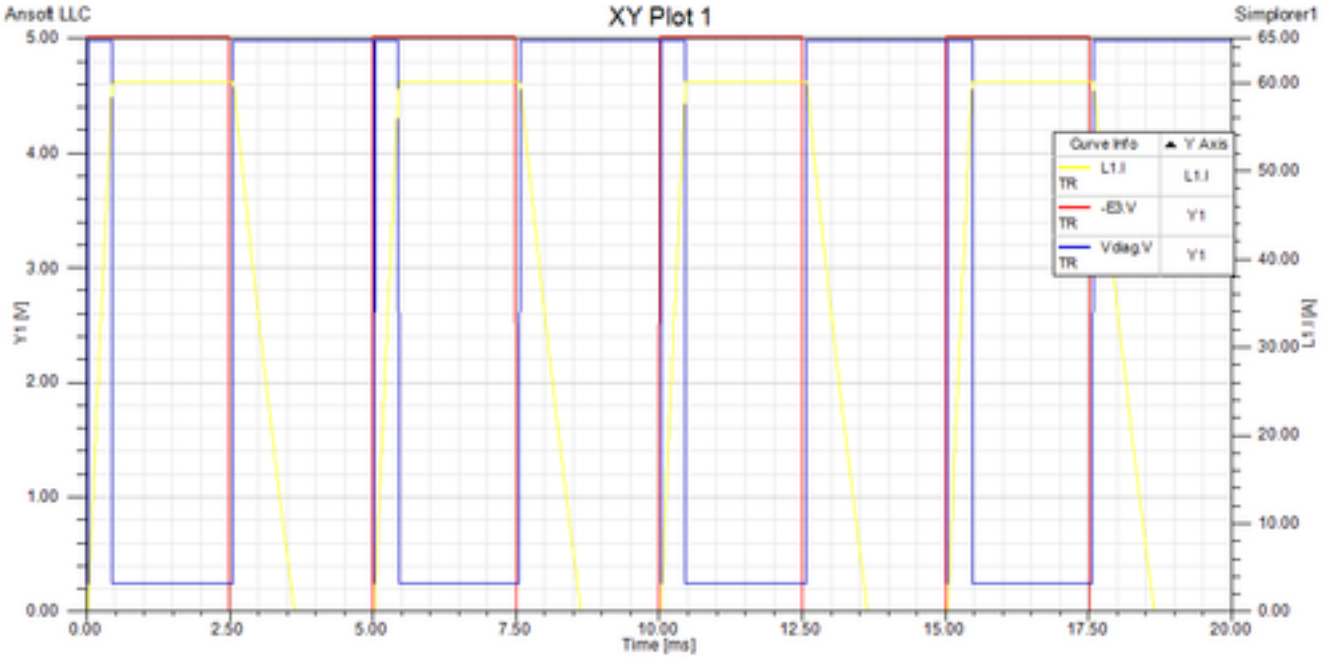

Yellow: load current

Red: input voltage

Blue: diagnostic voltage

Figure 5. Simulation results

When the load current reaches the current limit, is clamped to this value. Then, the diagnosis voltage falls to its low value.

Detail of timing implementation:

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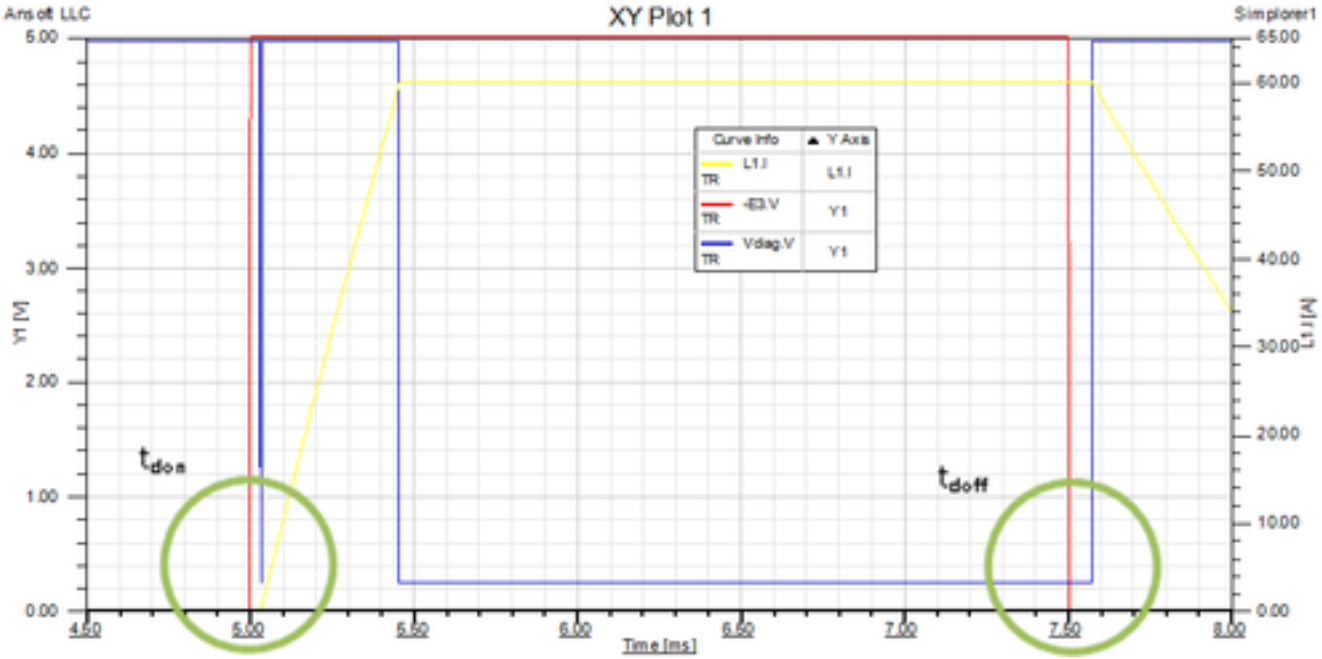

Yellow: load current

Red: input voltage

Blue: diagnostic voltage

Figure 6. Detail of timing implementation

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References

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IPS6021: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

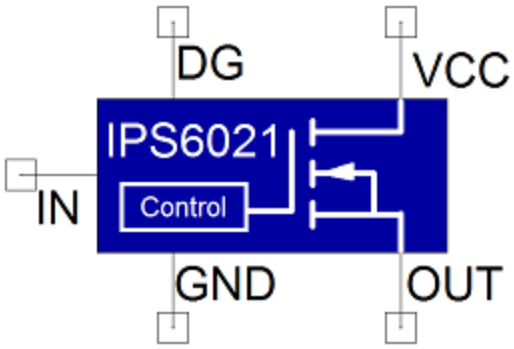

Figure 1. Component symbol

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• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

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Description

The *IPS6021* is a five terminal Intelligent Power Switch (IPS) for use in a high side configuration. It features short circuit, inductive load capability and diagnostic feedback. The output current is limited to the Ilimit value. A diagnostic pin provides different voltage levels for each fault condition. The double level shifter circuitry will allow large offsets between the logic and load ground.

The model has four parts. The first one models the input voltage limitation and measures it. The left-up one models the diagnosis voltage with an ideal switch and a zener diode. The main part models the MOSFET with an ideal switch and a variable impedance which allows to model the Rdson and the current limit. The last part is a state machine which controls the main switching and its delays.

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Conservative Pins

Table 1

Symbol	Description
IN	Control signal
VCC	MOSFET drain
OUT	MOSFET source
DG	Diagnostic signal
GND	Logic ground

Product summary:

Table 2

Rds (on)	30mΩ (max.)
Vclamp	39V
I Limit	32A (typ.)
Open load	3V / 1.1A

Table 3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdon	Turn-on delay time	-	14	28	µs
Tr1	Rise time to Vout=Vcc-5V	-	10	28	
Tr2	Rise time to Vout=0.9 x	-	18	50	

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Tdoff	Turn-off delay time	-	40	70	
Tf	Fall time to Vout=0.1 x Vcc	-	15	45	
F max.	Max. switch-ing frequency	-	-	1.5	kHz

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Parameters

Comparison between model and real component.

The model matches the real model parameters concerning switching delays (ton and toff), maximum current, voltage clamp and conduction resistance as they appear in the product summary section.

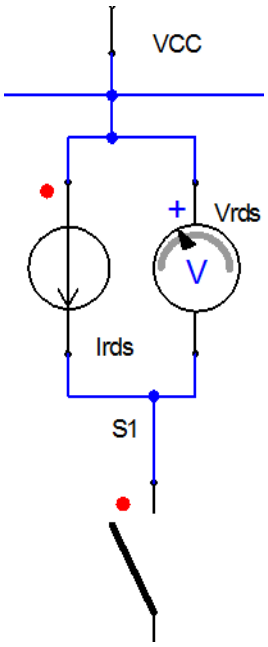

Figure 2. Partial View of the Block Diagram

Conduction resistance has been modeled with a current source in parallel with a voltmeter. This way we can achieve resistive impedance until the output current reaches the Ilimit value (32 A) from which the current is constant and equal to this value:

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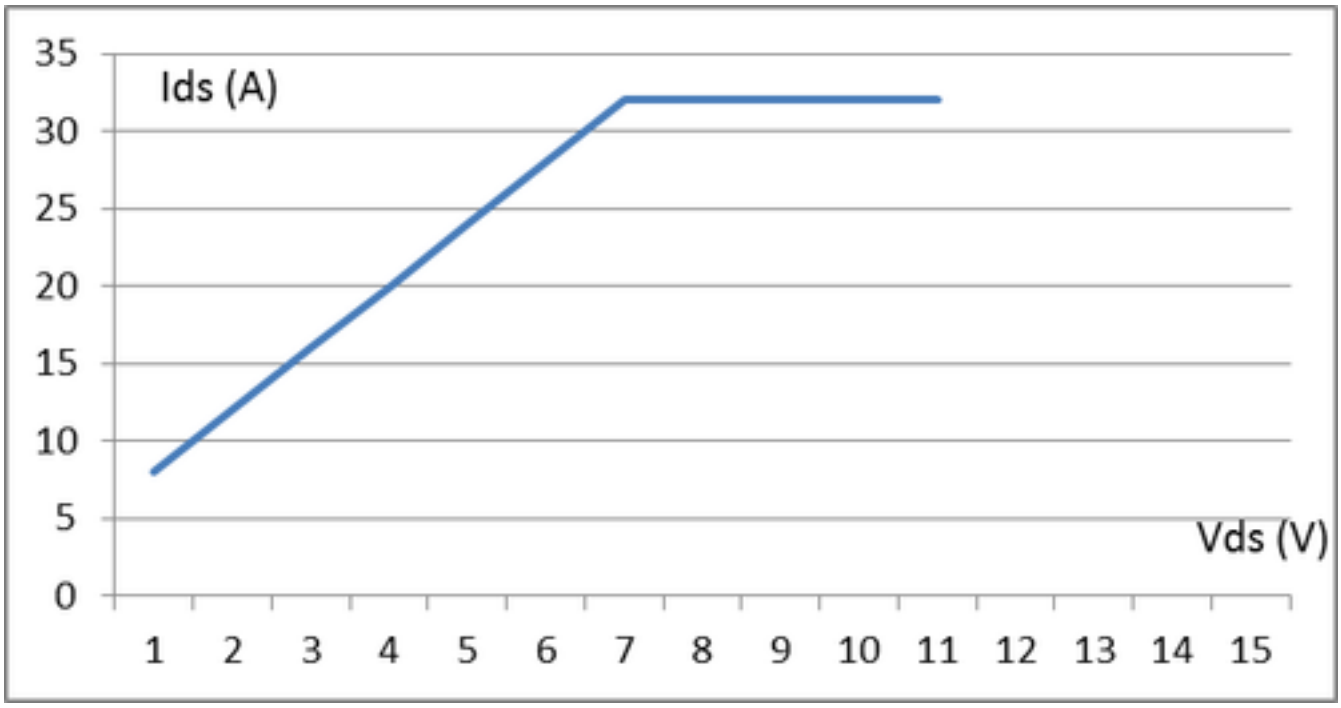

Figure 3. Conduction Resistance Curve

Input impedance is 150 kOhm. Input voltage is limited to 6 V by a zener diode. Temperature influence parameters have not been implemented.

Static Electrical Characteristics:

Tj=25°C, Vcc=14V (unless otherwise specified)

Table 4

Symbol	Parameter	IPS6021	MODEL	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	24	30	mΩ	Vin=5V, Iout=10A
	ON state resistance Tj=150°C	42	30		Vin=5V, Iout=10A
	ON state resistance Tj=25°C, Vcc=6V	29	30		Vin=5V, Iout=5A
	ON state resistance during	31	30		Vcc-Gnd=14V

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	reverse bat-tery				
Vcc op.	Operating voltage range with short circuit protection	6-28	X	V	
V clamp 1	Vcc to Out clamp voltage 1	39	39		Iout=40mA
V clamp 2	Vcc to Out clamp voltage 2	40	40		Iout=8A
Icc Off	Supply cur-rentwhen Off	4	X	µA	Vin=0V, Vout=0V
Icc On	Supply cur-rentwhen On	2.2	X	mA	Vin=5V
Vih	Input high threshold voltage	2.5	2.5	V	
Vil	Input low threshold voltage	2	2		
In hyst.	Input hys-teresis	0.5	X		
Iin On	Input cur-rent when device is On	40	80	µA	Vin=5V
Idg	Dg leakagecur-rent	0.1	0		Vdg=5V
Vdg	Low level DG voltage	0.25	0.25	V	Idg=1.6mA

X: not implemented

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Example circuit :

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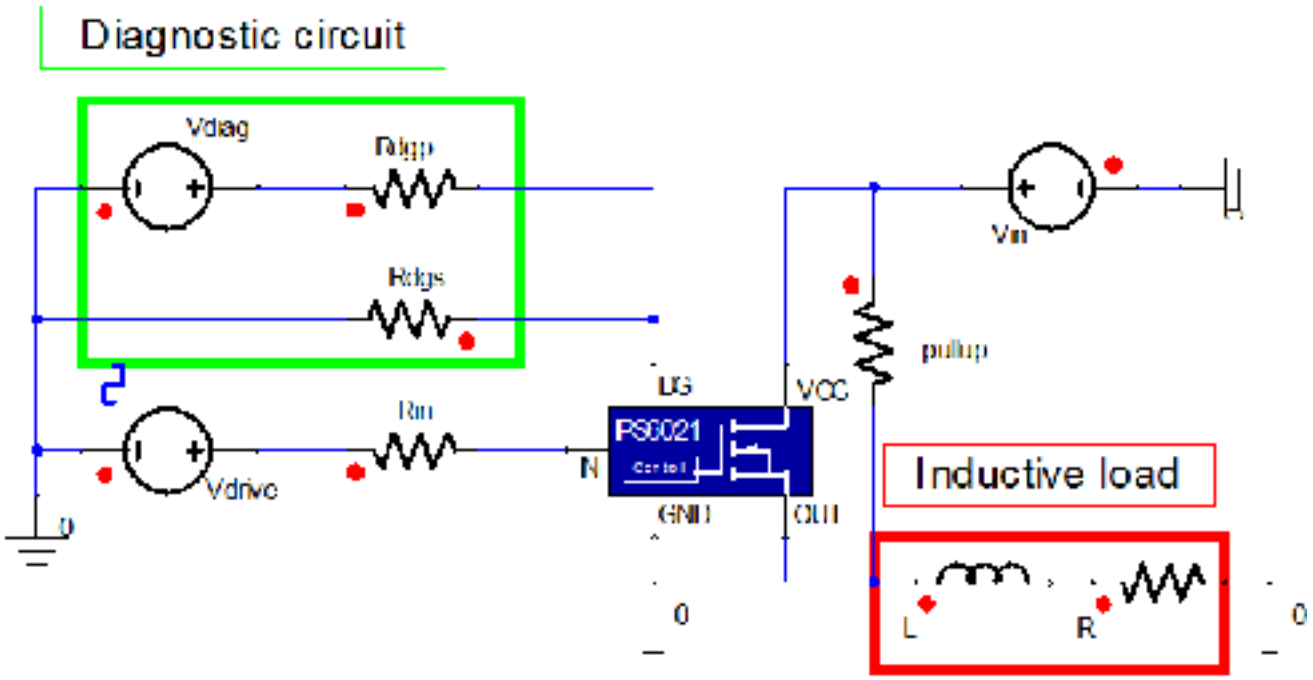

Figure 4. Example Circuit

This low side switch is used here to feed an inductive load. This kind of load allows us to check the steady operation and the current limitation system.

Simulation results :

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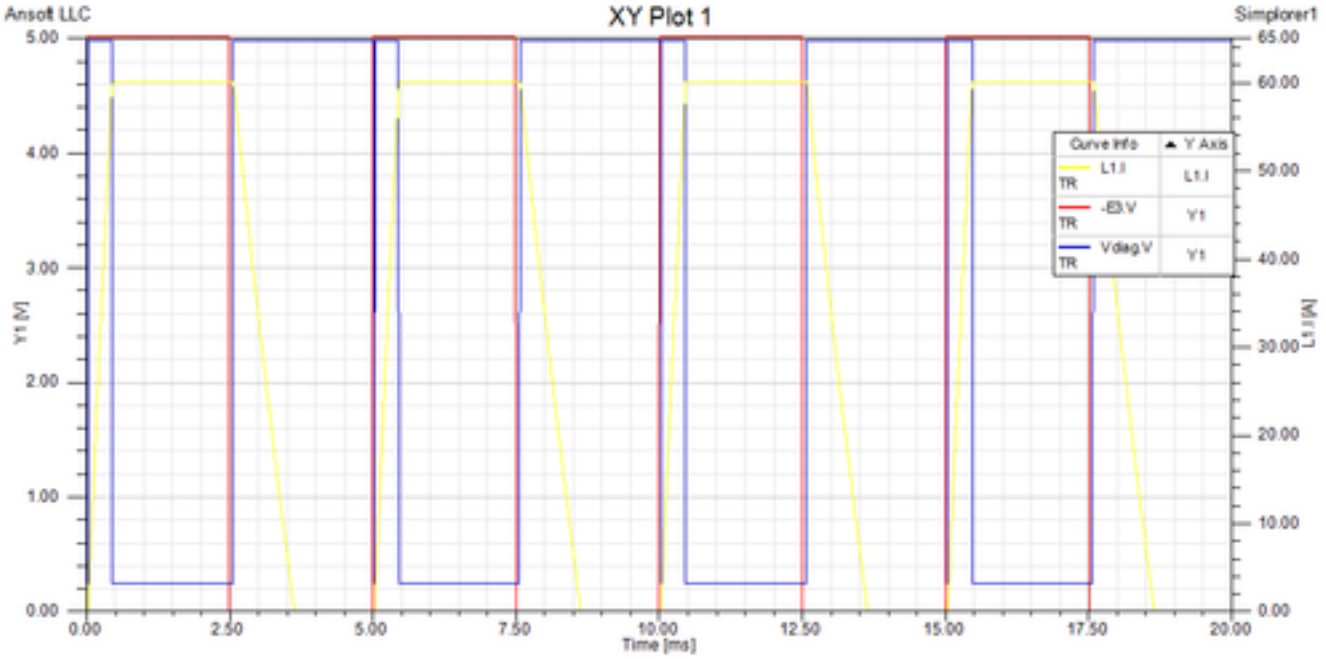

Yellow: load current

Red: input voltage

Blue: diagnostic voltage

Figure 5. Simulation results

When the load current reaches the current limit, is clamped to this value. Then, the diagnosis voltage falls to its low value.

Detail of timing implementation:

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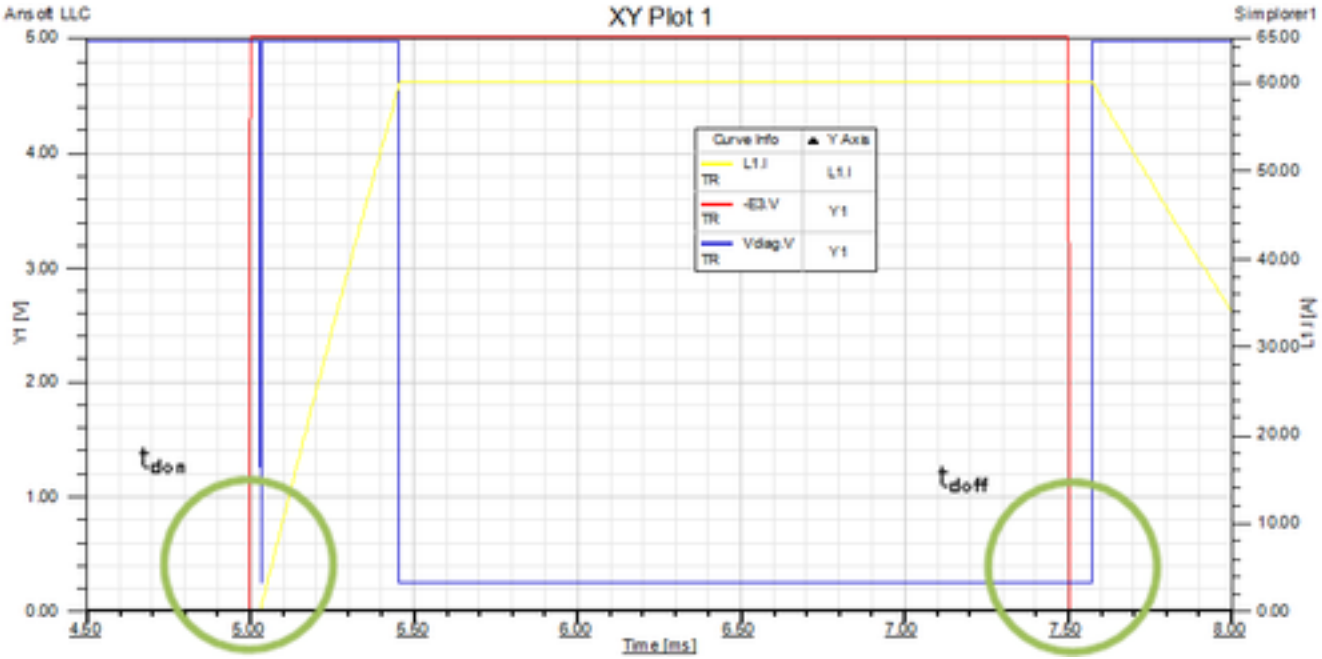

Yellow: load current

Red: input voltage

Blue: diagnostic voltage

Figure 6. Detail of timing implementation

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References

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IPS6031: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

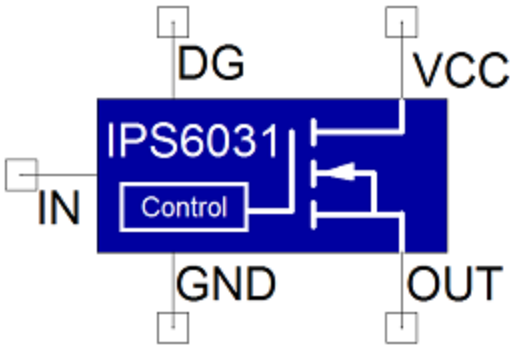

Figure 1. Component symbol

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Description

The *IPS6031* is a five terminal Intelligent Power Switch (IPS) for use in a high side configuration. It features short circuit, inductive load capability and diagnostic feedback. The output current is limited to the Ilimit value. A diagnostic pin provides different voltage levels for each fault condition. The double level shifter circuitry will allow large offsets between the logic and load ground.

The model has four parts. The first one models the input voltage limitation and measures it. The left-up one models the diagnosis voltage with an ideal switch and a zener diode. The main part models the MOSFET with an ideal switch and a variable impedance which allows to model the Rdson and the current limit. The last part is a state machine which controls the main switching and its delays.

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Conservative Pins

Table 1

Symbol	Description
IN	Control signal
VCC	MOSFET drain
OUT	MOSFET source
DG	Diagnostic signal
GND	Logic ground

Product summary:

Table 2

Rds (on)	60mΩ (max.)
Vclamp	39V
I Limit	16A (typ.)
Open load	3V / 0.55A

Table 3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdon	Turn-on delay time		8	25	µs
Tr1	Rise time to Vout=Vcc-5V		5	20	
Tr2	Rise time to		8	35	

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Tdoff	Turn-off delay time		20	45	
Tf	Fall time to Vout=0.1 x Vcc		9	30	
F max.	Max. switch-ing frequency			2.5	kHz

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Parameters

Comparison between model and real component.

The model matches the real model parameters concerning switching delays (ton and toff), maximum current, voltage clamp and conduction resistance as they appear in the product summary section.

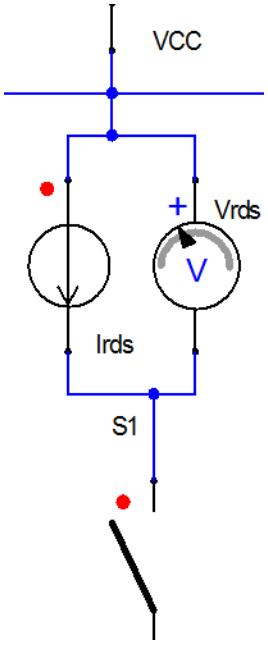

Figure 2. Partial View of the Block Diagram

Conduction resistance has been modeled with a current source in parallel with a voltmeter. This way we can achieve resistive impedance until the output current reaches the Ilimit value (16 A) from which the current is constant and equal to this value:

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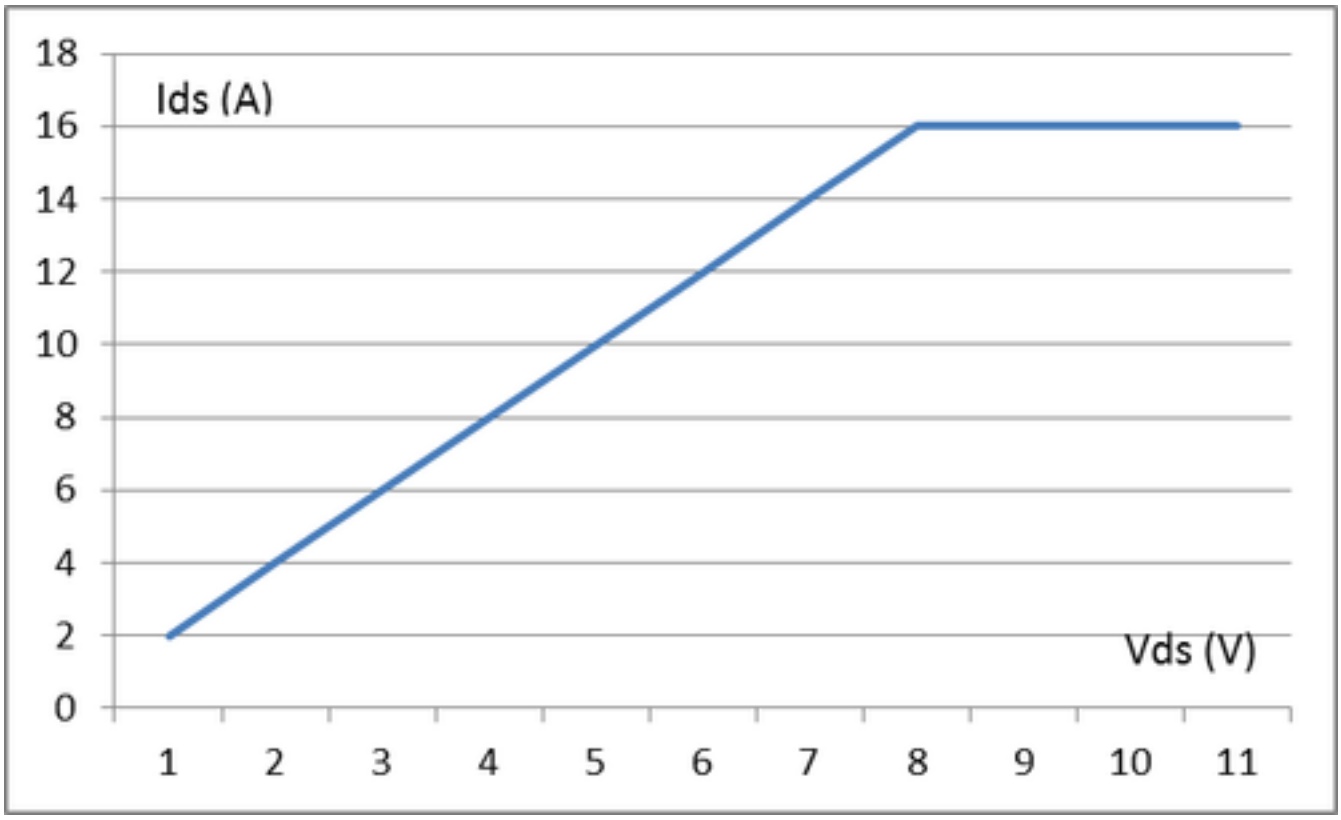

Figure 3. Conduction Resistance Curve

Input impedance is 150 kOhm. Input voltage is limited to 6 V by a zener diode. Temperature influence parameters have not been implemented.

Static Electrical Characteristics:

Tj=25°C, Vcc=14V (unless otherwise specified)

Table 4

Symbol	Parameter	IPS6031	MODEL	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	46	60	mΩ	Vin=5V, Iout=5A
	ON state resistance Tj=150°C	83	60		Vin=5V, Iout=5A
	ON state resistance Tj=25°C, Vcc=6V	55	60		Vin=5V, Iout=2.5A

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	ON state resistance during reverse bat-tery	60	60		Vcc-Gnd=14V
Vcc op.	Operating voltage range with short circuit protection	6-28	X		
V clamp 1	Vcc to Out clamp voltage 1	39	39		Iout=30mA
V clamp 2	Vcc to Out clamp voltage 2	40	40	V	Iout=4A
Icc Off	Supply cur-rentwhen Off	4	X	µA	Vin=0V, Vout=0V
Icc On	Supply cur-rentwhen On	2.2	X	mA	Vin=5V
Vih	Input high threshold voltage	2.5	2.5		
Vil	Input low threshold voltage	2	2		
In hyst.	Input hys-teresis	0.5	X	V	
Iin On	Input cur-rent when device is On	40	80	µA	Vin=5V
Idg	Dg leakagecur-rent	0.1	0		Vdg=5V
Vdg	Low level DG voltage	0.25	0.25	V	Idg=1.6mA

X: not implemented

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Input/Output Quantities

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Examples

Example circuit :

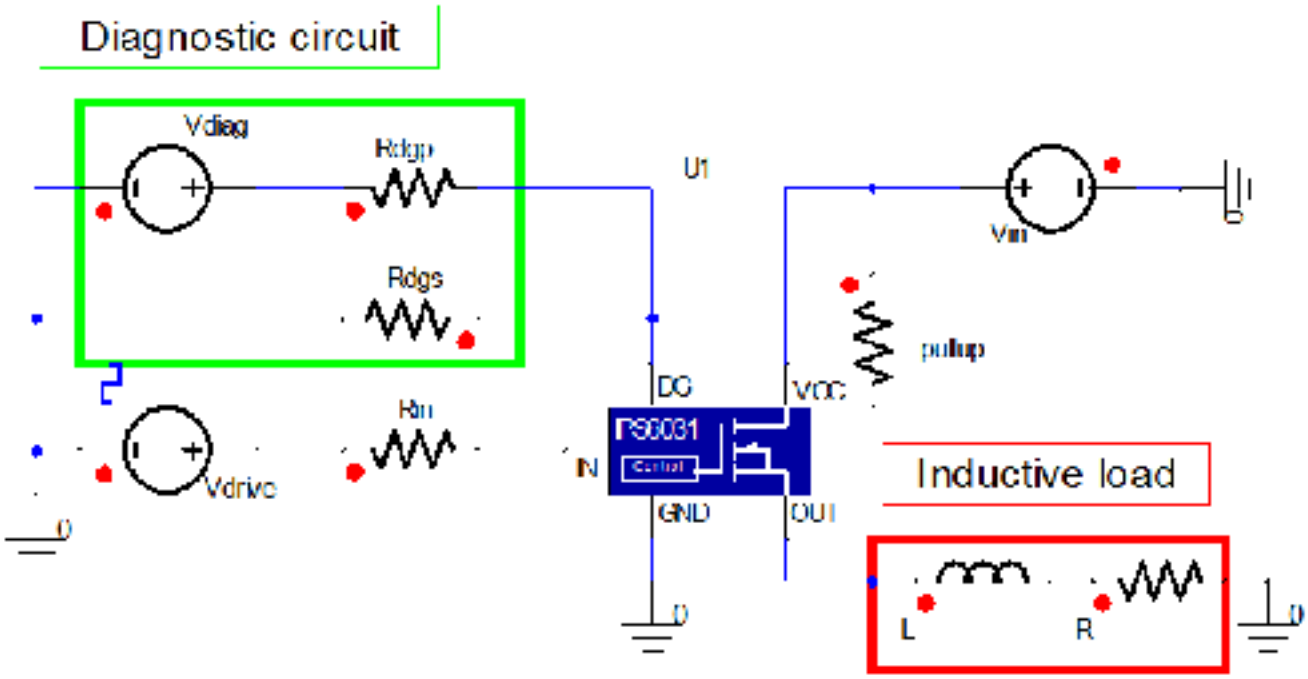

Figure 4. Example Circuit

This low side switch is used here to feed an inductive load. This kind of load allows us to check the steady operation and the current limitation system.

Simulation results :

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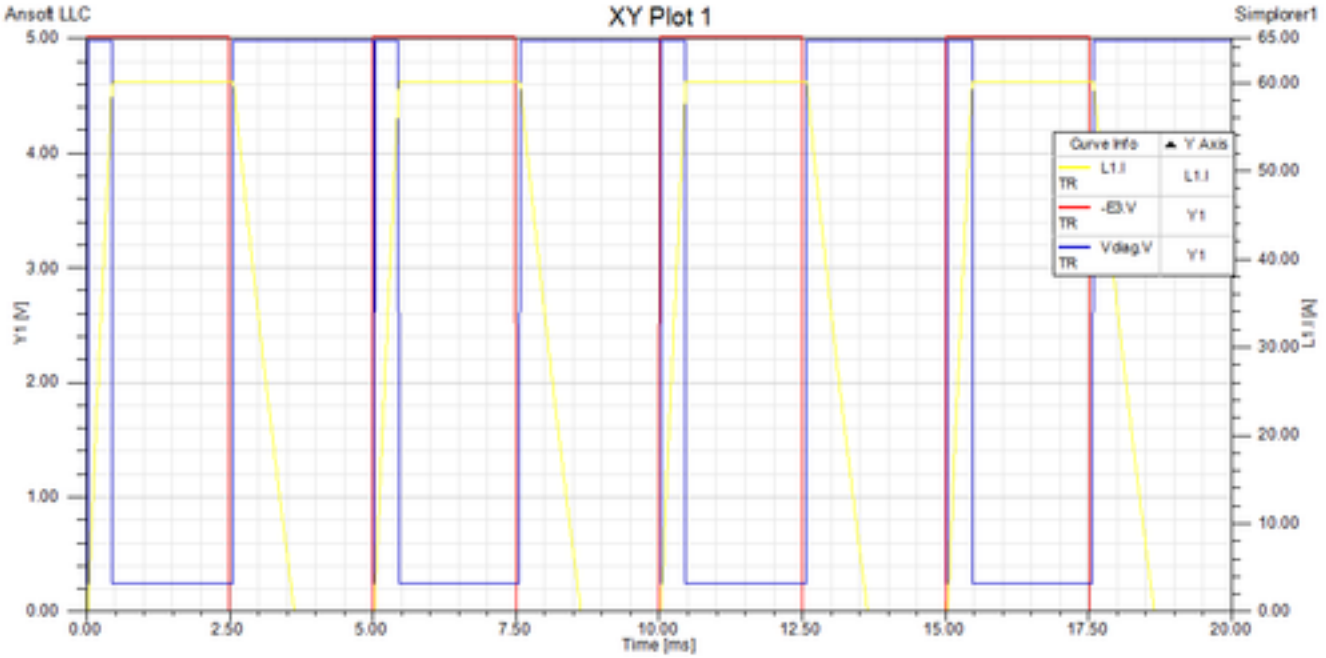

Yellow: load current

Red: input voltage

Blue: diagnostic voltage

Figure 5. Simulation results

When the load current reaches the current limit, is clamped to this value. Then, the diagnosis voltage falls to its low value.

Detail of timing implementation:

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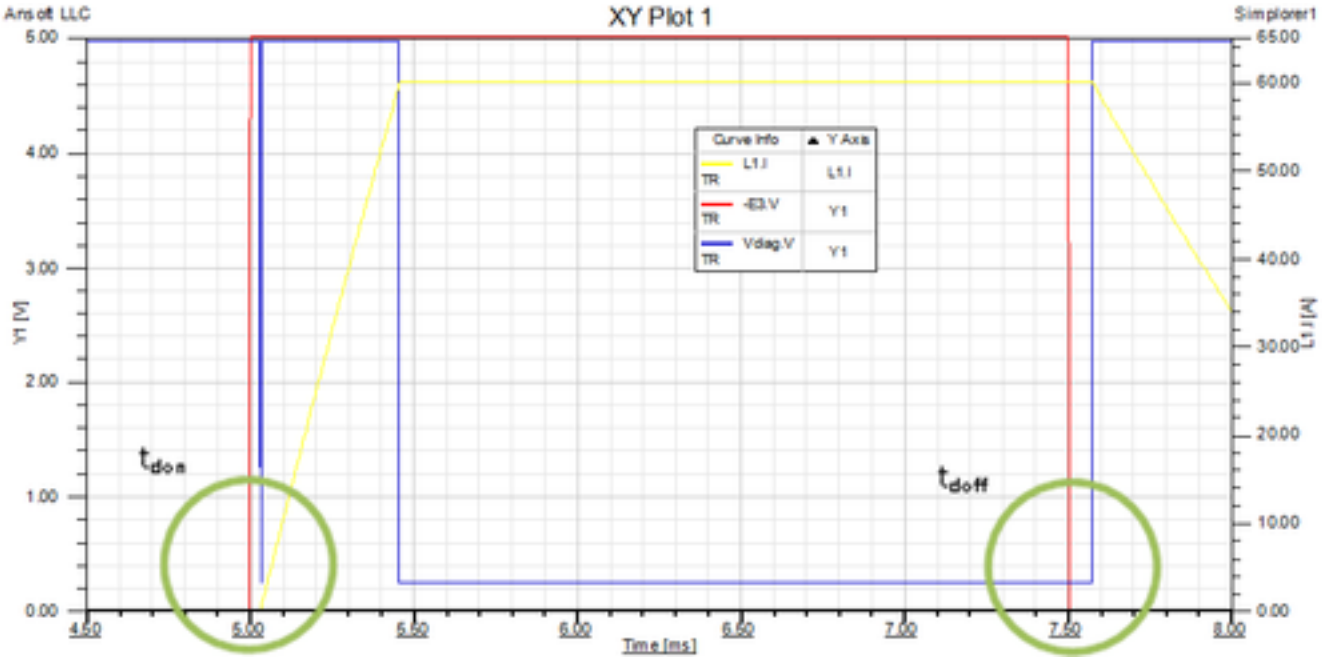

Yellow: load current

Red: input voltage

Blue: diagnostic voltage

Figure 6. Detail of timing implementation

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References

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IPS6041: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

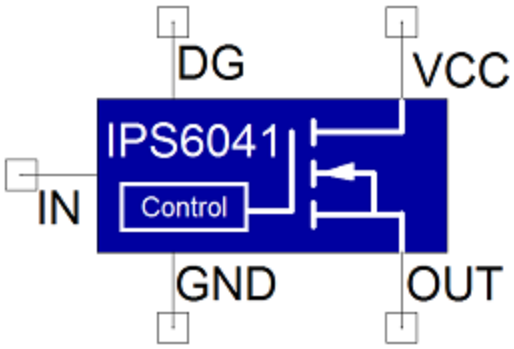

Figure 1. Component symbol

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Description

The *IPS6041* is a five terminal Intelligent Power Switch (IPS) for use in a high side configuration. It features short circuit, inductive load capability and diagnostic feedback. The output current is limited to the Ilimit value. A diagnostic pin provides different voltage levels for each fault condition. The double level shifter circuitry will allow large offsets between the logic and load ground.

The model has four parts. The first one models the input voltage limitation and measures it.The left-up one models the diagnosis voltage with an ideal switch and a zener diode. The main part models the MOSFET with an ideal switch and a variable impedance which allows to model the Rdson and the current limit. The last part is a state machine which controls the main switching and its delays.

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Conservative Pins

Table 1

Symbol	Description
IN	Control signal
VCC	MOSFET drain
OUT	MOSFET source
DG	Diagnostic signal
GND	Logic ground

Product summary:

Table 2

Rds (on)	130mΩ (max.)
Vclamp	39V
I Limit	7A (typ.)
Open load	3V / 0.22A

Table 3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdon	Turn-on delay time		5	15	µs
Tr1	Rise time to Vout=Vcc-5V		3	10	
Tr2	Rise time to Vout=0.9 x		4	20	

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Tdoff	Turn-off delay time		10	20	
Tf	Fall time to Vout=0.1 x Vcc		3	10	
F max.	Max. switch-ing frequency			3.5	kHz

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Parameters

Comparison between model and real component.

The model matches the real model parameters concerning switching delays (ton and toff), maximum current, voltage clamp and conduction resistance as they appear in the product summary section.

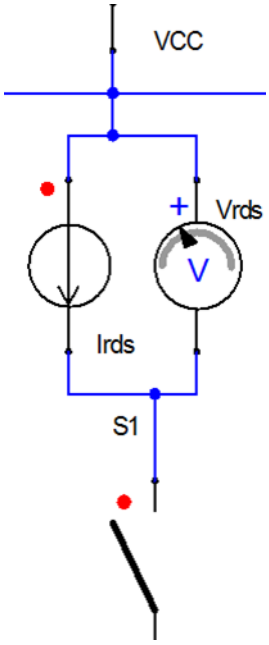

Figure 2. Partial View of the Block Diagram

Conduction resistance has been modeled with a current source in parallel with a voltmeter. This way we can achieve resistive impedance until the output current reaches the Ilimit value (7 A) from which the current is constant and equal to this value:

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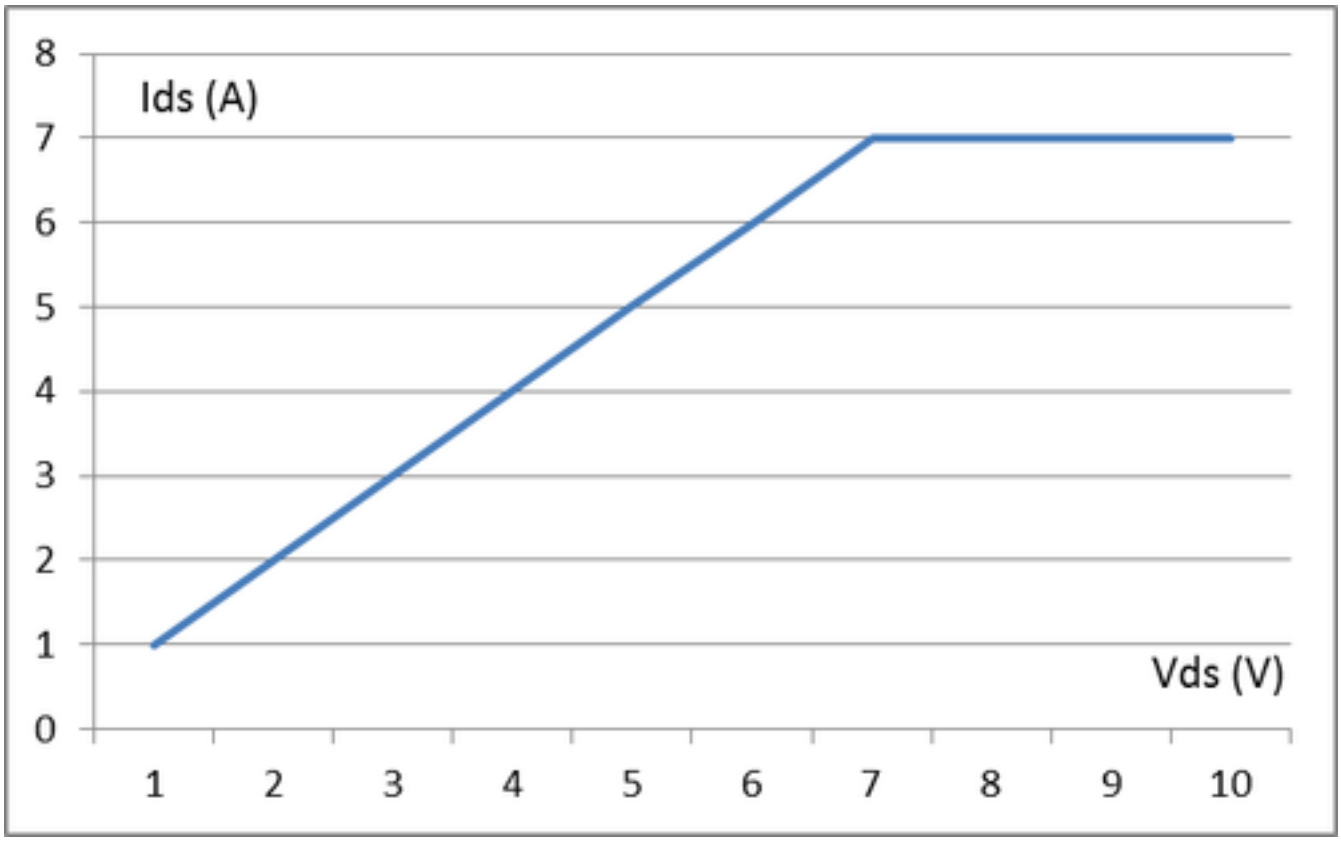

Figure 3. Conduction Resistance Curve

Input impedance is 150 kOhm. Input voltage is limited to 6 V by a zener diode. Temperature influence parameters have not been implemented.

Static Electrical Characteristics:

Tj=25°C, Vcc=14V (unless otherwise specified)

Table 4

Symbol	Parameter	UPS6011	MODEL	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	110	130	mΩ	Vin=5V, Iout=2.5A
	ON state resistance Tj=150°C	190	230		Vin=5V, Iout=2.5A
	ON state resistance Tj=25°C,	125	155		Vin=5V, Iout=1.5A

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	Vcc=6V				
	ON state resistance during reverse battery	140	180		Vcc-Gnd=14V
Vcc op.	Operating voltage range with short circuit protection	6-28	X		
V clamp 1	Vcc to Out clamp voltage 1	39	39		Iout=20mA
V clamp 2	Vcc to Out clamp voltage 2	40	40	V	Iout=2.5A
Icc Off	Supply currentwhen Off	4	X	µA	Vin=0V, Vout=0V
Icc On	Supply currentwhen On	2.2	X	mA	Vin=5V
Vih	Input high threshold voltage	2.5	2.5		
Vil	Input low threshold voltage	2	2		
In hyst.	Input hysteresis	0.5	X	V	
Iin On	Input current when device is On	40	80	µA	Vin=5V
Idg	Dg leakagecurrent	0.1	0		Vdg=5V
Vdg	Low level DG voltage	0.25	0.25	V	Idg=1.6mA

X: not implemented

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Examples

Example circuit :

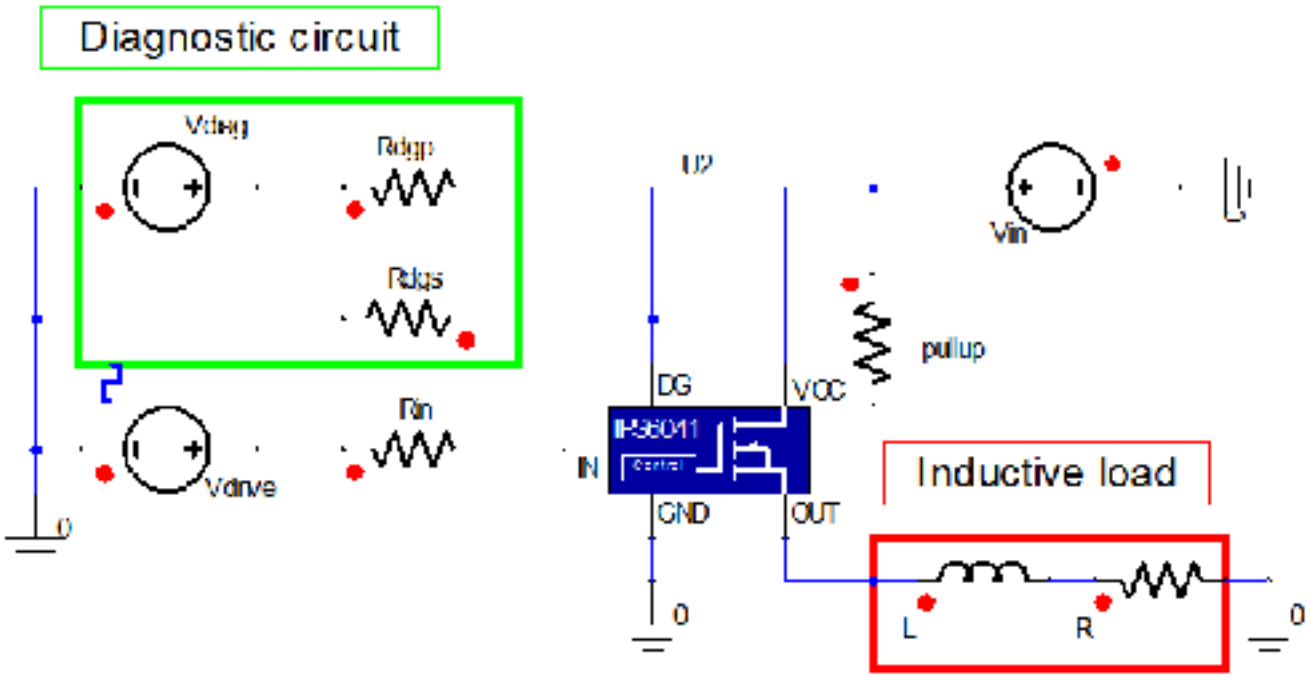

Figure 4. Example Circuit

This low side switch is used here to feed an inductive load. This kind of load allows us to check the steady operation and the current limitation system.

Simulation results :

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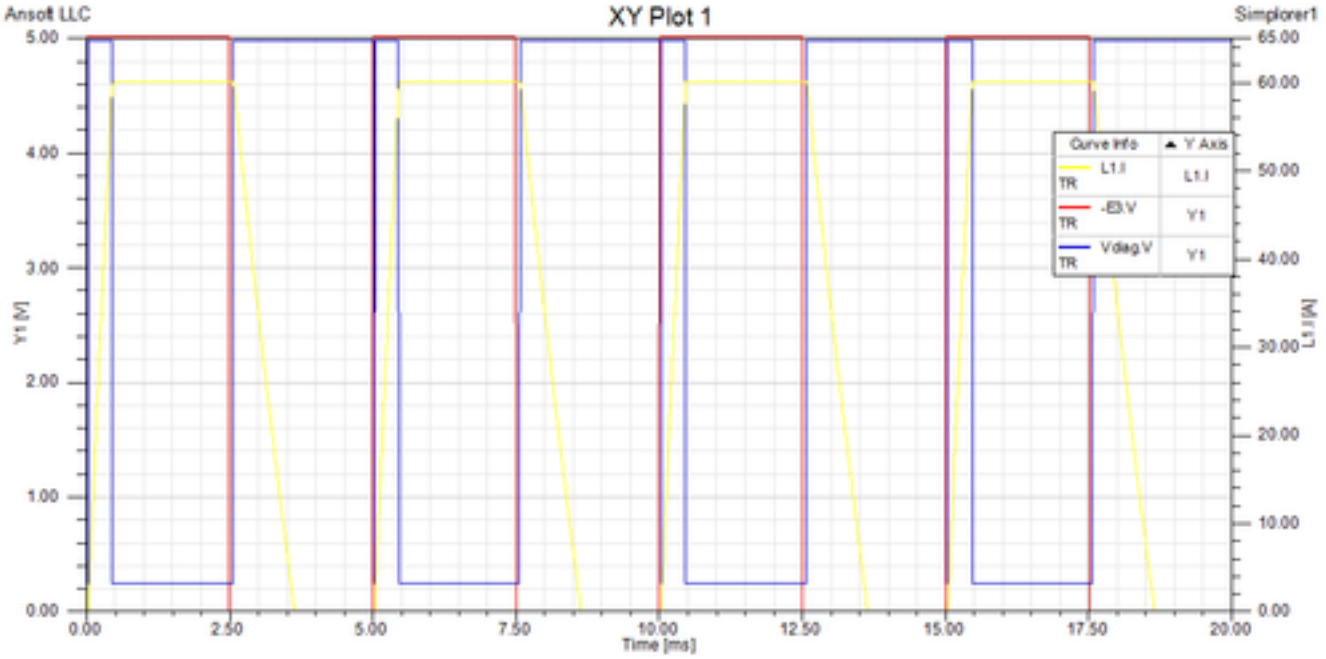

Yellow: load current

Red: input voltage

Blue: diagnostic voltage

Figure 5. Simulation results

When the load current reaches the current limit, is clamped to this value. Then, the diagnosis voltage falls to its low value.

Detail of timing implementation:

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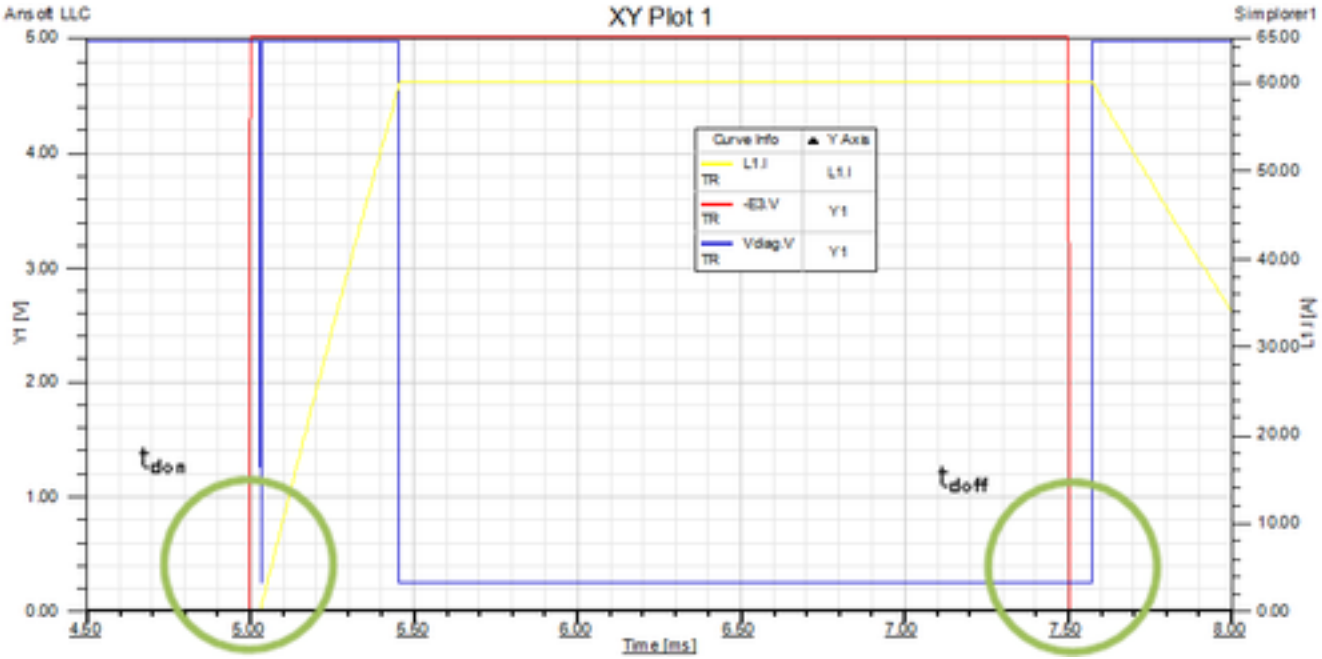

Yellow: load current

Red: input voltage

Blue: diagnostic voltage

Figure 6. Detail of timing implementation

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References

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Linear Regulators

The Linear Regulators consist of the following types of models:

- UCx832
- UCx833
- UCx834
- UCx835
- UCx836

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UCx832: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

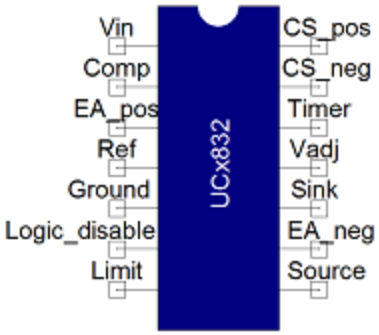

Figure 1. Component symbol

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Description

The *UC2832* and *UC3833* series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. The constant-current-limit is programmable on the *UCx832* to allow higher peak current during the on-time of the pass device. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

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These IC's include a 2 Volt (±1%) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

The model consists of a bipolar transistor that supplies the current to the external pass device base junction. The transconductance operational amplifiers are modeled by controlled current source. An internal logic limits the current supplied by the Voltage amplifier. Two set of state machines controls the Under Voltage Lock Out.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	Vin	SupplyVoltage
2	Comp /Shutdown	Compensation and Shutdown
3	E/A (+)	Error Amplifier (positive)
4	+2V REF R	Voltage Reference
5	Gnd	Ground
6	Logic Disable	LogicDisable
7	Limit	Driver Limit
8	CurrentSense (+)	Current Sense Amplifier (positive) (positive)
9	CurrentSense (-)	Current Sense Amplifier (negative)
10	Timer RC	TimerFunction
11	Vadj	AdjustFunction
12	Sink	Driver Sink

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13	E/A (-)	Error Amplifier (negative)
14	Source	Driver Source

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Parameters

Comparison between model and real component.

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Table 2

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Input Supply						
Supply Current	$+V_{IN}$= 6 V		6.5	10	6.5	mA
	$+V_{IN}$= 36 V		9.5	15	9.5	mA
	Logic Disable = 2 V		3.3		3.3	mA
Reference Section						
Output Voltage	T_J = 25°C, I_{DRIVER} = 10 mA	1.98	2.00	2.02	2	V
Load Regulation	I_O = 0 to 10 m	-10	-5.0		-5	mV
Line Regulation	V_{IN}=4.5V to 36V, I_{DRIVER}=10 mA		0.03-3	0.5	0	mV/V
UVLO Threshold			3.6	4.5	3.6	V
Logic Disable Input						
Threshold Voltage		1.3	1.4	1.5	1.4	V
Input Bias Current	Logic Disable = 0 V	-5	-1		-1	uA
Current SenseSection						
Comparator Offset		95	100	105	100	mV
Amplifier Offset	V_{ADJ} >= 2.1 V	110	135	170	135	mV
	V_{ADJ} = 1 V	180	235	290	236	mV
	V_{ADJ} = 0 V	250	305	360	305	mV
Input BiasCurrent	V_{CM} = $+V_{IN}$	65	100	135	0	uA
Input Offset Current	V_{CM} = $+V_{IN}$	-10		10	0	uA
Amplifier CMRR	V_{CM} = 4.1 V to $+V_{IN}$ + 0.3		80		-	dB
Transconductance	I_{COMP} = +-100 uA		65		65	mS
Vadj Input Current	V_{ADJ} = 0 V	-10	-1		0	uA
Timer						
Inactive Leakage Current	C/S(+) = C/S(-) = $+V_{IN}$; TRC pin = 2 V		0.25	1	0	uA

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Active Pull-up Current	C/S(+)= $+V_{IN}$; C/S(-) = $+V_{IN}$ - 0.4 V ; TRC pin = 0 V	-345	-270	-175	-270	uA
Duty Ratio	Ontime/period, R_T= 200k, C_T = 0.27uF		4.8		2.3	%
Period	Ontime + period, R_T= 200k, C_T=0.27uF		36		38	mS
Upper Trip Threshold (Vu)			1.8		1.8	V
Lower Trip Threshold (Vl)			0.9		0.9	V
Trip Threshold Ratio	Vu/Vl		2.0		2.0	V/V
Error Amplifier						
Input Offset Voltage	V_{CM} = V_{COMP} = 2 V	-8.0		8.0	0	mV
Input BiasCurrent	V_{CM} = V_{COMP} = 2 V	-4.5	-1.1		0	uA
Input Offset Current	V_{CM} = V_{COMP} = 2 V	-1.5		1.5	0	uA
AVOL	V_{COMP} = 1 V to 13 V	50	70		60	dB
Transcon-ductance	I_{COMP} = +- 10 uA		4.3		4.3	mS
VOH	I_{COMP} = 0		0.95	1.3	-	V
VOL	I_{COMP} = 0		0.45	0.7	-	V
IOH	V_{COMP} = 2 V	-700	-500	-100	-	uA
IOL	V_{COMP} = 2 V ; C/S(-) = $+V_{IN}$	100	500	700	-	uA
	V_{COMP}=2V; C/S(-)= $+V_{IN}$ - 0.4V	2	6		-	uA
PARAMET-ER	**TEST CONDITIONS**	**MI-N**	**TY-P**	**MA-X**	**MOD-EL**	**UNI-TS**
Driver						
Maximum Current	Driver Limit & Source pins com-mon; T_J= 25°C	200	300	400	300	mA

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Limiting Voltage	Driver limit to Source voltage at current limit I_{SOURCE}= -10mA; T_J = 25°C		0.72		0.7	V
Internal Cur-rentSense Resistance	T_J = 25°C		2.4		2.4	ohm
Pull-up Cur-rent at Driver Sink	Com-pens-ation/Shutdown = 0.4 V ; Driver Sink = +V_{IN} - 1 V	-800	-300	-100	0	uA
	Com-pens-ation/Shutdown = 0.4 V ; +V_{IN} = 36 V; Driver Sink= 35 V	-100-0	-300	-75	0	uA
Pull-Down Current at Driver Source	Com-pens-ation/Shutdown = 0.4 V ; Driver Source = 1 V	150	300	700	0	uA
Saturation Voltage Sink to Source	Driver Source = 0 V ; Driver Cur-rent Source = 100 A		1.5		1.25	V
Maximum Source Voltage	Driver Sink = +V_{IN}, Driver Cur-rent = 100 mA		3.0		2.5	V
UVLO Sink Leakage	+V_{IN} =C/S(+) =C/S(-) =2.5 V ; Driver Sink = 15 V ; Driver Source = 0 V; TA = 25°C		2.5		0	uA
Maximun Reverse Source Voltage	Com-pens-ation/Shutdown = 0 V ; I_{SOURCE} = 100 uA ; +V_{IN} = 3 V		1.6		0.3	V
Thermal Shutdown			160		X	°C

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Note 4: These parameters are first-order supply-independent, however both may vary with supply for +VIN less than about 4 V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.

*Note 5: With recommended RT value of 200k, TOFF » RT CT * ln(Vu/Vl) ±10%.*

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Example circuit :

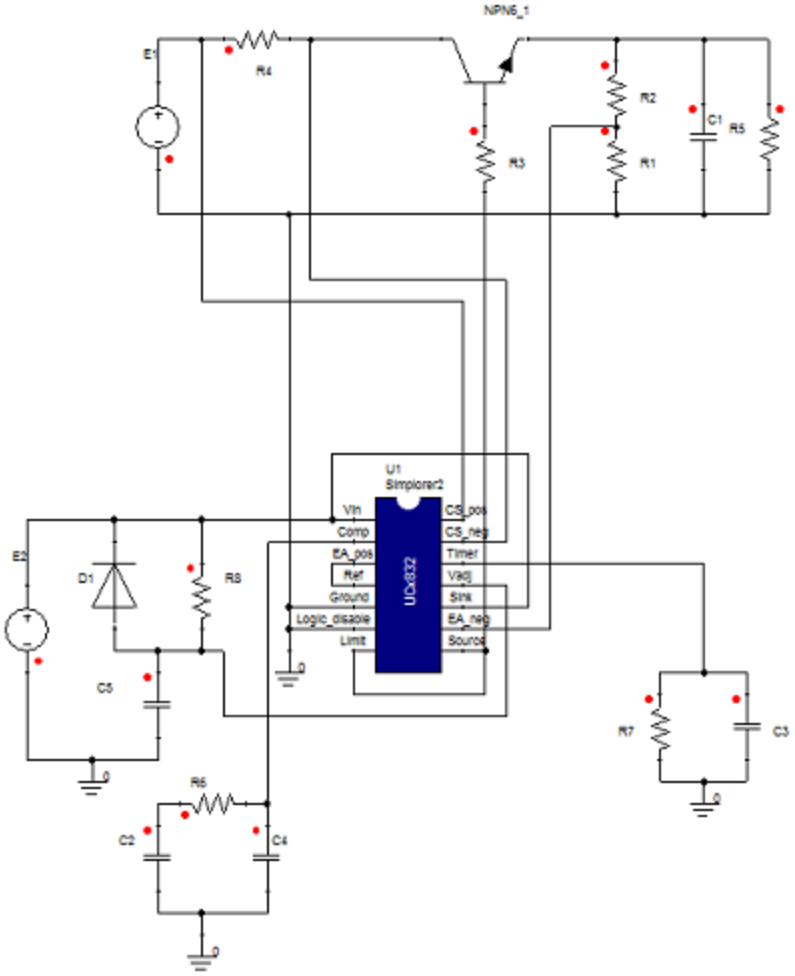

Figure 2. Example Circuit

Simulation results :

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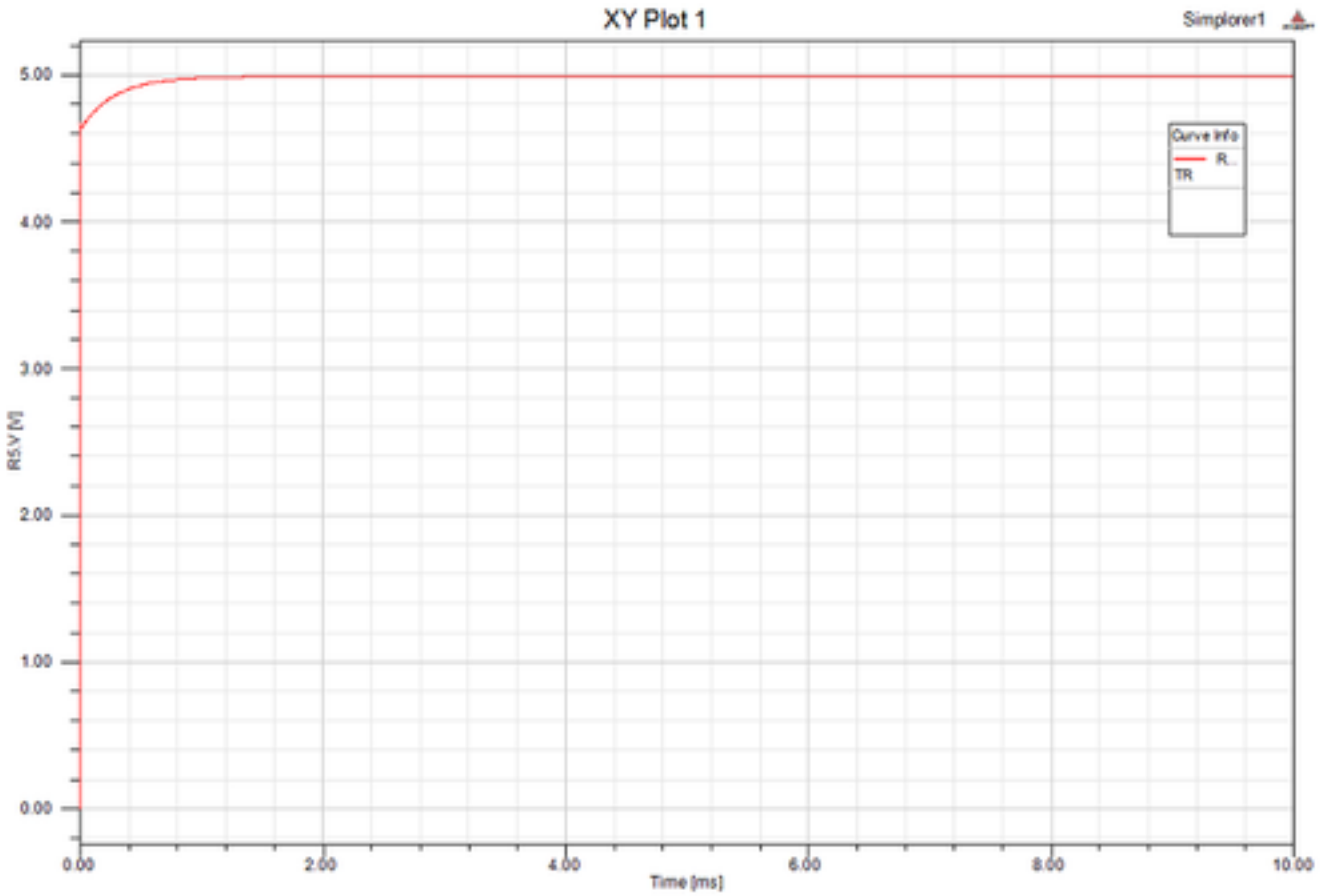

Figure 3. Simulation results

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References

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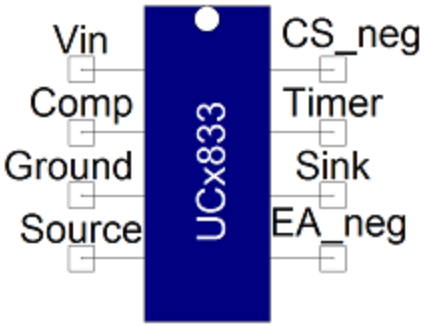
UCx833: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UC2832* and *UC3833* series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

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These IC's include a 2 Volt (±1%) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

The *UC3833* family includes the basic functions of this design in a low-cost, 8- pin mini-dip package, while the *UC2832* series provides added versatility with the availability of 14 pins. Packaging options include plastic (N suffix), or ceramic (J suffix). Specified operating temperature ranges are: commercial (0°C to 70°C), order *UC3832/3* (N or J); and industrial (-40°C to 85°C), order *UC2832/3* (N or J). Surface mount packaging is also available.

The model consist of a Darlington pair between Sink and Source pins. The transconductance operational amplifiers are modeled by controlled current sources. Two set of state machines controls the Overvoltage and Timer protection.

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Table 1

PIN	NAME	FUNCTION
1	Vin & C/S (+)	SupplyVoltage
2	Comp /Shutdown	Compensation and Shutdown
5	Gnd	Ground
4	Source	Driver Source
5	E/A (-)	Error Amplifier (negative)
6	Sink	Driver Sink
7	Timer RC	TimerFunction
8	CurrentSense (-)	Current Sense Amplifier (negative)

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Parameters

Comparison between model and real component.

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Table 2

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Input Supply						
Supply Current	$+V_{IN}$= 6 V		6.5	10	6.5	mA
	$+V_{IN}$= 36 V		9.5	15	9.5	mA
Reference Section						
Output Voltage	T_J = 25°C, I_{DRIVER} = 10 mA	1.98	2.00	2.02	2	V
Line Regulation	$+V_{IN}$= 4.5 V to 36 V, I_{DRIVER} = 10 mA		0.033	0.5	0	mV/V
Under-Voltage Lokout Threshold			3.6	4.5	3.6	V
Current Sense Section						
Comparator Offset		95	100	105	100	mV
Amplifier Offset	V_{ADJ} >= 2.1 V	110	135	170	135	mV
Input Bias Current	V_{CM} = $+V_{IN}$	65	100	135	0	uA
Input Offset Current	V_{CM} = $+V_{IN}$	-10		10	0	uA
Transconductance	I_{COMP} = +-100 uA		65		65	mS
Timer						
Inactive Leakage Current	C/S(+) = C/S(-) = $+V_{IN}$; TRC pin = 2 V		0.25	1	0	uA
Active Pullup Current	C/S(+)= $+V_{IN}$; C/S(-) = $+V_{IN}$ - 0.4 V ; TRC pin = 0 V	-345	-270	-175	-270	uA
Duty Ratio	Ontime/period, R_T= 200k, C_T = 0.27 uF		4.8		2.3	%
Period	Ontime + period, R_T= 200k, C_T = 0.27 uF		36		38	mS
Upper Trip Threshold (Vu)			1.8		1.8	V
lower Trip			0.9		0.9	V

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Threshold (Vl)						
Trip Threshold Ratio	Vu/Vl		2.0		2.0	V/V
Error Amplifier						
Input Bias Current	$V_{CM} = V_{COMP} = 2$ V	-4.5	-1.1		0	uA
AVOL	V_{COMP} = 1 V to 13 V	50	70		60	dB
CMRR	V_{CM} = 0V to $+V_{IN}$ - 3V	60	80		-	dB
PSRR	V_{CM} = 2V, $+V_{IN}$ = 4.5 to 36 V		90		-	dB
Transcon-ductance	I_{COMP} = +- 10 uA		4.3		4	mS
VOH	$I_{COMP} = 0$		0.95	1.3	-	V
VOL	$I_{COMP} = 0$		0.45	0.7	-	V
IOH	V_{COMP} = 2 V	-700	-500	-100	-	uA
IOL	V_{COMP} = 2 V ; C/S(-) = $+V_{IN}$	100	500	700	-	uA
	V_{COMP} = 2 V; C/S (-)= $+V_{IN}$ - 0.4 V	2	6		-	uA
Driver						
Maximum Current	Driver Limit & Source pins common; T_J= 25°C	200	300	400	300	mA
Internal Current Sense Resistance	T_J = 25°C		2.4		2.4	ohm
Pull-up Current at Driver Sink	Compensation/Shutdown = 0.4 V ; Driver Sink = $+V_{IN}$ - 1 V	-800	-300	-100	0	uA
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MODEL**	**UNITS**
Pull-up Current at Driver Sink	Compensation/Shutdown = 0.4 V ; $+V_{IN}$ = 36 V; Driver Sink= 35 V	-100-0	-300	-75	0	uA
Pull-Down Current at Driver	Compensation/Shutdown =	150	300	700	0	uA

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Source	0.4 V ; Driver Source = 1 V					
Saturation Voltage Sink to Source	Driver Source = 0 V ; Driver Current Source = 1 V		1.5		1.25	V
Maximum Source Voltage	Driver Sink = $+V_{IN}$, Driver Current = 100 mA		3.0		2.5	V
UVLO Sink Leakage	$+V_{IN}$ =C/S(+) =C/S(-) =2.5 V ; Driver Sink = 15 V ; Driver Source = 0 V; TA = 25°C		2.5		0	uA
Maximun Reverse Source Voltage	Compensation/Shutdown = 0 V ; I_{SOURCE} = 100 uA ; $+V_{IN}$ = 3 V		1.6		0.3	V
Thermal Shutdown			160		X	°C

Note 3: On the UCx833 this voltage is defined as the regulating level at the error amplifier inverting input, with the error amplifier driving VSOURCE to 2 V.

Note 4: These parameters are first-order supply-independent, however both may vary with supply for +VIN less than about 4 V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.

*Note 5: With recommended RT value of 200k, TOFF » RT CT * ln(Vu/Vl) ±10%.*

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Example circuit :

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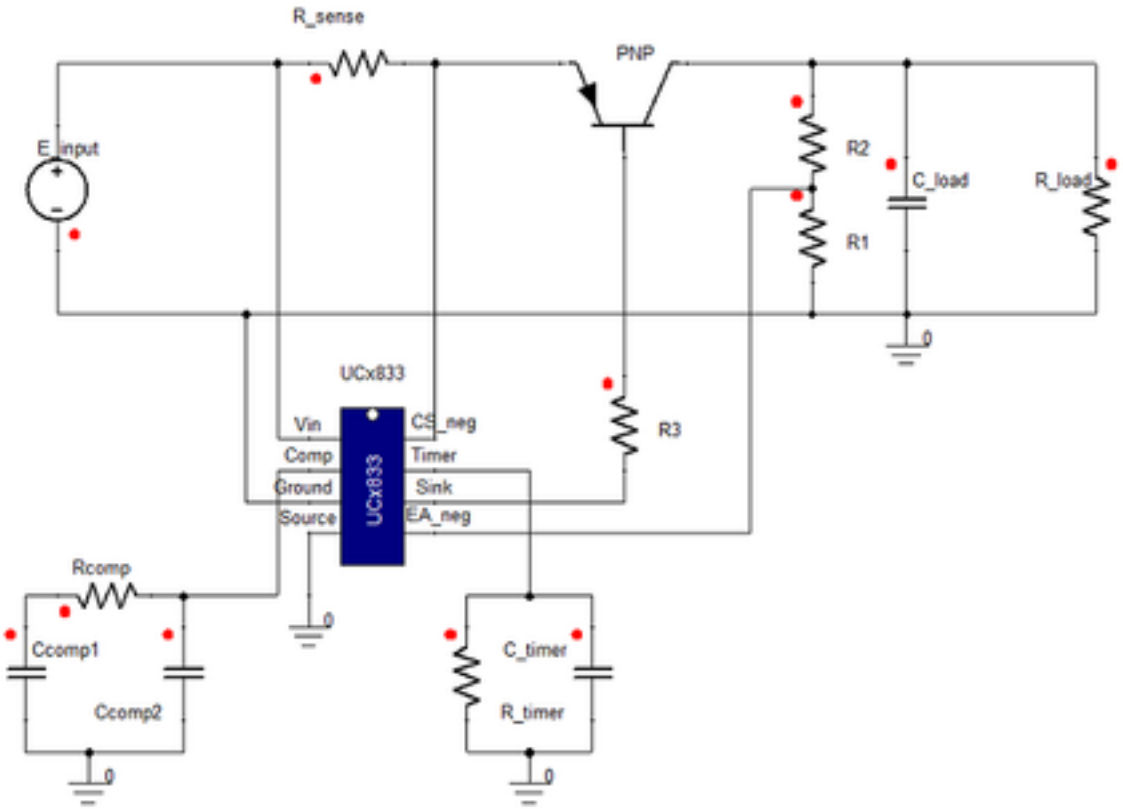

Figure 2. Example Circuit

Simulation results :

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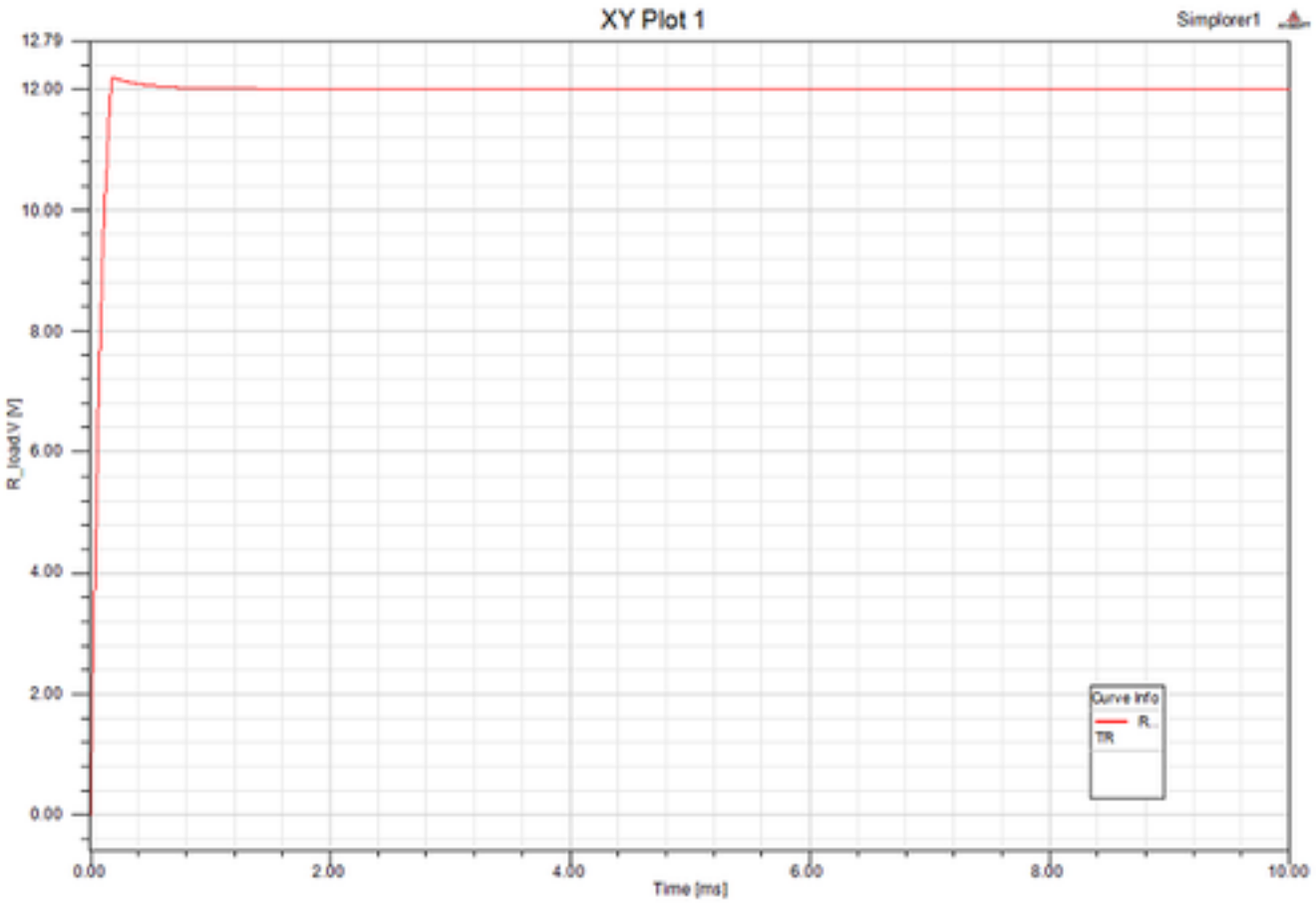

Figure 3. Simulation results

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References

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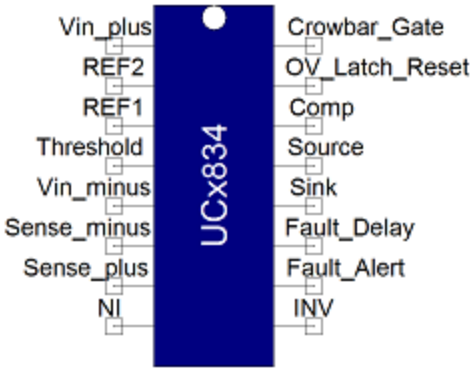
UCx834: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UC1834* family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated.

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An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

The model consists of a Darlington pair between Sink and Source pins, with an additional bipolar transitor to limit the current. The transconductance operational amplifiers are modeled by controlled current sources. Various sets of state machines control the Fault detection, protection logic and delay.

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Conservative Pins

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Table 1

PIN	NAME	FUNCTION
1	Vin+	Input Supply (+)
2	-2V Ref.	-2V Reference
3	-1.5V Ref.	-1.5V Reference
4	Threshold Adj.	Threshold Adjust
5	Vin-	Input Supply (-) orGround
6	Sense(-)	Current Sense Inverting Input
7	Sense(+)	Current Sense non Inverting Input
8	N.Inv.Input	Error Amplifier non Inverting Input
9	Inv. Input	Error Amplifier Inverting Input
10	Fault Alert	Fault Alert
11	Fault Delay	Fault Delay
12	Driver Sink	Driver Sink
13	Driver Source	Driver Source
14	Compensation/Shutdown	Compensation and Shutdown
15	O.V. Latch Output/Reset	Over-Voltage Latch Output and

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		Reset
16	Crowbar Gate	Crowbar gate

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Parameters

Comparison between model and real component.

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Table 2

PARAMET-ER	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
Turn-on Characteristics						
Standby SupplyCur-rent			5.5	10	5.5	mA
+1.5 Volt Reference						
Output Voltage	TJ = 25°C	1.47	1.5	1.53	1.5	V
Line Regu-lation	VIN+ = 5 to 35V		1	15	0	mV
Load Regu-lation	IOUT = 0 to 2mA		1	15	1	mV
-2.0 Volt Reference						
Output Voltage (Referenced to VIN+)		-2.06	-2	-1.94	-2	V
Line Regu-lation	VIN+ = 5 to 35V		1.5	20	0	mV
Output Impedance			2.3		2.3	Ohm
Error AmplifierSection						
Input Offset Voltage	VCM = 1.5V		1	10	0	mV
Input BiasCurrent	VCM = 1.5V		-1	-8	0	uA
Input Offset Current	VCM = 1.5V		0.1	2	0	uA
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = V_{IN+} Pin 13, 20Ω to V_{IN-}	50	65		65	dB
CMRR	VCM = 0.5 to 33V, VIN+ = 35V	90	80		-	dB
PSRR	VIN+ = 5 to 35V, VCM = 1.5V	70	100		-	dB
Driver Section						
Maximum Output Cur-		200	350		350	mA

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rent						
Saturation Voltage	IOUT = 100mA		0.5	1.5	1.15	V
Output Leak-ageCurrent	Pin 12 = 35V, Pin 13 = VIN-, Pin 14 = VIN-		0.1	50	0	uA
Shutdown Input Voltage at Pin 14	IOUT < 100uA, Pin 13 = VIN-, Pin 12 = VIN+	0.4	1		-	V
Shutdown Input Cur-rent at Pin 14	Pin14=VIN-, Pin12-2=VIN+ IOUT<100u-A, Pin 13=VIN-		-100	-150	-	uA
Thermal Shutdown			165		X	°C
Fault AmplifierSection						
Under- and Over-Voltage Fault Threshold	VCM = 1.5V, @ E/A Inputs	110	150	190	150	mV
Common ModeSens-itivity	VIN+ = 35V, VCM = 1.5 to 33V		-0.4	-1	-	%/V
Supply Sens-itivity	VCM = 1.5V, VIN+ = 5 to 35V		0.5	-1.2	-	%/V
PARAMET-ER	**TEST CONDITIO-NS**	**MIN**	**TYP**	**MAX**	**MODE-L**	**UNIT-S**
Fault Delay		30	45	60	45	Ms/uF
Fault Alert Output Cur-rent		2	5		5	mA
Fault AlertSat-uration Voltage	IOUT = 1mA		0.2	0.5	0.2	V
O.V. Latch Output Cur-rent		2	4		0	mA

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O.V. Latch Saturation Voltage	IOUT = 1mA		1.0	1.3	-	V
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	0.4	V
Crowbar GateCurrent		-100	-175		-175	mA
Crowbar GateLeak-ageCurrent	Vin+ = 35V, Pin 16 = Vin		-0.5	-50	0	uA
Current SenseAmplifierSection						
Threshold Voltage	Pin 4 > 1.5 V ; Vcm = Vin+ or Vin-	120	150	180	150	mV
	Pin 4 > 0.5 V ; Vcm = Vin+ or Vin-	30	50	70	50	mV
Threshold SupplySens-itivity	Pin 4 > 1.5 V				0	%/V
Adj. Input Current	Pin 4 > 0.5 V		-2	-10	0	uA
Sense Input BiasCurrent	Vcm = Vin+		100	200	0	uA
	Vcm = Vin-		-100	-200	0	uA

Note 2: When using both the 1.5V and -2.0V references the current out of pin 3 should be balanced by an equivalent current into Pin 2. The -2.0V output will change -2.3mV per µA of imbalance.

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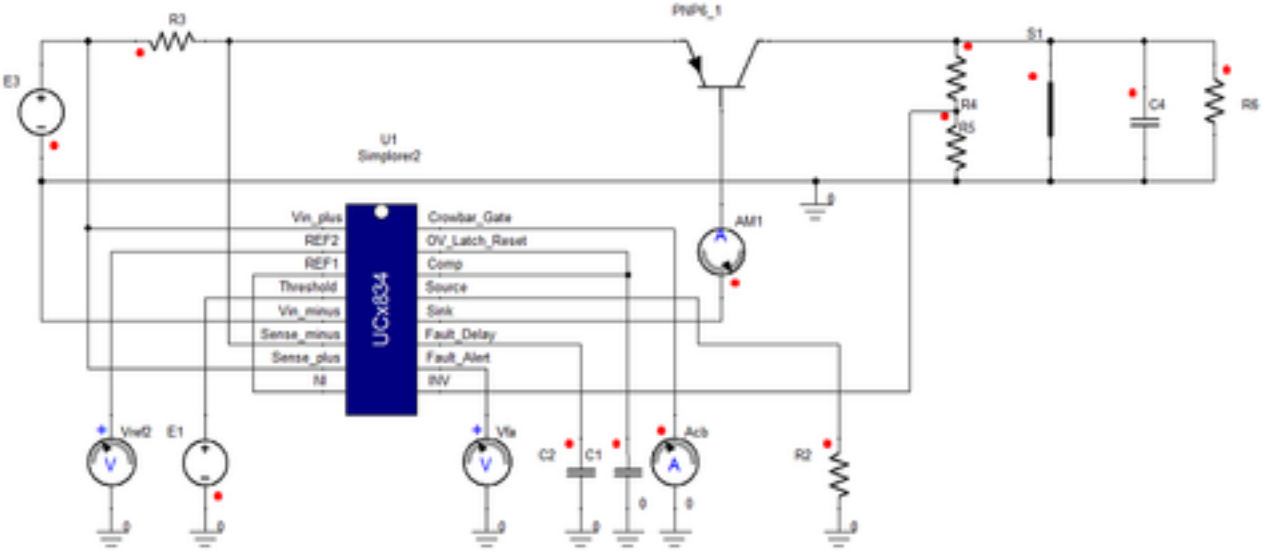

Figure 2. Example Circuit

Simulation results :

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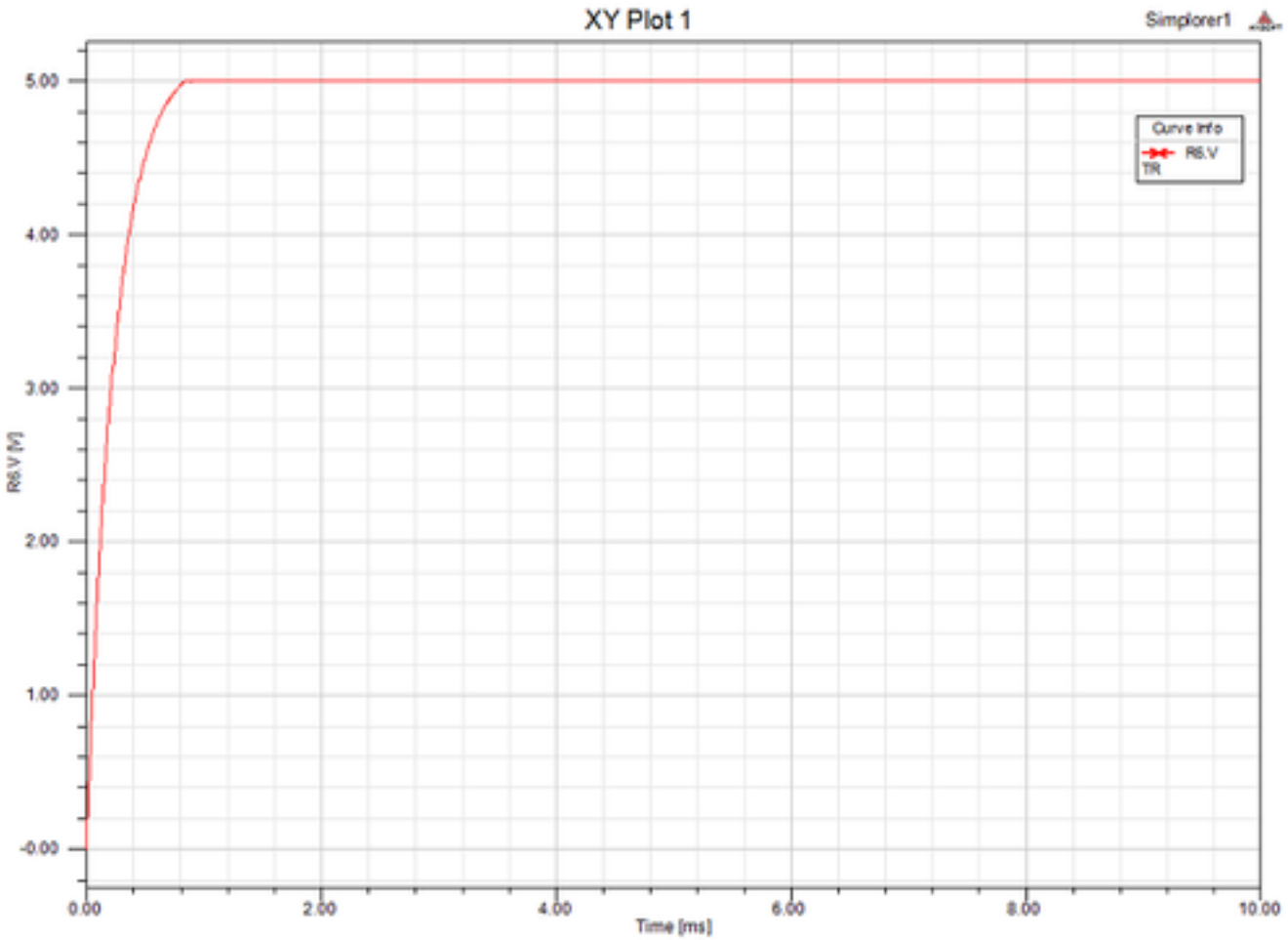

Figure 3. Simulation results

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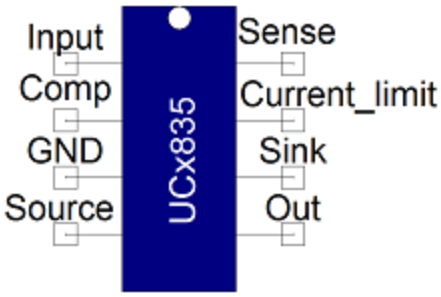
UCx835: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UC1835/6* families of linear controllers are optimized for the design of low cost, low dropout, linear regulators. Using an external pass element, dropout voltages of less than 0.5V are readily obtained.

These devices contain a high gain error amplifier, a 250mA output driver, and a precision reference. In addition, current sense with foldback provides for a 2.5A peak output current dropping to less than 0.5A at short circuit.

These devices are available in fixed, 5V, (*UC1835*), or adjustable, (*UC1836*), versions. In the fixed 5 volt version, the only external parts required are an external pass element, an output capacitor, and a compensation capacitor. On the adjustable version the output voltage can be set anywhere from 2.5V to 35V with two external resistors.

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Additional features of these devices include under-voltage lockout for predictable start-up, thermal shutdown and short circuit current limiting to protect the driver device. On the fixed voltage version, a reverse voltage comparator minimizes reverse load current in the event of a negative input to output differential.

The model consists of a bipolar transistor that supplies the current to the external pass device base junction.

The transconductance operational amplifiers are modeled by controlled current source. An internal logic limits the current supplied by the Voltage amplifier.

Two set of state machines controls the Under Voltage Lock Out and Reverse protection.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	Vin	Positive Supply Voltage
2	Comp	Compensation and Shutdown
3	GND	Ground
4	Source	Driver Source
5	Sense	Sense Resistor Out
6	Current_limit	Current limit
7	Sink	Driver Sink
8	Out	Sense Output Voltage

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Parameters

Comparison between model and real component.

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Table 2

PARAMETER	TEST CONDITIONS	MIN	TYPE	MAX	MODEL	UNITS
Driver						
Maximum Current		250	500		-	mA
Saturation Voltage	Driver Current = 250mA, Driver Sink		2.0	2.8	2	V
Pull-Up Current at Driver Sink	Compensation/Shutdown =0.45V	140	250	300	250	mA
Driver SinkLeakage	In UVLO			10	0	A
	In Reverse Voltage			10	0	A
Thermal Shutdown			165		X	°C
Foldback Current Limit						
Current Limit Levels at Sense Resistor Out	V_{OUT} Sense = (0.99) V_{REG}	2.2	2.5	2.8	2.45	A
	V_{OUT} Sense = (0.5) V_{REG}	1.3	1.5	1.7	1.55	A
	V_{OUT} Sense = 0V	0.25	0.4	0.55	0.5	A
Current Limit Amp Tanscon ductance	100 A at Compensation/ Shutdown, V_{OUT} Sense	12	24	42	240	mS

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	= (0.9) V_{REG}					
Limiting Voltage at Current Limit	V_{OUT} Sense = (0.9) V_{REG} Volts Below $+V_{IN}$, T_J = 25°C	80	100	140	93	mV
Sense Resistor Value	V_{OUT} Sense = (0.9) V_{REG} I_{OUT} = I_A, T_J = 25°C		40		40	mOhm
Input Supply						
Supply Current	$+V_{IN}$ = 6V		2.75	4.0	2.75	mA
	$+V_{IN}$ = 40V		3.75	6.0	3.75	mA
UVLO Threshold	$+V_{IN}$ Low to High, V_{OUT} Sense = 0V	3.9	4.4	4.9	4.4	V
Threshold Hysteresis			0.1	0.35	0.1	V
Reverse Current	$+V_{IN}$ = -1.0V, Driver Sink Open		6.0	20	-	mA
Regulating Voltage and Error Amplifier						
Regulating Level at V_{OUT} Sense (V_{REG})	Driver Current = 10mA, T_J = 25°C	4.94	5.0	5.06	5	V
Line Regulation	$+V_{IN}$ = 5.2V to 35V		15	40	0	mV

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Load Regulation	Driver Current = 0 to 250mA		6.0	25	6	mV
Bias Current at V_{OUT} Sense	V_{OUT} Sense = 5.0V	75	125	210	0	A
Error Amp Transconductance	100 A at Compensation/ Shutdown Pin	0.8	1.3	2.0	1.3	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	-	uA

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Examples

Example circuit :

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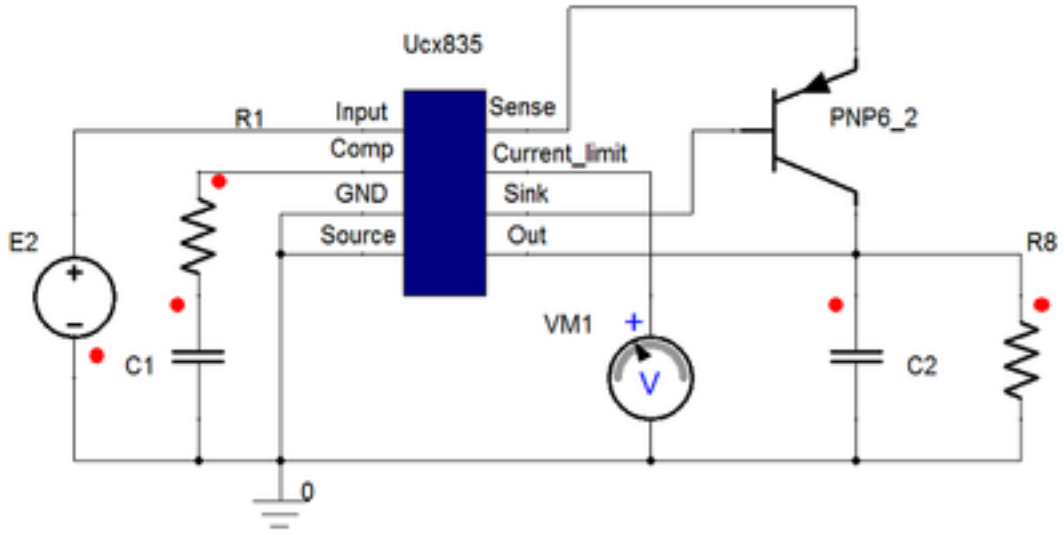

Figure 2. Example Circuit

Simulation results :

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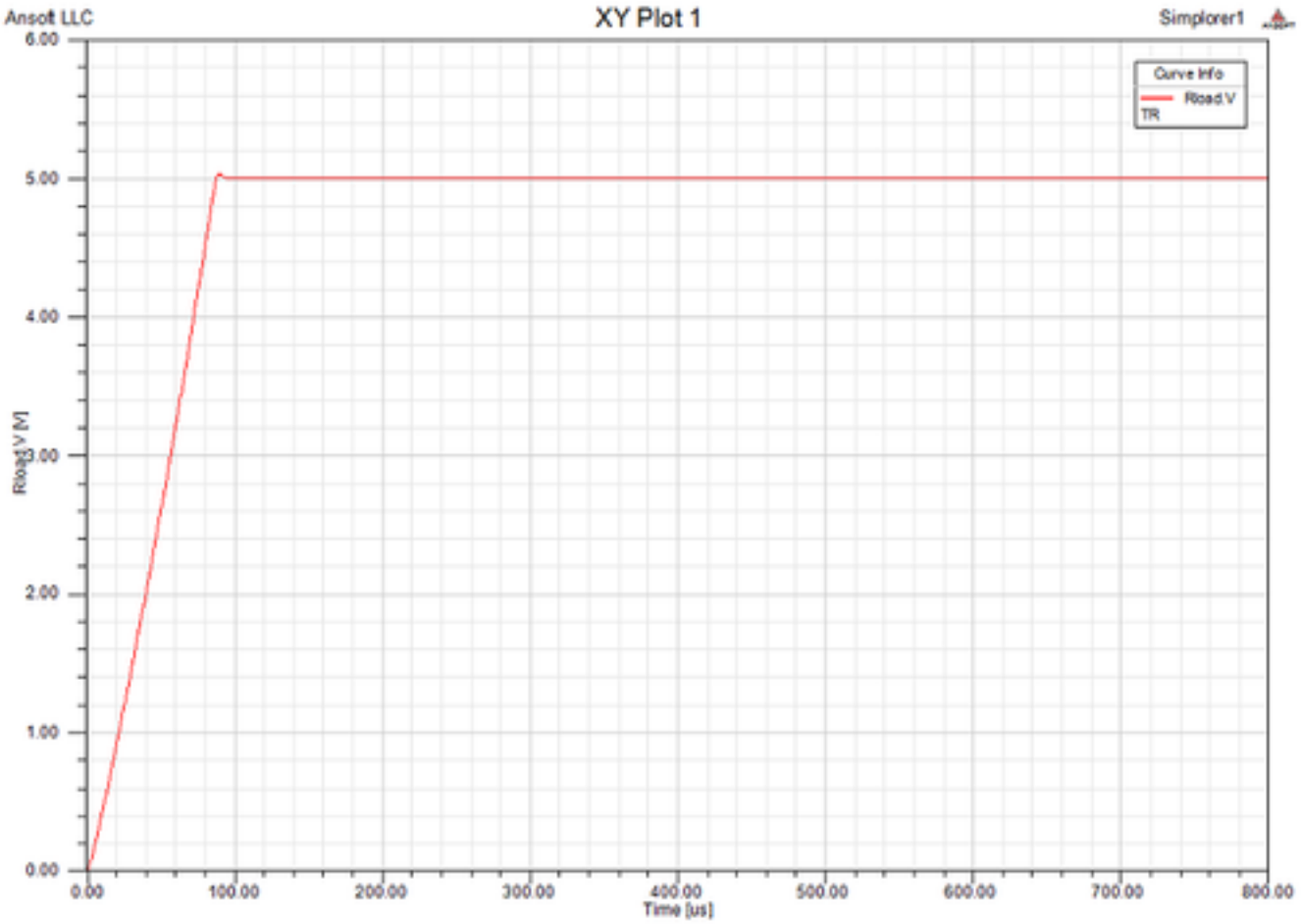

Figure 3. Simulation results

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References

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UCx836: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

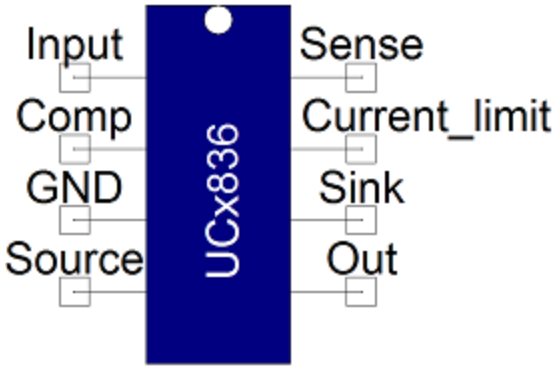

Figure 1. Component symbol

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Description

The *UC1835/6* families of linear controllers are optimized for the design of low cost, low dropout, linear regulators. Using an external pass element, dropout voltages of less than 0.5V are readily obtained.

These devices contain a high gain error amplifier, a 250mA output driver, and a precision reference. In addition, current sense with foldback provides for a 2.5A peak output current dropping to less than 0.5A at short circuit.

These devices are available in fixed, 5V, (*UC1835*), or adjustable, (*UC1836*), versions. In the fixed 5 volt version, the only external parts required are an external pass element, an output capacitor, and a compensation capacitor. On the adjustable version the output voltage can be set anywhere from 2.5V to 35V with two external resistors.

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Additional features of these devices include under-voltage lockout for predictable start-up, thermal shutdown and short circuit current limiting to protect the driver device. On the fixed voltage version, a reverse voltage comparator minimizes reverse load current in the event of a negative input to output differential.

The model consists of a bipolar transistor that supplies the current to the external pass device base junction. The transconductance operational amplifiers are modeled by controlled current source. An internal logic limits the current supplied by the Voltage amplifier. Two set of state machines controls the Under Voltage Lock Out.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	Vin	Positive Supply Voltage
2	Comp	Compensation and Shutdown
3	GND	Ground
4	Source	Driver Source
5	Sense	Sense Resistor Out
6	Current_limit	Current limit
7	Sink	Driver Sink
8	Out	Sense Output Voltage

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Parameters

Comparison between model and real component.

Table 2

PARAMETER	TEST CONDITIONS	MIN	TYPE	MAX	MODEL	UNITS

Twin Builder 2025 R2 - © ANSYS, Inc. All rights reserved. - Contains proprietary and confidential information of ANSYS, Inc. and its subsidiaries and affiliates.

Driver						
Maximum Current	+VIN = 12V	25-0	500		-	mA
Saturation Voltage	Driver Current = 250mA, Driver Sink		2.0	2.8	2	V
Pull-Up Current at Driver Sink	Compensation/ Shutdown=0.45V	14-0	250	300	250	A
Driver SinkLeakage	In UVLO			10	0	A
	In Reverse Voltage			10	0	A
Thermal Shutdown			165		X	°C
Foldback CurrentLimit						
Current Limit Levels at Sense Resistor Out	VOUT Sense = (0.99) VREG	2.2	2.5	2.8	2.45	A
	VOUT Sense = (0.5) VREG	1.3	1.5	1.7	1.55	A
	VOUT Sense = 0V	0.2-5	0.4	0.5-5	0.5	A
Current LimitAmp Tansconductance	100 A at Compensation/Shutdown, VOUT Sense = (0.9) VREG	12	24	42	240	mS
Limiting Voltage at Current Limit	VOUT Sense = (0.9) VREG Volts Below +VIN, TJ = 25°C	80	100	140	93	mV
Sense Resistor Value	VOUT Sense = (0.9) VREG, IOUT = IA, TJ = 25°C		40		40	mOhm
Input Supply						
Supply Current	+VIN = 6V		2.75	4.0	2.75	mA
	+VIN = 40V		3.75	6.0	3.75	mA
UVLO Threshold	+VIN Low to High, VOUT Sense = 0V	3.9	4.4	4.9	4.4	V
Threshold Hysteresis			0.1	0.3-5	0.1	V
Reverse Current	+VIN = -1.0V, Driver Sink Open		6.0	20	-	mA

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Regulating Voltage and Error Amplifier						
Regulating Level at VOUT Sense (VREG)	Driver Current = 10mA, TJ = 25°C	2.4-7	2.5	2.5-3	2.5	V
Line Regulation	+VIN = 5.2V + 35V		6	20	0	mV
Load Regulation	Driver Current = 0 to 250mA		3	15	3	mV
Bias Current at VOUT Sense	VOUT Sense = 5.0V	-1.0	-0.2		0	A
Error Amp Transconductance	100 A at Compensation/Shutdown Pin	0.8	1.3	2.0	1.3	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	-	uA

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Examples

Example circuit :

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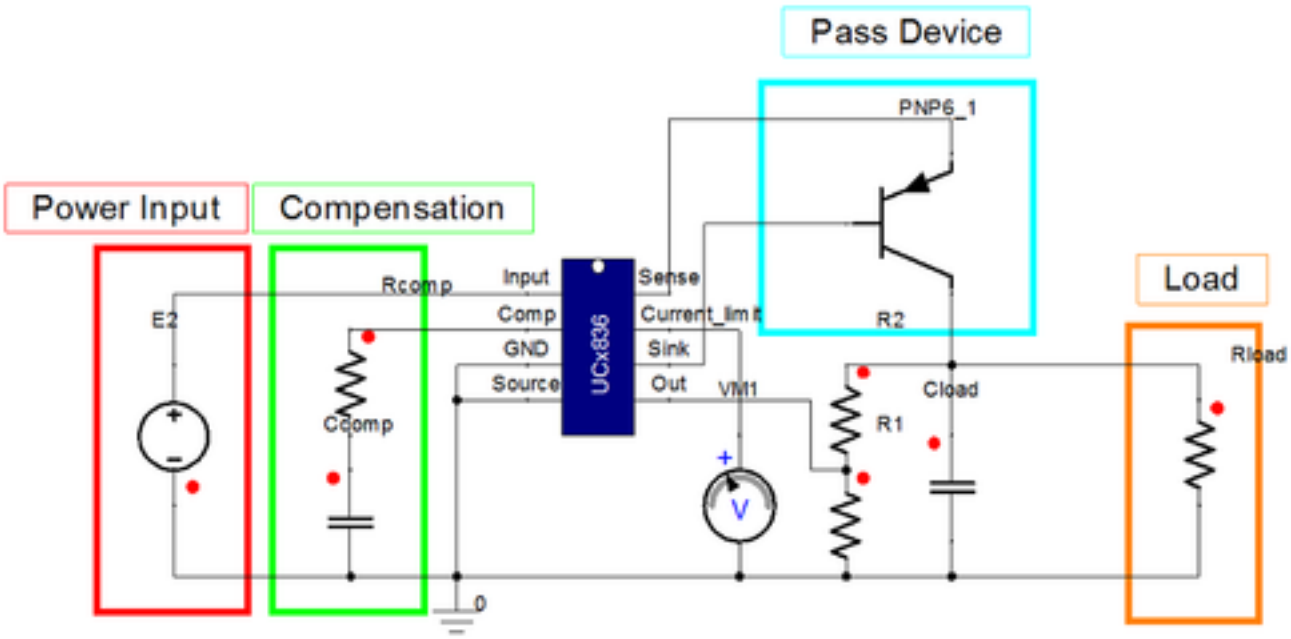

Figure 2. Example Circuit

Simulation results :

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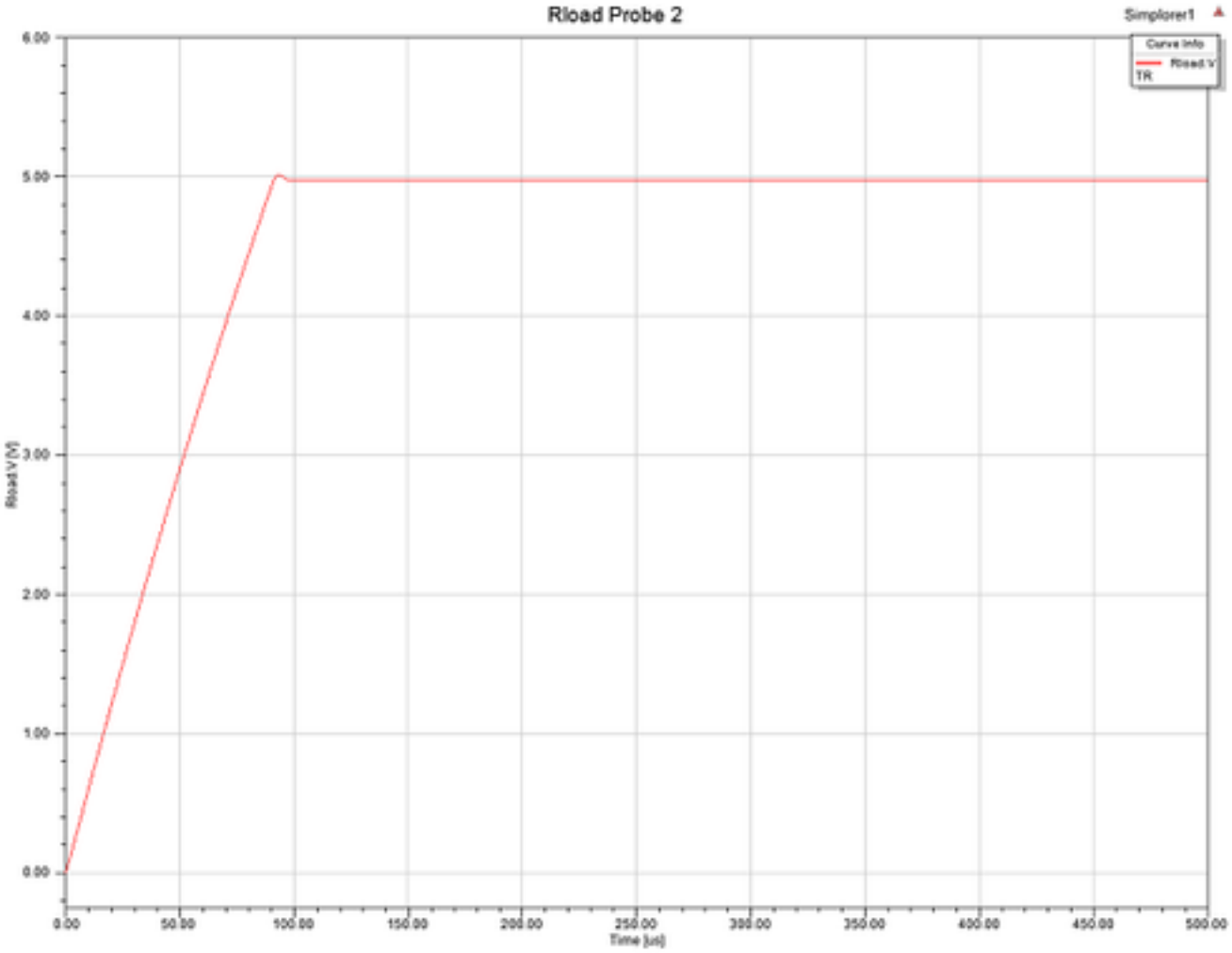

Figure 3. Simulation results

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References

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Load Share Controllers

Load Share Controllers consist of the following types of models:

- UC1902

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UC1902/2902/3902

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

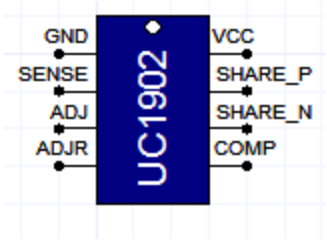

Figure 1. Component symbol

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Description

The UC1902 load share controller is an 8-pin device that balances the current drawn from independent, paralleled power supplies. Load sharing is accomplished by adjusting each supply's output current to a level proportional to the voltage on a share bus.

The primary power supply, which is automatically designated as the supply that regulates to the highest voltage, drives the share bus with a voltage proportional to its output current. The UC1902 trims the output voltage of the other paralleled supplies so that they each support their share of the load current. Typically, each supply is designed for the same current level although that is not necessary for use with the UC1902. By appropriately scaling the current sense resistor, supplies with different output current capability can be paralleled with each supply providing the same percentage of their output current capability for a particular load.

A differential line is used for the share bus to maximize noise immunity and accommodate different voltage drops in each power converter's ground return line. Trimming of each converter's output voltage is accomplished by injecting a small current into the output voltage sense line, which requires a small resistance (typically 20W – 100W) to be inserted

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Conservative Pins

Table 1

Name	Description
ADJ	Current output of adjust amplifier circuit (NPN collector).
ADJR	Current adjust amplifier range set (NPN emitter).
COMP	Output of error amplifier, input of adjust amplifier. This is where the compensation capacitor is connected.
GND	Local power supply return and signal ground.
SENSE	Inverting input of current sense amplifier.
SHARE_P	Positive input from share bus or drive to share bus.
SHARE_N	Reference for SHARE+.
VCC	Local power supply (positive).

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Examples

Example:

The next figure shows an example of connection of the UC1902. This is an example with three power supplies (PSU1, PSU2 and PSU3) that are connected in parallel to supply a load. In order to share the current among the power supplies, one UC1902 is placed with its correspondent power supply. All the UC1902 are communicated through a common bus with two lines, SHARE+ and SHARE-.

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In this example all the PSU will regulate the output voltage to 12V. In order to see the effect of the UC1902, the PSU1 reference voltage is initially set to 11.8V, and the other two PSUs are set to 12V. After 100ms, the reference voltage for PSU1 is set to 12.2V.

Figure 2 shows the output current of each power supply. It can be noticed how, even though the reference voltage of the three power supplies is different, the UC1902 forces the current sharing among the Power Supplies.

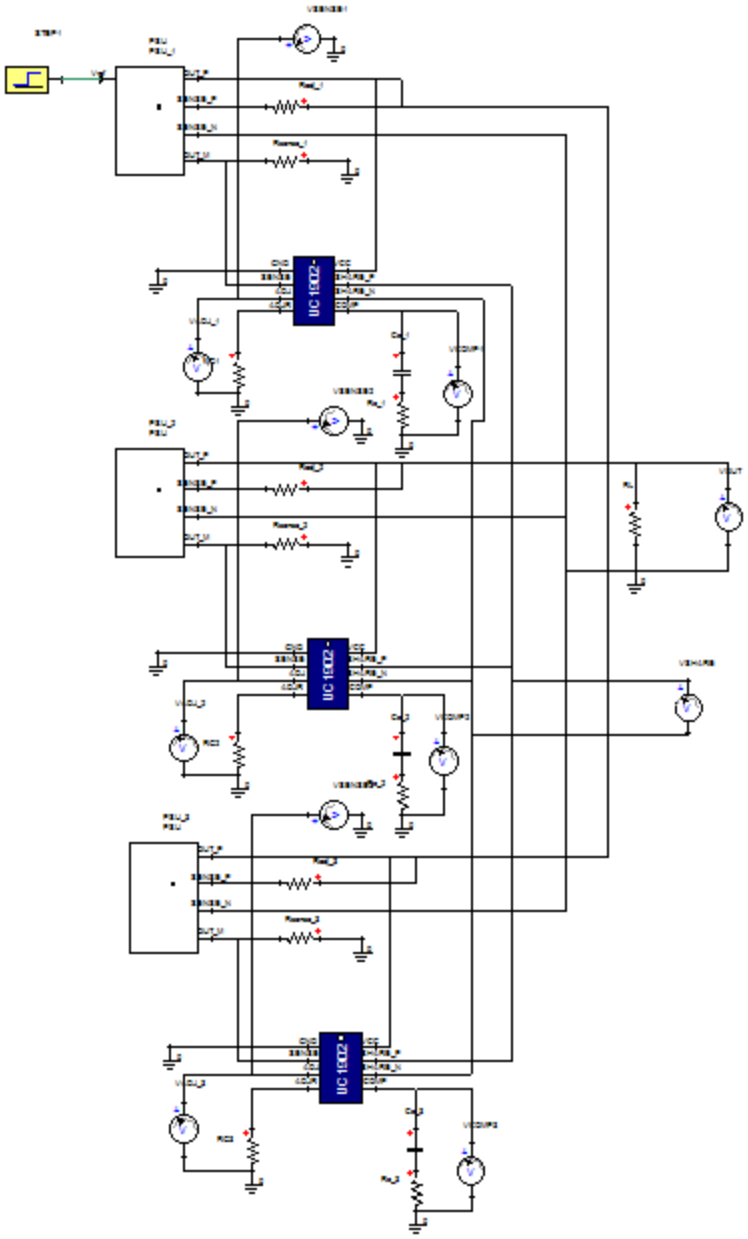

Figure 2. Twin Builder Schematic Example of use of the UC1902

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References

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Low Side Switches

The Low Side Switches consist of the following types of models:

- IPS1011
- IPS1021
- IPS1031
- IPS1041
- IPS1051

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IPS1011: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

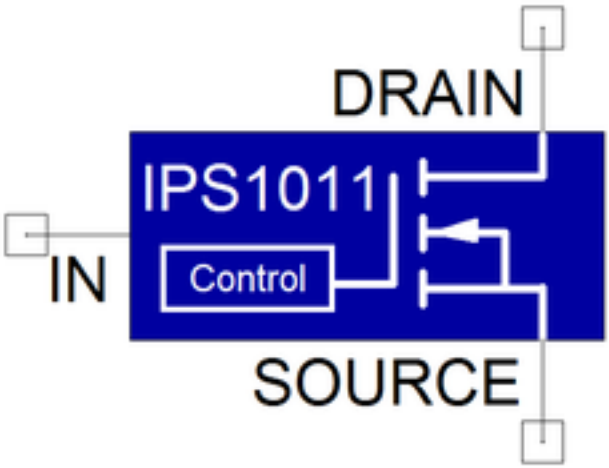

Figure 1. Component symbol

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Description

The *IPS1011* is a three terminal Intelligent Power Switch (IPS) that features a low side MOSFET with over-current and drain to source active clamp. The switch provides efficient protection by turning OFF the power MOSFET when the drain current reaches the shutdown current value. The device restarts once the input is cycled. A serial resistance connected to the input provides the diagnostic.

The internal MOSFET is modeled with an ideal switch in series with a resistor which represents the conduction internal resistance (Rdson). A state machine controls the diagnosis switch.

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Another one models the switching delays. The active clamp has been modeled with a zener diode equivalent circuit (two diodes and a voltage source).

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Conservative Pins

Table 1

Symbol	Description
IN	Control signal
DRAIN	MOSFET drain
SOURCE	MOSFET source

Product summary:

Table 2

Rds (on)	13mΩ (max.)
Vclamp	36V
Ishutdown	85A (typ.)

Table 3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdon	Turn-on delay time to 20%	15	50	150	us
Tr	Rise time 20% to 80%	20	50	100	
Tdoff	Turn-off delay time to 80%	100	330	1000	
Tf	Fall time 80% to	30	70	150	

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	20%				
Eon + Eoff	Turn on and off energy	-	5	-	mJ

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Parameters

Comparison between model and real component.

The model matches the real model parameters concerning switching delays (t_{on} and t_{off}), maximum current, voltage clamp and conduction resistance as they appear in the product summary section. Input and output impedances match the real ones. Leakage currents have not been implemented. Temperature influence parameters have not been implemented.

Tj=25°C, Vcc=14V (unless otherwise specified)

Table 4

Symbol	Parameter	IPS1011	MODEL	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	10	15	mΩ	Vin=5V, Ids=30A
	ON state resistance Tj=150°C (2)	19	15		
Idss1	Drain to source leakage current	0.1	X	µA	Vcc=14V, Tj=25°C
Idss2	Drain to source leakage current	0.2	X		Vcc=28V, Tj=25°C
V clamp1	Drain to source clamp voltage 1	39	39	V	Id=20mA
V clamp2	Drain to source clamp voltage 2	40	40		Id=5A
Vin clamp	IN to source pin clamp voltage	6.5	6.5		Iin=1mA
Vth	Input threshold voltage	1.7	X		Id=10mA

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X: not implemented

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Example circuit :

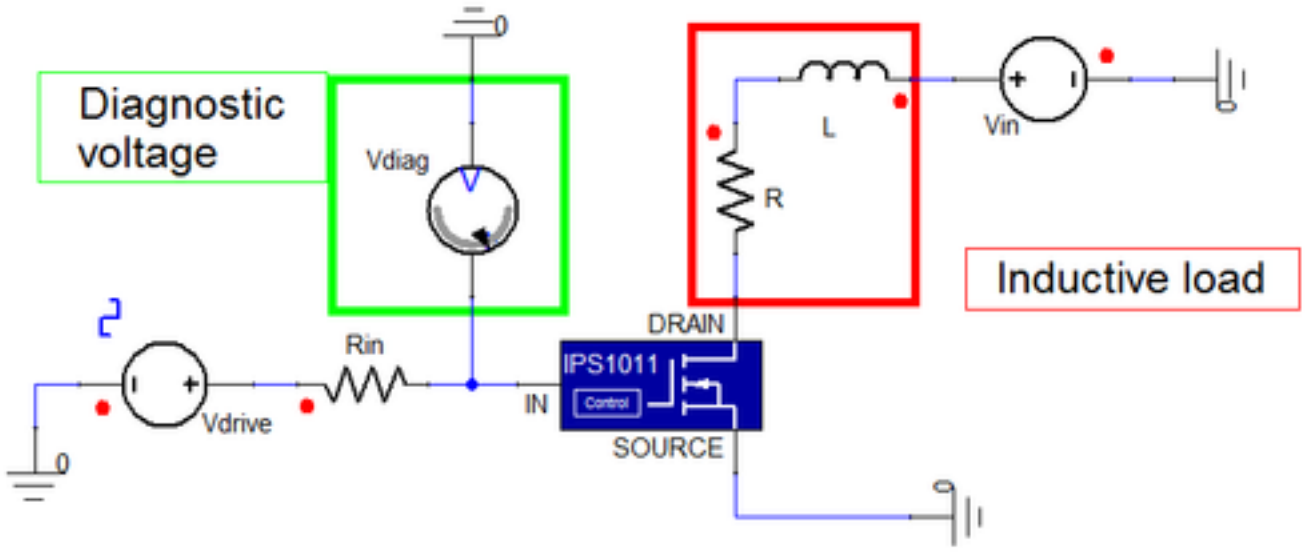

Figure 2. Example Circuit

This low side switch is used here to feed an inductive load. This kind of load allows us to check the steady operation and the overcurrent protection.

Simulation results :

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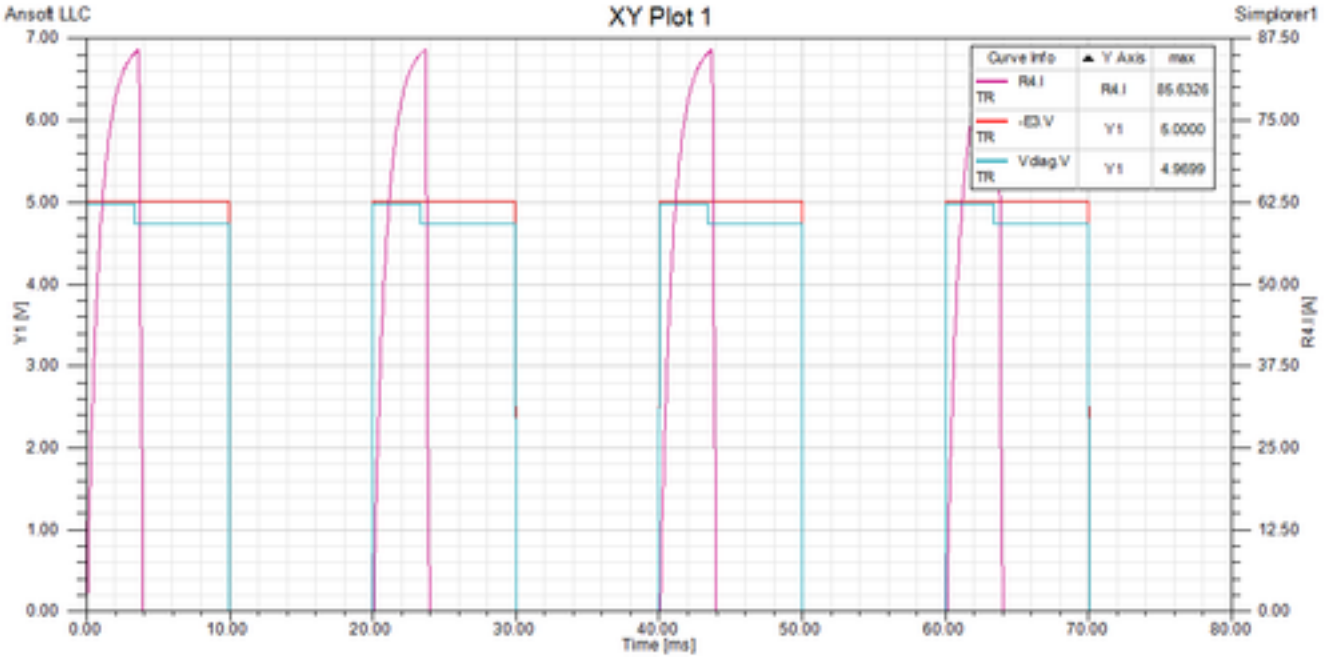

Purple: load current

Red: input voltage

Blue: diagnosis voltage

Figure 3. Simulation results

This circuit operates as a usual MOSFET with an overcurrent protection system and a diagnosis output. When load current exceeds the shutdown current, MOSFET opens and diagnosis voltage falls.

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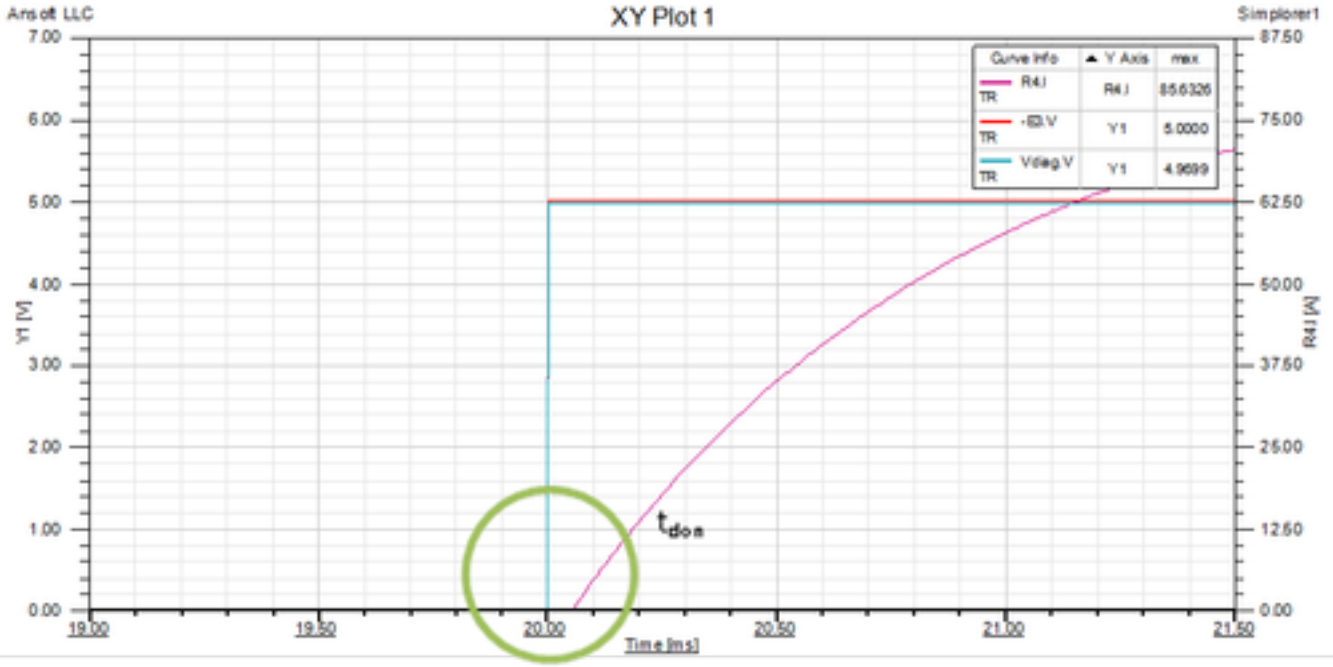

Purple: load current

Red: input voltage

Blue: diagnosis voltage

Figure 4. Detail of timing implementation

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References

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IPS1021: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

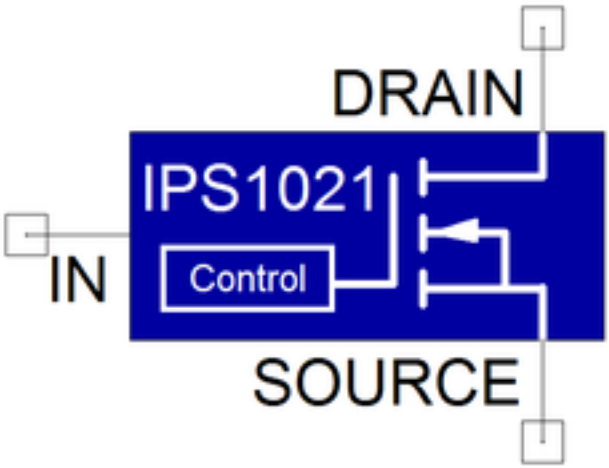

Figure 1. Component symbol

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Description

The *IPS1021* is a three terminal Intelligent Power Switch (IPS) that features a low side MOSFET with over-current and drain to source active clamp. The switch provides efficient protection by turning OFF the power MOSFET when the drain current reaches the shutdown current value. The device restarts once the input is cycled. A serial resistance connected to the input provides the diagnostic.

The internal MOSFET is modeled with an ideal switch (S1) in series with a resistor which represents the conduction internal resistance (Rdson). A state machine controls the diagnosis

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switch (S2). Another machine models the switching delays. The active clamp has been modeled with a zener diode equivalent circuit (two diodes and a voltage source).

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Conservative Pins

Table 1

Symbol	Description
IN	Control signal
DRAIN	MOSFET drain
SOURCE	MOSFET source

Product summary:

Table 2

Rds (on)	25mΩ (max.)
Vclamp	36V
Ishutdown	35A (typ.)

Table 3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdon	Turn-on delay time to 20%	10	30	100	us
Tr	Rise time 20% to 80%	10	30	60	
Tdoff	Turn-off delay time to 80%	40	150	400	
Tf	Fall time 80% to	15	30	60	

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	20%				
Eon + Eoff	Turn on and off energy	-	2	-	mJ

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Parameters

Comparison between model and real component.

The model matches the real model parameters concerning switching delays (t_{on} and t_{off}), maximum current, voltage clamp and conduction resistance as they appear in the product summary section. Input and output impedances match the real ones. Leakage currents have not been implemented. Temperature influence parameters have not been implemented.

Tj=25°C, Vcc=14V (unless otherwise specified)

Table 4

Symbol	Parameter	IPS1021	MODEL	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	20	25	mΩ	Vin=5V, Ids=8A
	ON state resistance Tj=150°C (2)	38	25		
Idss1	Drain to source leakage current	0.1	X	ÂµA	Vcc=14V, Tj=25°C
Idss2	Drain to source leakage current	0.2	X		Vcc=28V, Tj=25°C
V clamp1	Drain to source clamp voltage 1	39	39	V	Id=20mA
V clamp2	Drain to source clamp voltage 2	40	40		Id=2A
Vin clamp	IN to source pin clamp voltage	6.5	6.5		Iin=1mA
Vth	Input threshold voltage	1.7	X		Id=10mA

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X: not implemented

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Examples

Example circuit :

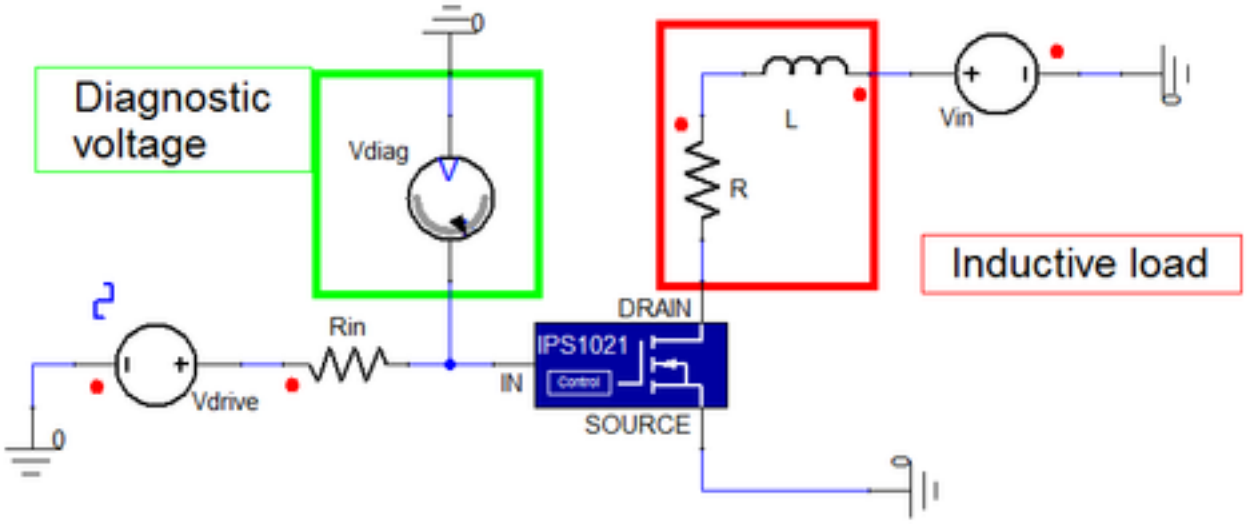

Figure 2. Example Circuit

This low side switch is used here to feed an inductive load. This kind of load allows us to check the steady operation and the overcurrent protection.

Simulation results :

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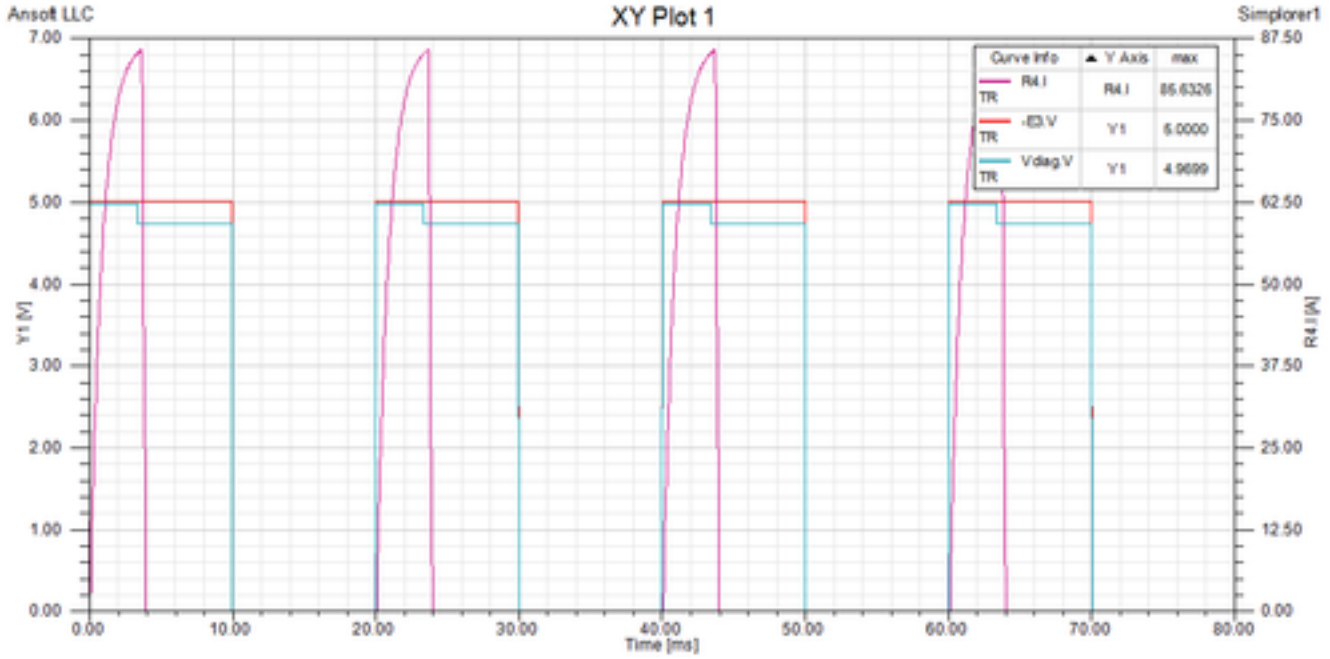

Purple: load current

Red: input voltage

Blue: diagnosis voltage

Figure 3. Simulation results

This circuit operates as a usual MOSFET with an overcurrent protection system and a diagnosis output. When load current exceeds the shutdown current, MOSFET opens and diagnosis voltage falls.

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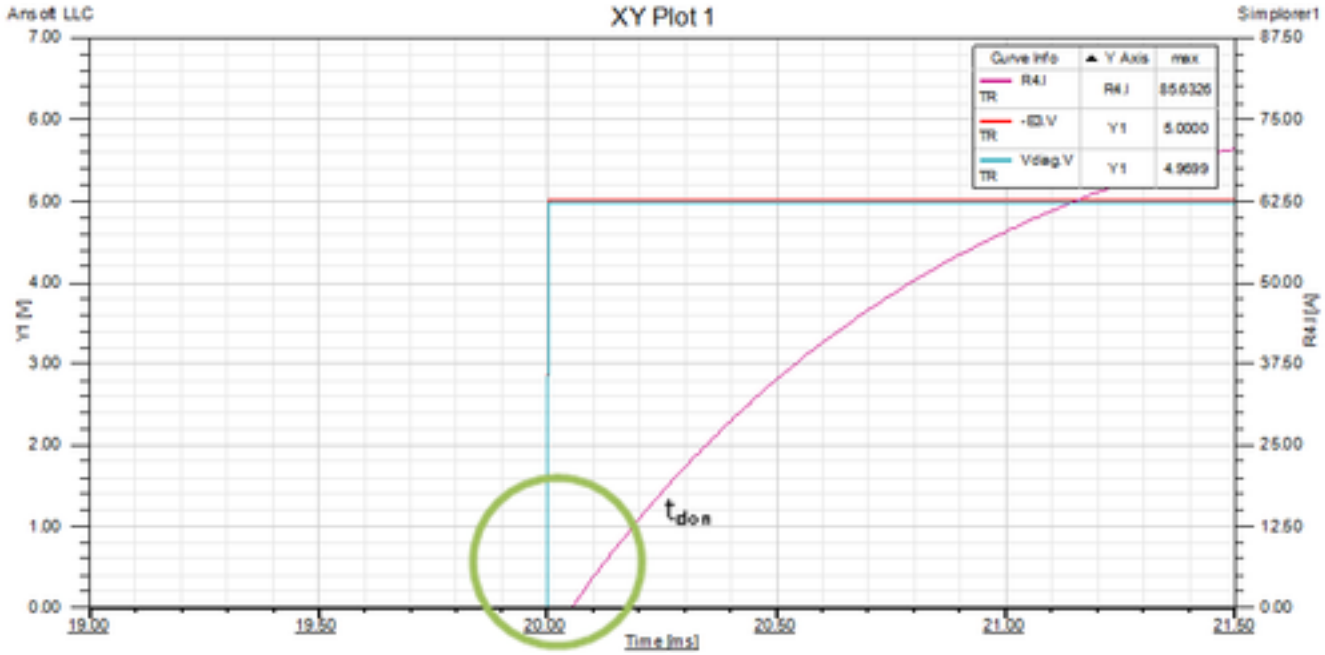

Purple: load current

Red: input voltage

Blue: diagnosis voltage

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IPS1031: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

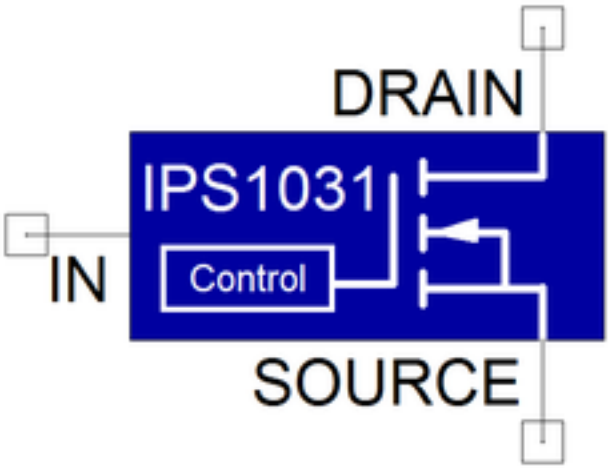

Figure 1. Component symbol

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Description

The *IPS1031* is a three terminal Intelligent Power Switch (IPS) that features a low side MOSFET with over-current and drain to source active clamp. The switch provides efficient protection by turning OFF the power MOSFET when the drain current reaches the shutdown current value. The device restarts once the input is cycled. A serial resistance connected to the input provides the diagnostic.

The internal MOSFET is modeled with an ideal switch in series with a resistor which represents the conduction internal resistance (Rdson). A state machine controls the diagnosis switch.

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Another one models the switching delays. The active clamp has been modeled with a zener diode equivalent circuit (two diodes and a voltage source).

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Table 1

Symbol	Description
IN	Control signal
DRAIN	MOSFET drain
SOURCE	MOSFET source

Product summary:

Table 2

Rds (on)	50mΩ (max.)
Vclamp	36V
Ishutdown	18A (typ.)

Table 3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdon	Turn-on delay time to 20%	3	10	30	us
Tr	Rise time 20% to 80%	6	20	40	
Tdoff	Turn-off delay time to 80%	20	70	200	
Tf	Fall time 80% to	6	15	30	

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	20%				
Eon + Eoff	Turn on and off energy	-	0.7	-	mJ

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Parameters

Comparison between model and real component.

The model matches the real model parameters concerning switching delays (t_{on} and t_{off}), maximum current, voltage clamp and conduction resistance as they appear in the product summary section. Input and output impedances match the real ones. Leakage currents have not been implemented. Temperature influence parameters have not been implemented.

Tj=25°C, Vcc=14V (unless otherwise specified)

Table 4

Symbol	Parameter	IPS1031	MODEL	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	40	50	mΩ	Vin=5V, Ids=8A
	ON state resistance Tj=150°C (2)	76	50		
Idss1	Drain to source leakage current	0.1	X	µA	Vcc=14V, Tj=25°C
Idss2	Drain to source leakage current	0.2	X		Vcc=28V, Tj=25°C
V clamp1	Drain to source clamp voltage 1	39	39	V	Id=20mA
V clamp2	Drain to source clamp voltage 2	40	40		Id=1A
Vin clamp	IN to source pin clamp voltage	6.5	6.5		Iin=1mA
Vth	Input threshold voltage	1.7	X		Id=10mA

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X: not implemented

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Example circuit :

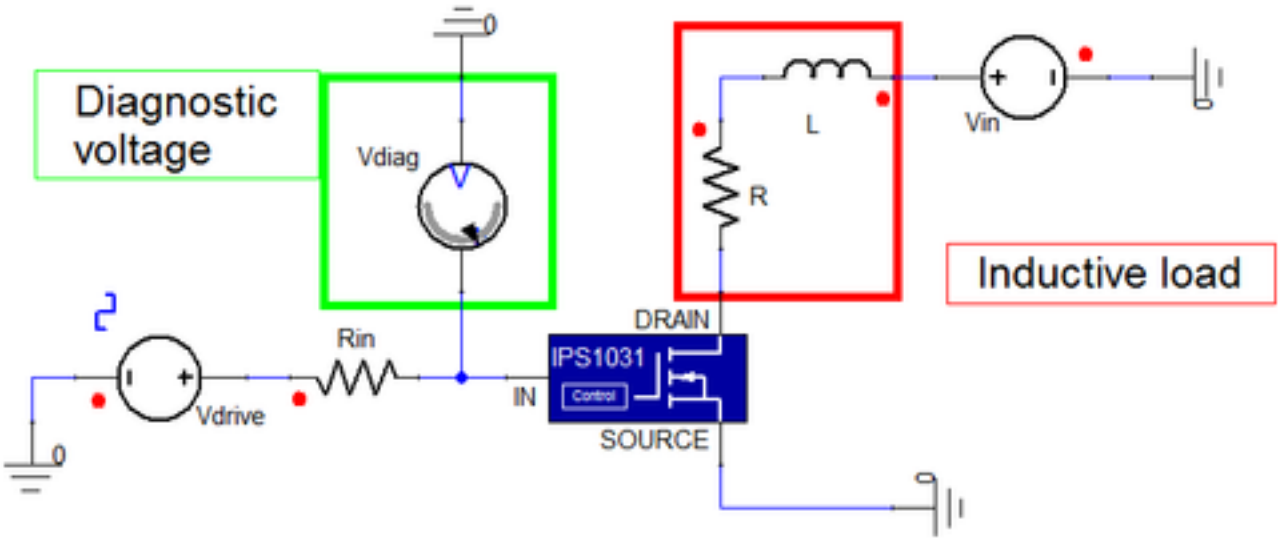

Figure 2. Example Circuit

This low side switch is used here to feed an inductive load. This kind of load allows us to check the steady operation and the overcurrent protection.

Simulation results :

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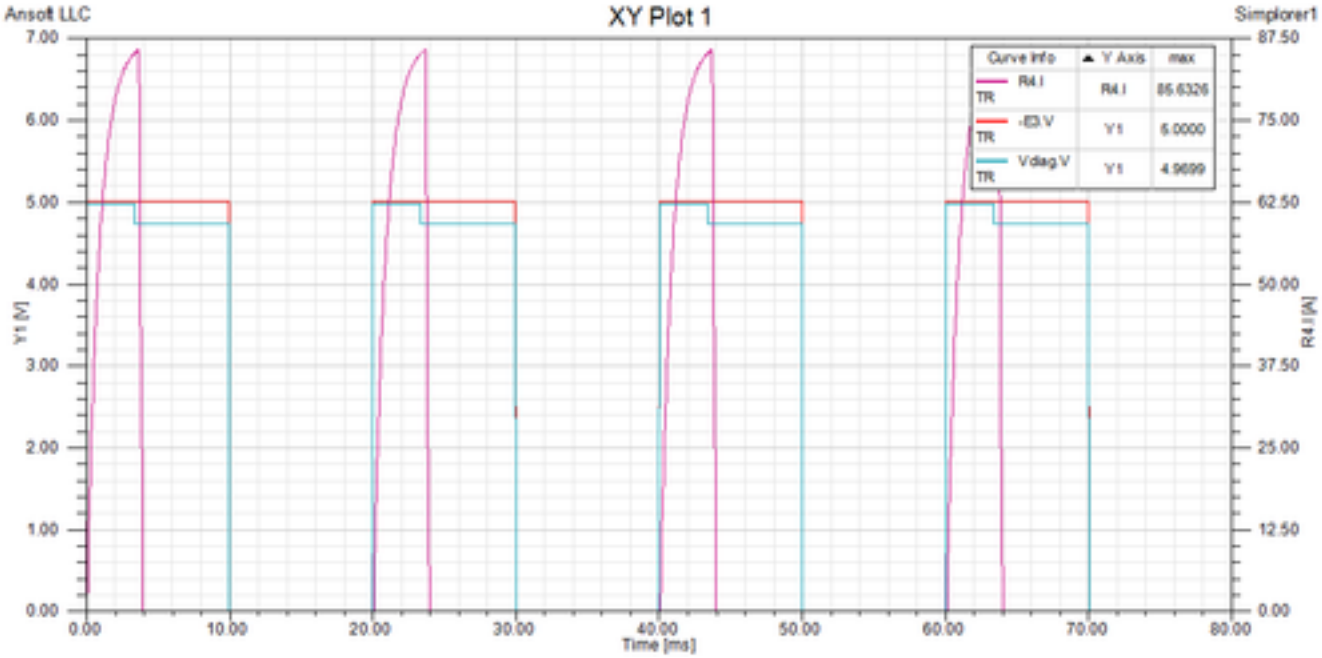

Purple: load current

Red: input voltage

Blue: diagnosis voltage

Figure 3. Simulation results

This circuit operates as a usual MOSFET with an overcurrent protection system and a diagnosis output. When load current exceeds the shutdown current, MOSFET opens and diagnosis voltage falls.

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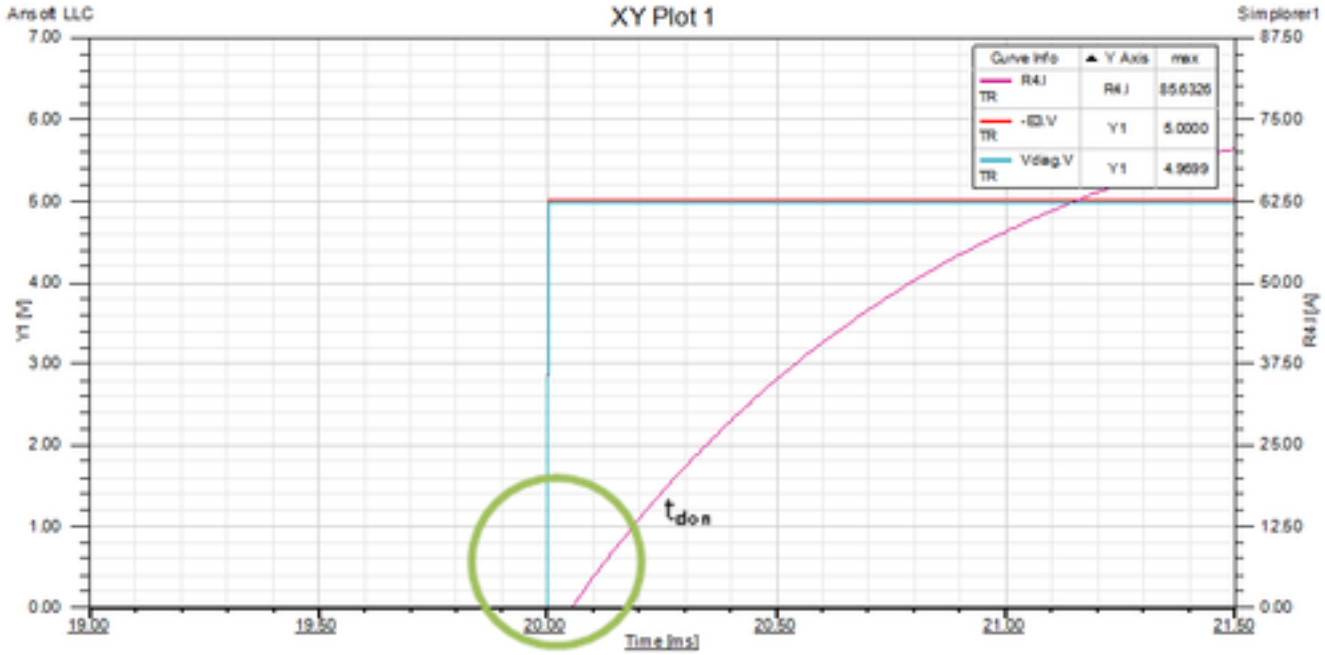

Purple: load current

Red: input voltage

Blue: diagnosis voltage

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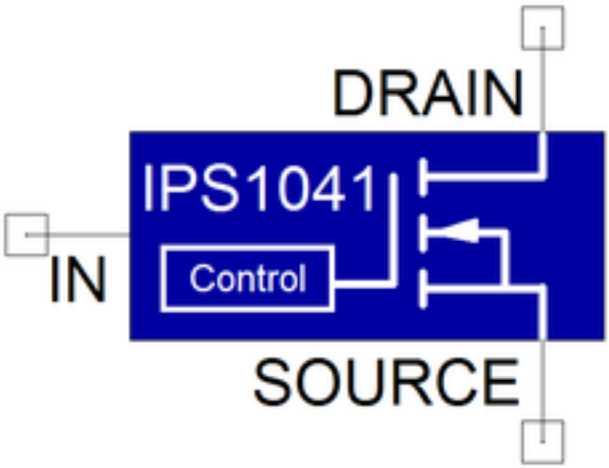
IPS1041: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *IPS1041* is a three terminal Intelligent Power Switch (IPS) that features a low side MOSFET with over-current and drain to source active clamp. The switch provides efficient protection by turning OFF the power MOSFET when the drain current reaches the shutdown current value. The device restarts once the input is cycled. A serial resistance connected to the input provides the diagnostic.

The internal MOSFET is modeled with an ideal switch in series with a resistor which represents the conduction internal resistance (Rdson). A state machine controls the diagnosis switch.

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Another one models the switching delays. The active clamp has been modeled with a zener diode equivalent circuit (two diodes and a voltage source).

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Conservative Pins

Table 1

Symbol	Description
IN	Control signal
DRAIN	MOSFET drain
SOURCE	MOSFET source

Product summary:

Table 2

Rds (on)	100mΩ (max.)
Vclamp	39V
Ishutdown	4.5A (typ.)

Table 3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdon	Turn-on delay time to 20%	3	10	23	us
Tr	Rise time 20% to 80%	2	7	20	
Tdoff	Turn-off delay time to 80%	15	40	150	
Tf	Fall time 80% to	4	10	20	

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	20%				
Eon + Eoff	Turn on and off energy	-	0.2	-	mJ

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Parameters

Comparison between model and real component.

The model matches the real model parameters concerning switching delays (t*on* and t*off*), maximum current, voltage clamp and conduction resistance as they appear in the product summary section. Input and output impedances match the real ones. Leakage currents have not been implemented. Temperature influence parameters have not been implemented.

Tj=25°C, Vcc=14V (unless otherwise specified)

Table 4

Symbol	Parameter	IPS1041	MODEL	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	80	100	mΩ	Vin=5V, Ids=3A
	ON state resistance Tj=150°C (2)	135	175		
Idss1	Drain to source leakage current	0.1	X	µA	Vcc=14V, Tj=25°C
Idss2	Drain to source leakage current	0.2	X		Vcc=28V, Tj=25°C
V clamp1	Drain to source clamp voltage 1	39	39	V	Id=20mA
V clamp2	Drain to source clamp voltage 2	40	40		Id=1A
Vin clamp	IN to source pin clamp voltage	6.5	6.5		Iin=1mA
Vth	Input threshold voltage	1.7	X		Id=10mA

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X: not implemented

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Example circuit :

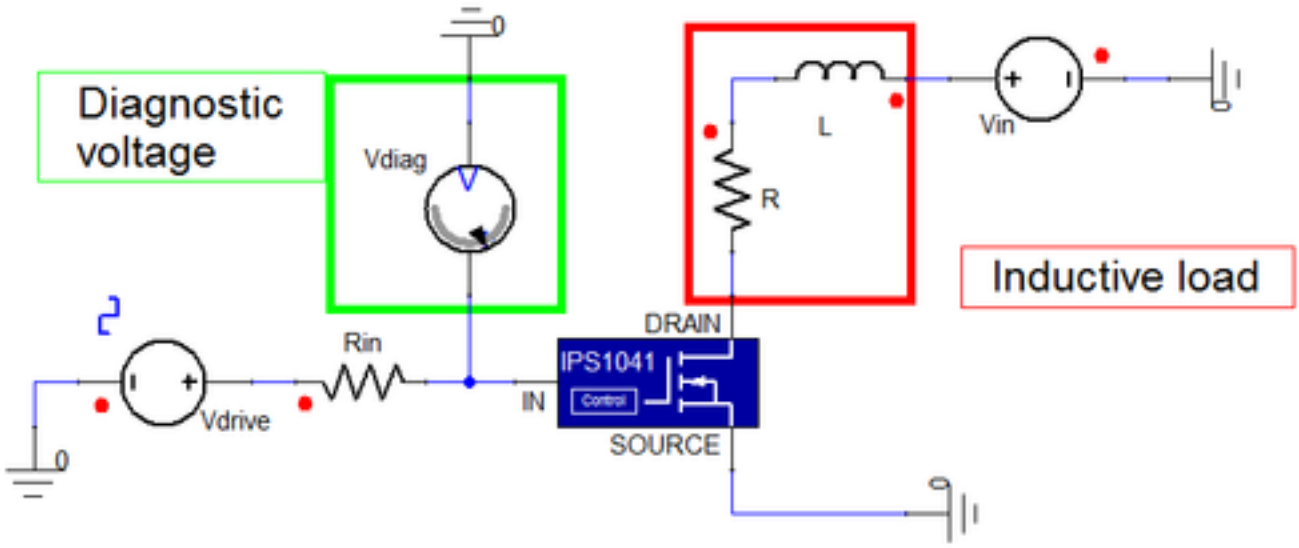

Figure 2. Example Circuit

This low side switch is used here to feed an inductive load. This kind of load allows us to check the steady operation and the overcurrent protection.

Simulation results :

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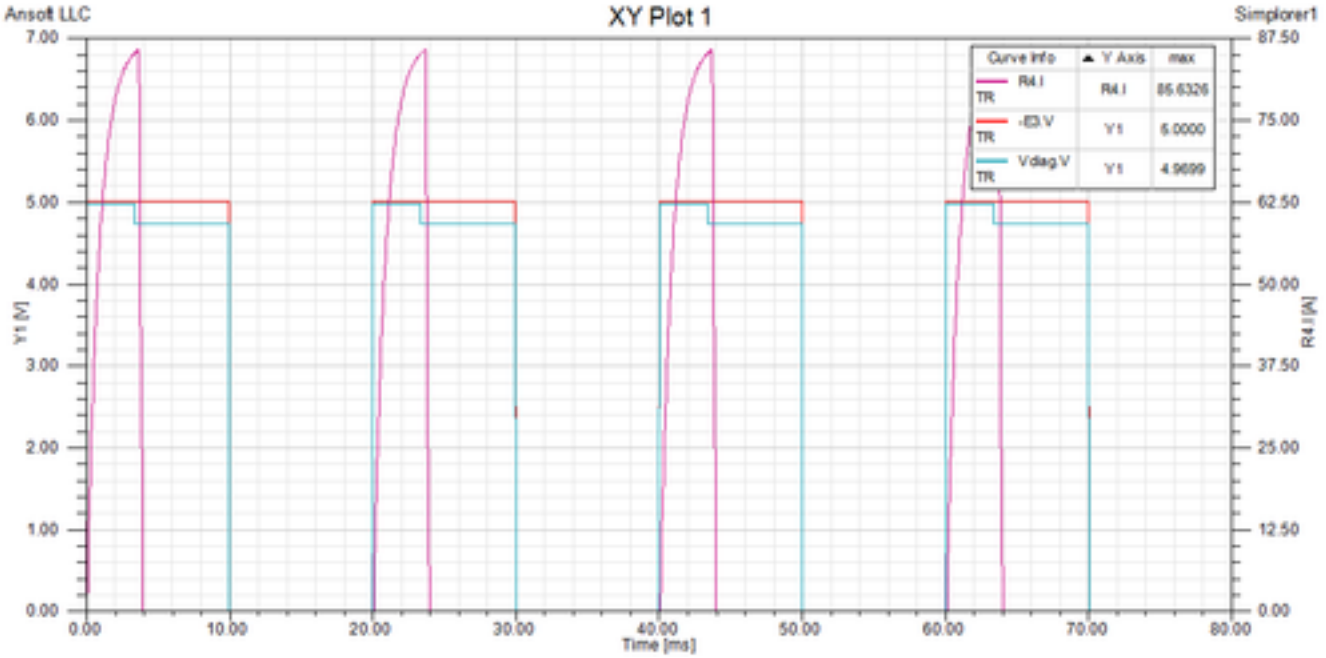

Purple: load current

Red: input voltage

Blue: diagnosis voltage

Figure 3. Simulation results

This circuit operates as a usual MOSFET with an overcurrent protection system and a diagnosis output. When load current exceeds the shutdown current, MOSFET opens and diagnosis voltage falls.

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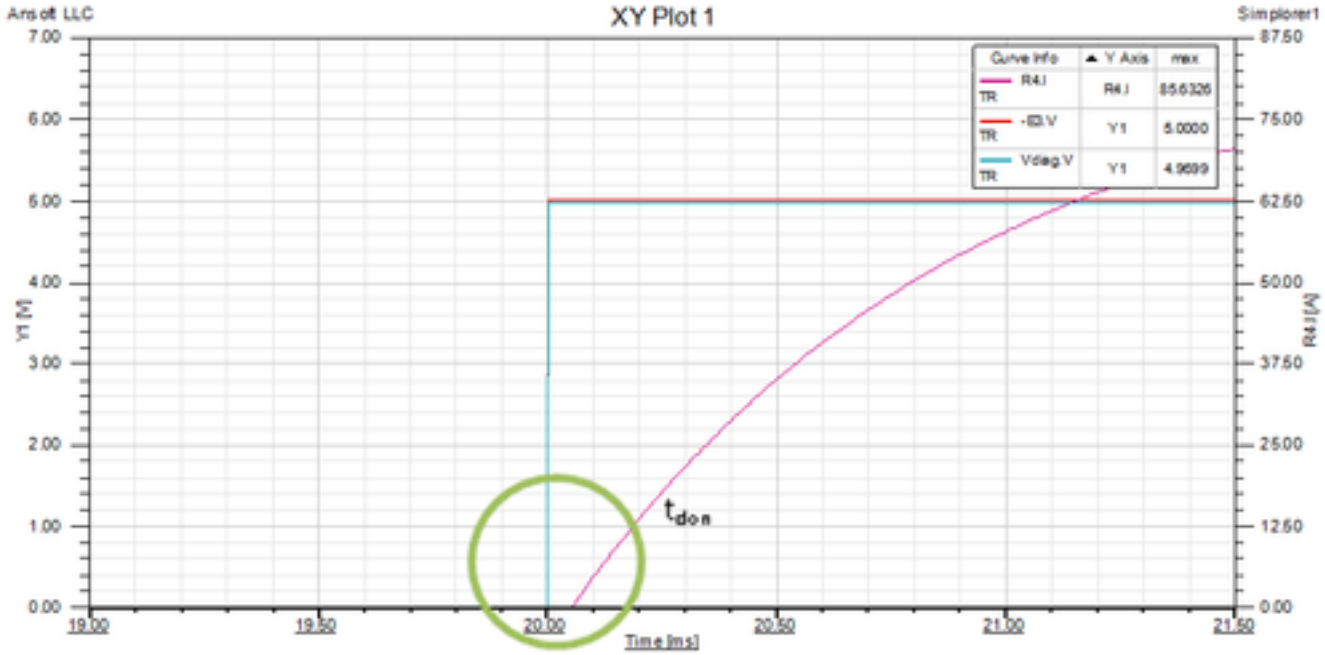

Purple: load current

Red: input voltage

Blue: diagnosis voltage

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IPS1051: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

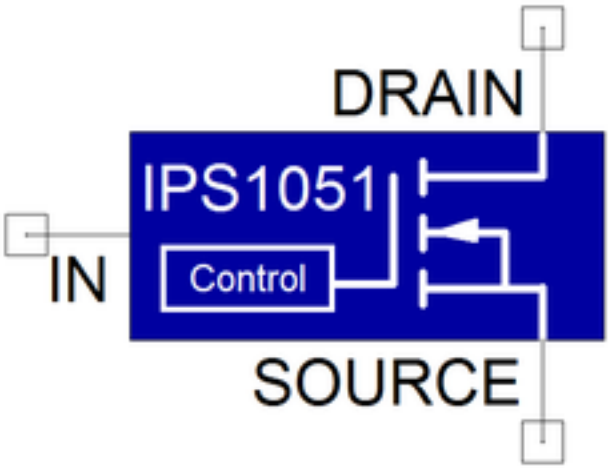

Figure 1. Component symbol

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Description

The *IPS1051* is a three terminal Intelligent Power Switch (IPS) that features a low side MOSFET with over-current and drain to source active clamp. The switch provides efficient protection by turning OFF the power MOSFET when the drain current reaches the shutdown current value. The device restarts once the input is cycled. A serial resistance connected to the input provides the diagnostic.

The internal MOSFET is modeled with an ideal switch in series with a resistor which represents the conduction internal resistance (Rdson). A state machine controls the diagnosis switch.

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Another one models the switching delays. The active clamp has been modeled with a zener diode equivalent circuit (two diodes and a voltage source).

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Conservative Pins

Table 1

Symbol	Description
IN	Control signal
DRAIN	MOSFET drain
SOURCE	MOSFET source

Product summary:

Table 2

Rds (on)	250mΩ (max.)
Vclamp	39V
Ishutdown	2.8A (typ.)

Table 3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tdon	Turn-on delay time to 20%	1	3	10	us
Tr	Rise time 20% to 80%	1	3	10	
Tdoff	Turn-off delay time to 80%	3	15	40	
Tf	Fall time 80% to	2	4	10	

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	20%				
Eon + Eoff	Turn on and off energy	-	0.1	-	mJ

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Parameters

Comparison between model and real component.

The model matches the real model parameters concerning switching delays (ton and toff), maximum current, voltage clamp and conduction resistance as they appear in the product summary section. Input and output impedances match the real ones. Leakage currents have not been implemented. Temperature influence parameters have not been implemented.

Tj=25°C, Vcc=14V (unless otherwise specified)

Table 4

Symbol	Parameter	IPS1051	MODEL	Units	Test Conditions
Rds(on)	ON state resistance Tj=25°C	160	250	mΩ	Vin=5V, Ids=1A
	ON state resistance Tj=150°C (2)	340	175		
Idss1	Drain to source leakage current	0.1	X	µA	Vcc=14V, Tj=25°C
Idss2	Drain to source leakage current	0.2	X		Vcc=28V, Tj=25°C
V clamp1	Drain to source clamp voltage 1	39	39		Id=20mA
V clamp2	Drain to source clamp voltage 2	40	40		Id=0.5A
Vin clamp	IN to source pin clamp voltage	6.5	6.5		Iin=1mA
Vth	Input threshold voltage	1.7	X	V	Id=10mA

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X: not implemented

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Example circuit :

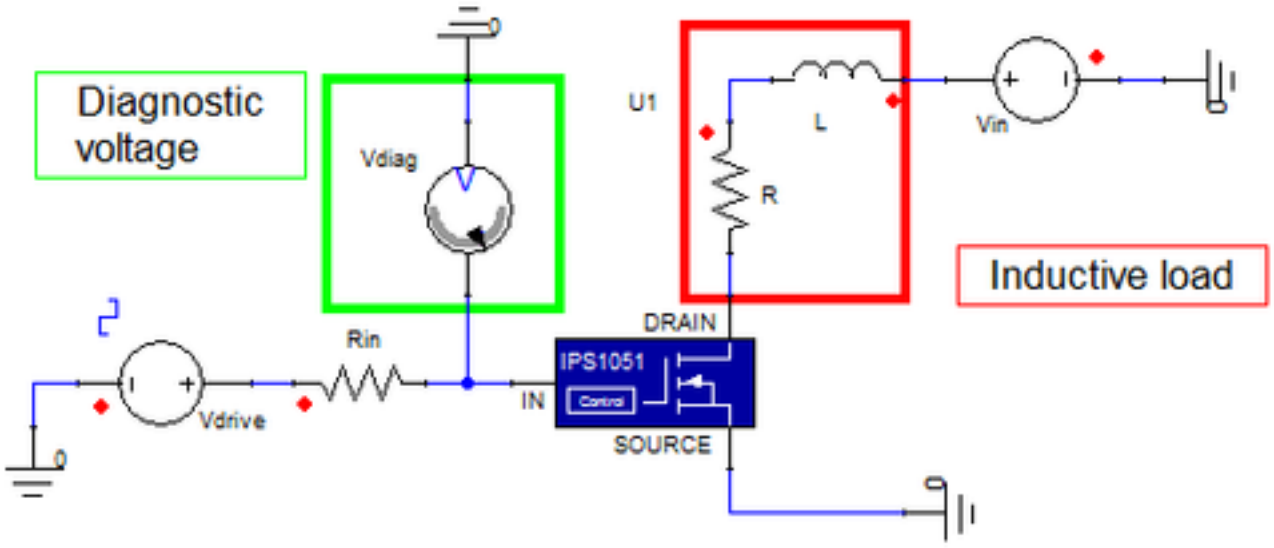

Figure 2. Example Circuit

This low side switch is used here to feed an inductive load. This kind of load allows us to check the steady operation and the overcurrent protection.

Simulation results :

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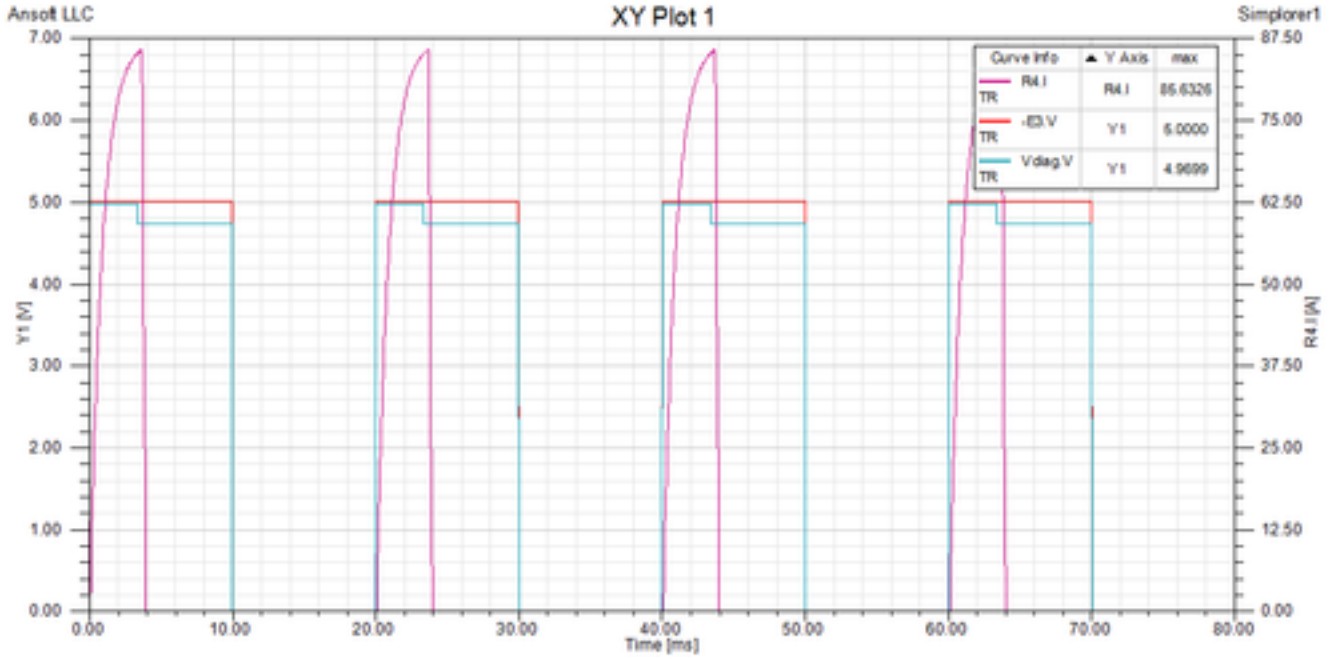

Purple: load current

Red: input voltage

Blue: diagnosis voltage

Figure 3. Simulation results

This circuit operates as a usual MOSFET with an overcurrent protection system and a diagnosis output. When load current exceeds the shutdown current, MOSFET opens and diagnosis voltage falls.

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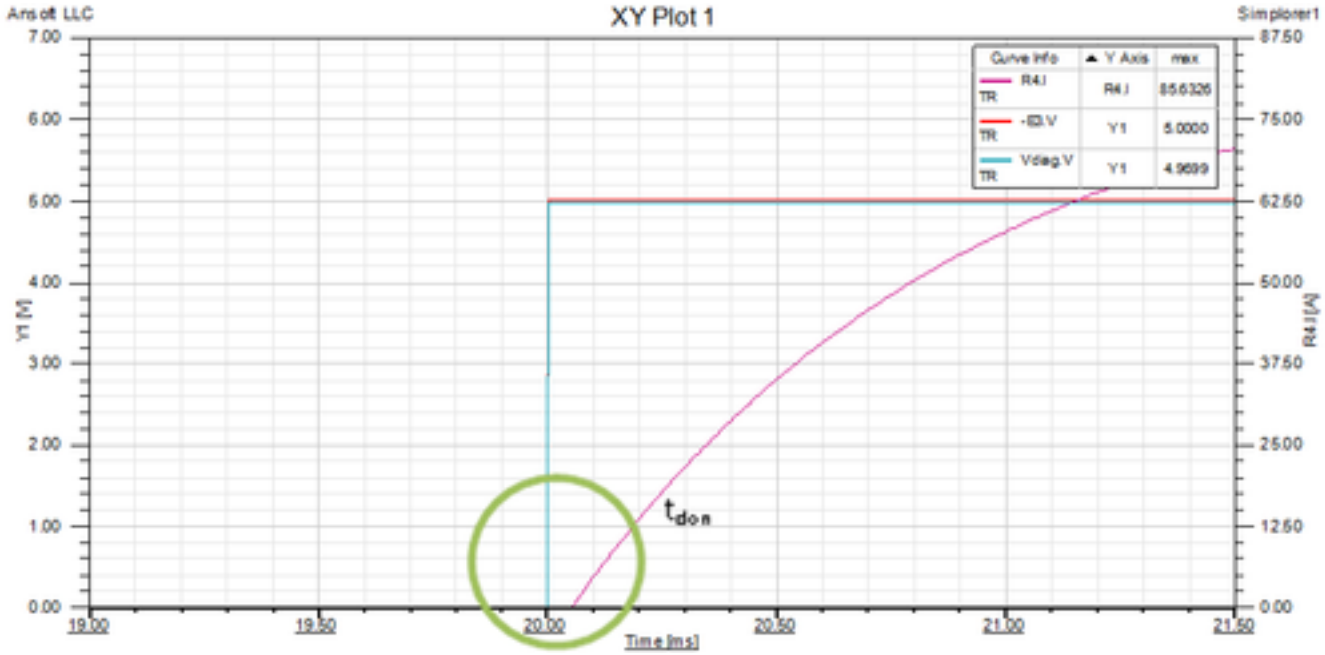

Purple: load current

Red: input voltage

Blue: diagnosis voltage

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Power Factor Correction

The Power Factor Correction consist of the following types of models:

- IR1150
- UCC28019
- UCCx818
- UCx854

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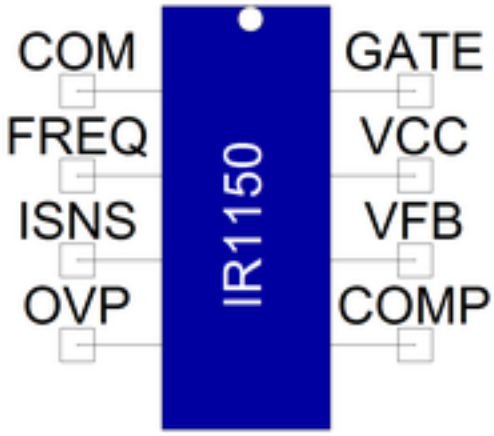
IR1150: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The International Rectifier *IR1150* is a Power Factor Correction (PFC) control IC designed to operate in Continuous Conduction Mode (CCM).

The main operation of this IC is controlled by several state machines. The top one controls the switch that resets the integrator. The bottom ones control the undervoltage, overvoltage and overcurrent protections respectively. The frequency of operation is calculated in a constant block before use its value in other calculus. The ideal switches that model the totem-pole output are controlled by comparing the adder and integrator outputs.

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Conservative Pins

Table 1

Pin #	Name	Description
1	COM	Ground
2	FREQ	Frequency Set
3	ISNS	Current Sense
4	OVP	Overvoltage Fault Detect / Enable
5	COMP	Voltage Loop Compensation
6	VFB	Output Voltage Sense
7	VCC	IC Supply Voltage
8	GATE	Gate Drive Output

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Example circuit :

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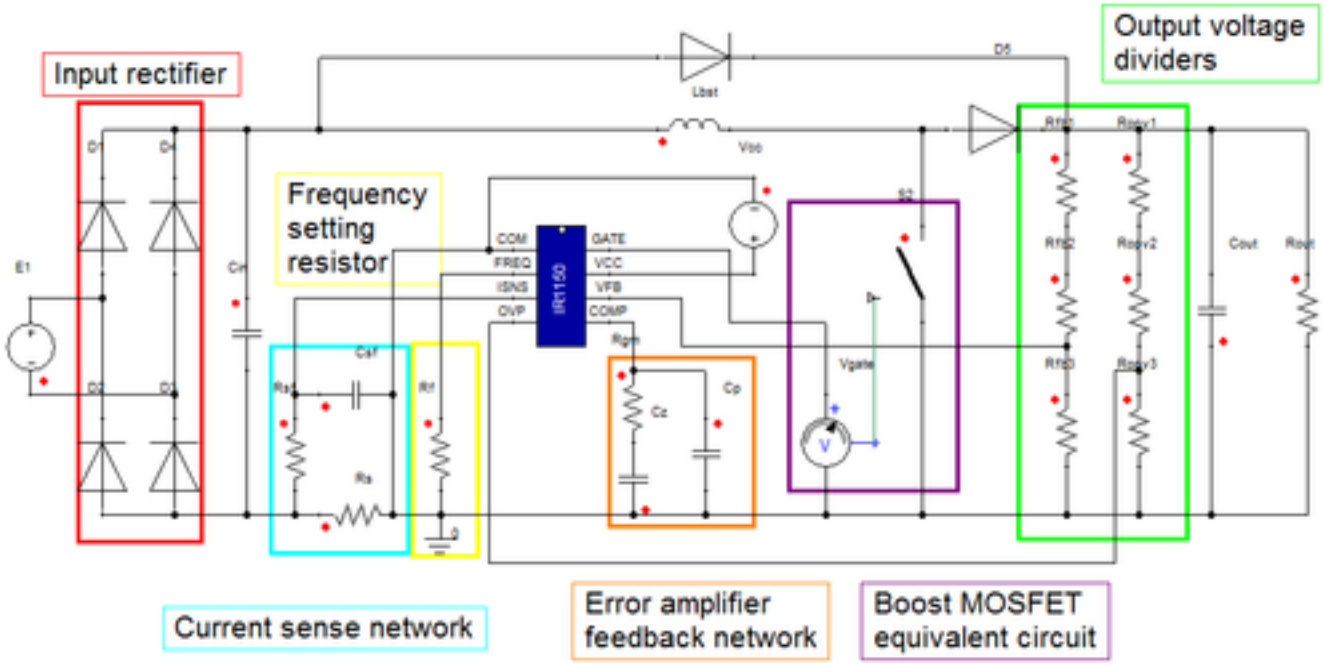

Figure 2. Example Circuit

In this circuit, the IC controls a boost converter with resistive load. The MOSFET has been replaced by an ideal switch.

Simulation results :

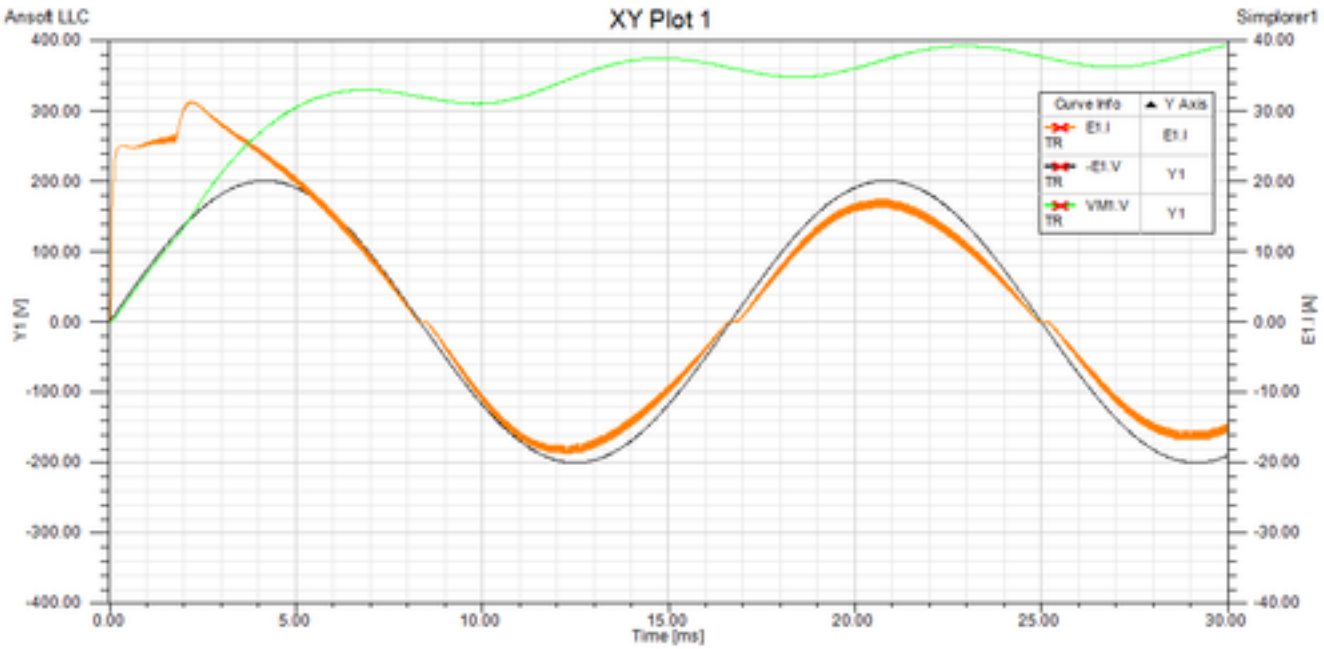

Figure 3. Simulation results

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Orange: source current

Black: source voltage

Green: output voltage

During simulation we get a "convergence failed" on net_227 (voltage loop compensation pin).

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References

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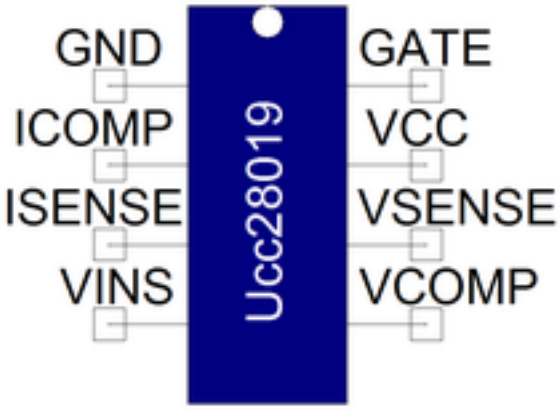
UCC28019: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCC28019* 8-pin active Power Factor Correction (PFC) controller uses the boost topology operating in Continuous Conduction Mode (CCM). The controller is suitable for systems in the 100 W to >2 kW range over a wide-range universal ac line input. Startup current during under-voltage lockout is less than 200 mA. The user can control low power standby mode by pulling the VSENSE pin below 0.77 V.

Low-distortion wave-shaping of the input current using average current mode control is achieved without input line sensing, reducing the Bill of Materials component count. Simple external

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networks allow for flexible compensation of the current and voltage control loops. The switching frequency is internally fixed and trimmed to better than 5% accuracy at 25°C. Fast 1.5-A gate peak current drives the external switch.

Numerous system-level protection features include peak current limit, soft over-current detection, open-loop detection, input brown-out detection, output over-voltage protection/under-voltage detection, a no-power discharge path on VCOMP, and overload protection on ICOMP. Soft-Start limits boost current during start-up. A trimmed internal reference provides accurate protection thresholds and regulation set-point. An internal clamp limits the gate drive voltage to 12.5 V.

The *UCC28019* is a switch-mode controller used in boost converters for power factor correction operating at a fixed frequency in continuous conduction mode. The *UCC28019* requires few external components to operate as an active PFC pre-regulator. Its trimmed oscillator provides a nominal fixed switching frequency of 65 kHz, ensuring that both the fundamental and second harmonic components of the conducted-EMI noise spectrum are below the *EN55022* conducted-band 150-kHz measurement limit.

Its tightly-trimmed internal 5-V reference voltage provides for accurate output voltage regulation over the typical world-wide 85 VAC to 265 VAC mains input range from zero to full output load. The usable system load ranges from 100 W to 2 kW and may be extended in special situations.

Regulation is accomplished in two loops. The inner current loop shapes the average input current to match the sinusoidal input voltage under continuous inductor current conditions. Under extremely light load conditions, depending on the boost inductor value, the inductor current may go discontinuous but still meet Class-D requirements of IEC 1000-3-2 despite the higher harmonics. The outer voltage loop regulates the output voltage on VCOMP (dependent upon the line and load conditions) which determines the internal gain parameters for maintaining a low-distortion steady-state input current waveshape.

State machines are used to model the numerous system-level protections features: Soft over-current, open loop detection, over and under-voltage, EDR function, brown-out detection, peak current limit, etc.

Outputs are modeled with voltage and current sources and inputs with voltage meters. Diodes and switches are also used on the model.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	GND	**Ground:** Device ground reference.
2	ICOMP	**Current loop compensation:** Transconductance current amplifier output. A capacitor connected to GND provides compensation and averaging of the current sense signal in the current control loop. The controller is disabled if the voltage on ICOMP is less than 0.6 V.
3	ISENSE	**Inductor current sense:** An input for the voltage across the external current sense resistor, which represents the instantaneous current through the PFC boost inductor. This voltage is averaged to eliminate the effects of noise and ripple. Soft Over Current (SOC) limits the average inductor current. Cycle-by cycle peak current limit (PCL) immediately shuts off the GATE drive if the peak-limit voltage is exceeded. Use a 220-Ω resistor between this pin and the current sense resistor to limit inrush-surge currents into this pin.
4	VINS	**Input ac voltage sense:** Input Brown Out Protection (IBOP) detects when the system ac-input voltage is above a user-defined normal operating level, or below a user-defined brown-out level. A filtered resistor-divider network connects from this pin to the rectified-mains node. At startup the controller is disabled until the VINS voltage exceeds a threshold of 1.5 V, initiating a soft-start. The controller is also disabled if VINS drops below the brown-out threshold of 0.8 V. Operation will not resume until both VINS and VSENSE voltages exceed their enable thresholds, initiating another soft-start.
5	VCOMP	**Voltage loop compensation:** Transconductance voltage error amplifier output. A resistor-capacitor network connected from this pin to GND provides compensation. VCOMP is held at GND until VCC, VINS, and VSENSE all exceed their threshold voltages. Once these conditions are satisfied, VCOMP is charged until the VSENSE voltage reaches 95% of its nominal regulation level. When the Enhanced Dynamic Response (EDR) is engaged, addi-

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		tional current is applied to VCOMP to reduce the charge time. EDR additional current is inhibited during soft-start. Soft-start is programmed by the capacitance on this pin.
6	VSENSE	**Output voltage sense:** An external resistor-divider network connected from this pin to the PFC output voltage provides feedback sensing for output voltage regulation. A small capacitor from this pin to GND filters high-frequency noise. Standby disables the controller and discharges VCOMP when the voltage at VSENSE drops below the enable threshold of 0.8V. An internal 100nA current source pulls VSENSE to GND for Open-Loop Protection (OLP), including pin disconnection. Output over-voltage protection (OVP) disables the GATE output when VSENSE exceeds 105% of the reference voltage. Enhanced Dynamic Response (EDR) rapidly returns the output voltage to its normal regulation level when a system line or load step causes VSENSE to fall below 95% of the reference voltage.
7	VCC	**Device supply:** External bias supply input. Under Voltage Lock Out (UVLO) disables the controller until VCC exceeds a turn-on threshold of 10.5 V. Operation continues until VCC falls below the turn-off (UVLO) threshold of 9.5 V. A ceramic by-pass capacitor of 0.1 mF minimum value should be connected from VCC to GND as close to the device as possible for high frequency filtering of the VCC voltage.
8	GATE	**Gate drive:** Integrated push-pull gate driver for one or more external power MOSFETs. 2.0-A sink and 1.5-A source capability. Output voltage is clamped at 12.5 V.

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Table 2

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
VCC Bias Supply							
I VCC	Pre-start current	Vcc = Vccon-0.1 V	25	100	200	-	uA
I VCC	Standby current	VSENSE = 0.5 V	1.0	2.1	2.9	2.1	mA
I VCC	Operating current	VSENSE = 4.5 V, CGATE = 4.7 nF	4	7	10		mA
Under Voltage Lockout (UVLO)							
VCC ON	Turn on threshold		10	10.-5	11.-0	10.5	V
VCC OFF	Turn off threshold		9	9.5	10	9.5	V
UVL-O	Hysteresis		0.8	1.0	1.2	1.0	V
Oscillator							
fsw	Switching frequency	TA = 25°C	61.-7	65.-0	68.-3	65	kHz
PWM							
D MIN	Min duty cycle	VCOMP = 0 V, VSENSE = 5 V			0%	0%	
D MAX	Max duty cycle	VSENSE = 4.95 V	9-4%	9-7%	9-9%	97%	
toff	Minimum off time	VSENSE = 3 V, ICOMP = 1 V	100	250	600	250	ns
System Protection							
Vsoc	ISENSE threshold SOC		-0.6-6	-0.7-3	-0.7-9	-0.73	V
Vpcl	ISENSE threshold PCL		-1	-1.0-8	-1.1-5	-1.08	V
Volp	VSENSE threshold OLP	ICOMP = 1 V ISENSE =	0.7-7	0.8-2	0.8-6	0.82	V

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		0 V VCOMP = 1 V					
	OLP pull-down current	VSENSE = 0.5 V		100	250	-	nA
Vuvd	VSENSE threshold UVD		4.6-3	4.7-5	4.8-7	4.75	V
Vovp	VSENSE threshold OVP	ISENSE = -0.2 V	5.1-2	5.2-5	5.3-8	5.25	V
Vins	Input brown-out detection (IBOP) high-to-low threshold		0.7-6	0.8-2	0.8-8	0.82	V
Vins	Input brown-out Detection (IBOP) low-to-high threshold		1.4	1.5	1.6	1.5	V
Ivins	VINS bias current	VINS = 0 V		0	0.1		uA
	ICOMP threshold, external over-load pro-tection			0.6		-	V
Current Loop							
gmi	Transcon-ductance gain	TA = 25°C	0.7-5	0.9-5	1.1-5	0.95	mS
	Output linear range			50		-	uA
	ICOMP (OLP)	VSENSE = 0.5 V	3.7	4.0	4.3	4	V
Voltage Loop							
V REF	Reference		4.9-0	5	5.1-0	5	V
gmv	Transcon-ductance gain		31.-5	42	52.-5	42	uS
	Maximum sink current under normal operation	VSENSE = 6 V, VCOMP = 4 V	21	30	38	42	uA
	Source cur-rent under	VSENSE = 4 V,	-21	-30	-38	-30	uA

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	soft start	VCOMP = 0 V					
	Maximum source current under EDR VSENSE = 4 V, VCOMP = 0 V -100 -170 -250 operation	VSENSE = 4 V, VCOMP = 0 V	-100	-170	-250	-170	uA
		VSENSE = 4 V, VCOMP = 4 V	-60	-100	-140	-100	uA
	EDR VSENSE low threshold, falling		4.6-3	4.7-5	7.8-7	4.75	V
	VSENSE input bias current	1 V ≤ VSENSE ≤ 5 V		100	250	0	nA
	VCOMP (OLP)	VSENSE = 0.5 V, IVCOMP = 0.5 mA	0	0.2	0.4	0	V
GATE Driver							
	GATE current, peak, sinking	CGATE = 4.7 nF		2.0		1.7	A
	GATE current, peak, sourcing	CGATE = 4.7 nF		-1.5		-1.06	A
	GATE rise time	CGATE = 4.7 nF, GATE = 2 V to 8 V		40	60	40	ns
	GATE fall time	CGATE = 4.7 nF, GATE = 8 V to 2 V		25	40	25	ns
	GATE low voltage, no load	GATE = 0 A		0	0.0-5	0	V
	GATE low voltage, sinking	GATE = 20 mA		0.3	0.8	0.17	V
	GATE low	GATE = -		-	-0.8	-0.17	V

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	voltage, sourcing	20 mA		0.3			
	GATE low voltage, sinking	VCC = 5 V, GATE = 5 mA	0.2	0.7-5	1.2	0.04	V
	GATE low voltage, sinking	VCC = 5 V, GATE = 20 mA	0.2	0.9	1.5	0.17	V
	GATE high voltage	VCC = 20 V, CGATE = 4.7 nF	11	12.-5	14	20	V
	GATE high voltage	VCC = 11 V, CGATE = 4.7 nF	9.5	10.-5	11	11	V
	GATE high voltage	VCC = VCCOFF + 0.2 V, CGATE = 4.7 nF	8	9	10.-2	-	V

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Example circuit :

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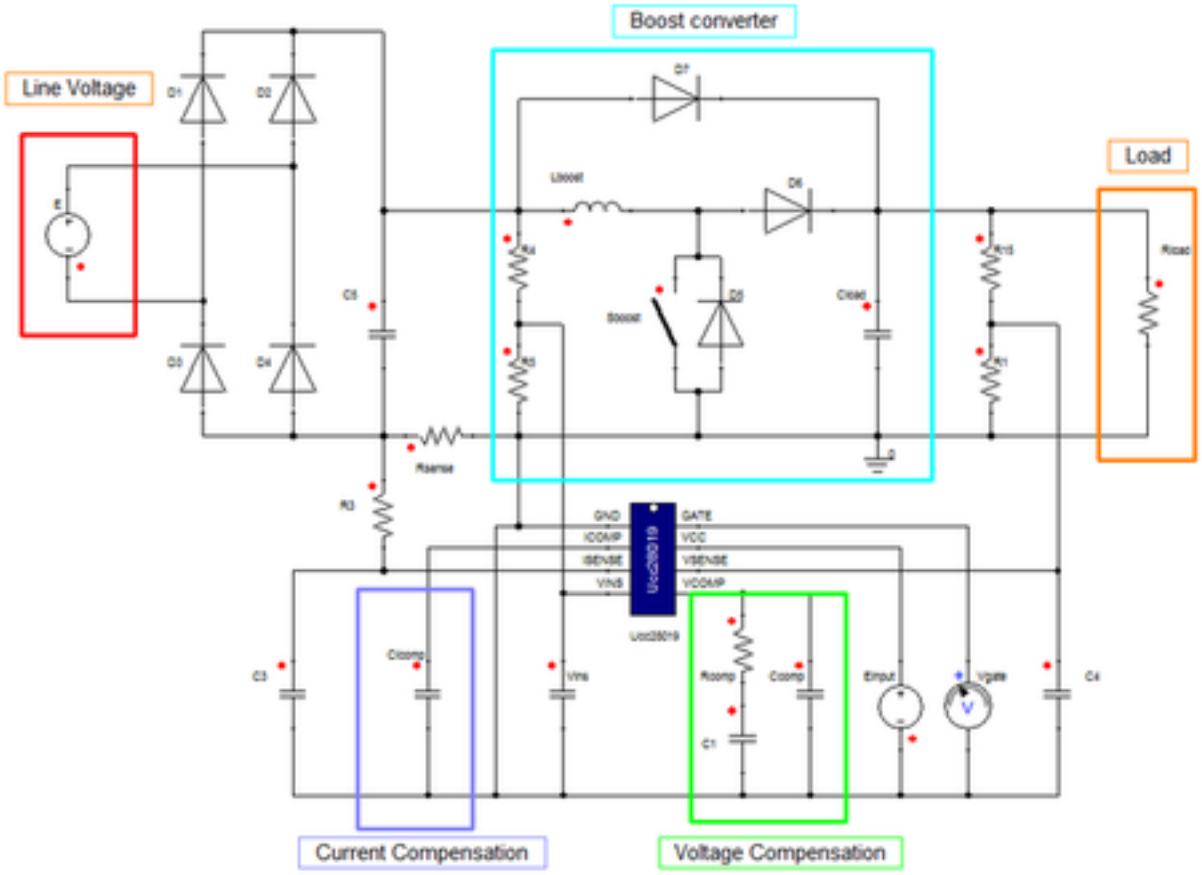

Figure 2. Example Circuit

Simulation results :

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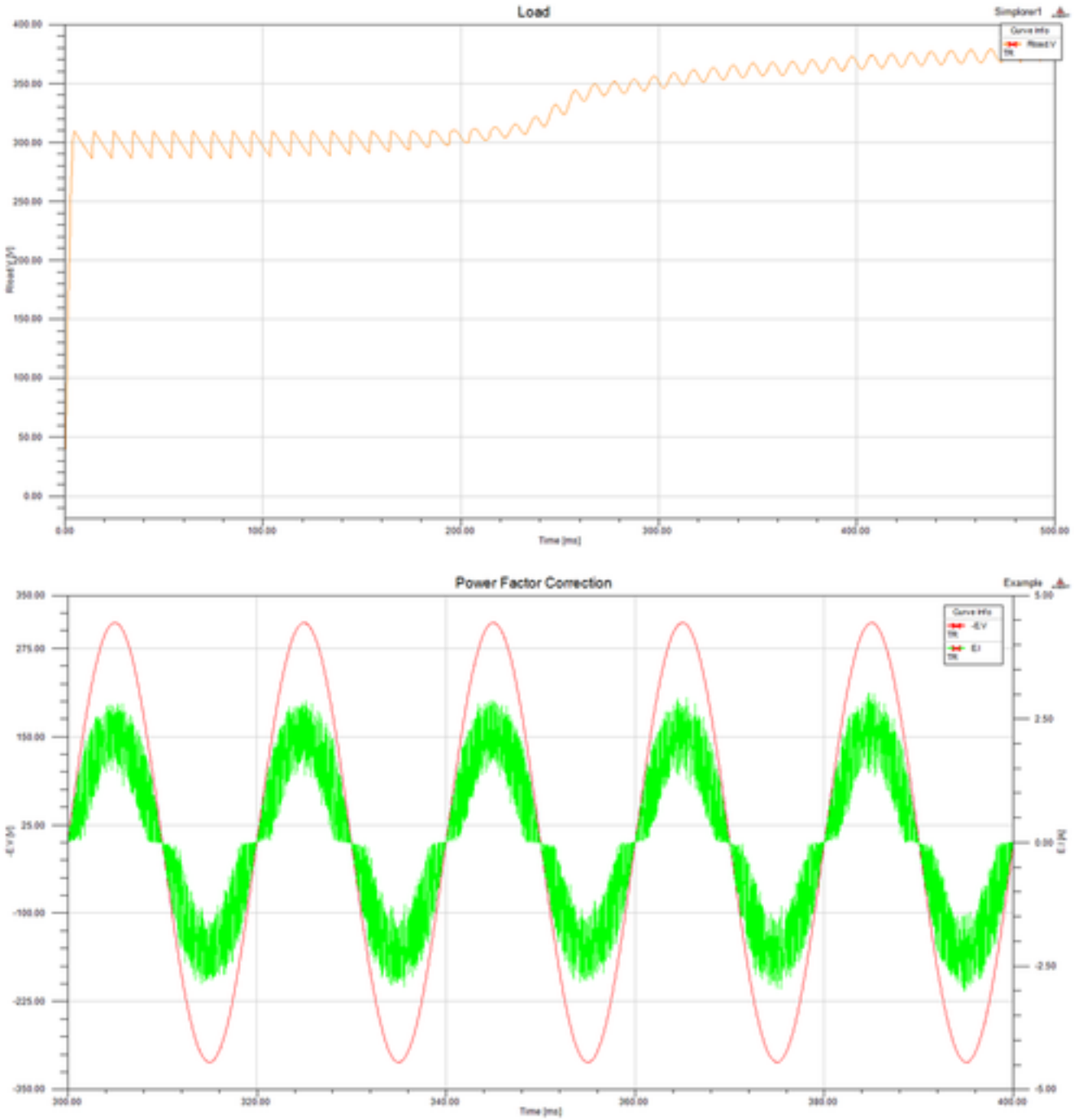

Figure 3. Simulation results

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References

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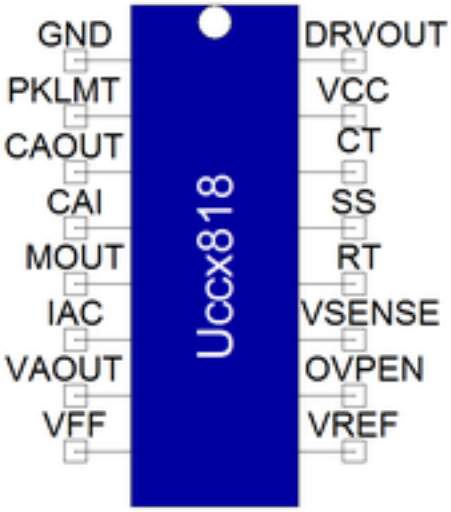
UCCx818: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCC2818* and *UCC3818* provide all the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the ac input line current waveform to correspond to that of the ac input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

Designed in Unitrode's BICMOS process, the *UCC2818* offers new features such as lower start-up current, lower power dissipation, over-voltage protection, a shunt UVLO detect circuitry, a

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leading-edge modulation technique to reduce ripple current in the bulk capacitor and an improved, low-offset (2mV) current amplifier to reduce distortion at light load conditions.

UCC2818 is intended for applications with a fixed supply (VCC).

The model consists of state machines to model internal logic, operational amplifiers and voltage sources and voltmeters to model inputs and outputs.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	GND	Ground.
2	PKLMT	Peak current limit
3	CAOUT	Current amplifier output
4	CAI	Current non-inverting input
5	MOUT	Multiplier output and current amplifier inverting input
6	IAC	Input AC current
7	VAOUT	Voltage amplifier output
8	VFF	Feed-forward signal
9	VREF	Voltage reference output
10	OVP/EN CT	Over-voltage/enable
11	VSENSE	Voltage amplifier inverting input
12	RT	Oscillator charging current
13	SS	Soft start
14	CT	Oscillator timing capacitor

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15	VCC	Positive supply voltage
16	DRVOUT	Gate drive

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Parameters

Comparison between model and real component.

Table 2

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Supply Current Section						
Supply current, off	V_{CC} = (V_{CC} turn-on threshold - 0.3V)		150	300	0	uA
Supply current, on	V_{CC} = 12 V. No load on DRVOUT	2	4		4	mA
UVLO Section						
VCC turn-on threshold		9.7	10.2	10.8	10.2	V
VCC turn-off threshold		9.4	9.7		9.7	V
UVLO hysteresis		0.3	0.5		0.5	V
Voltage Amplifier Section						
Input Voltage	T_A = 0°C to 70°C	7.387	7.5	7.613	7.5	V
	T_A = -40°C to 85°C	7.369	7.5	7.631	7.5	V
Vsense bias current	V_{SENSE} = V_{REF} ; V_{AOUT} = 2.5V		50	200	0	nA
Open loop gain	Vaout = 2V to 5V	50	90		90	dB
V_{OUT} high	I_L = -150uA	5.3	5.5	5.6	5.5	V
V_{OUT} high	I_L = 150uA	0	50	150	50	mV
Over Voltage Protection and Enable Section						
Over voltage ref-		0.48	0.50	0.52	-	V

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erence						
PARAMET-ER	**TEST CONDITIO-NS**	**MIN**	**TYP**	**MAX**	**MODE-L**	**UNIT-S**
Hysteresis			500		0	mV
Enable threshold		1.7	1.9	2.1	1.9	V
Enable hys-teresis		0.1	0.2		0	V
Current Amplifier Section						
Input offset voltage	V_{CM} = 0 V ; V_{CAOUT} = 3 V	-2	0	2	0	mV
Input bias current	V_{CM} = 0 V ; V_{CAOUT} = 3 V		-50	-100	0	nA
Input offset current	V_{CM} = 0 V ; V_{CAOUT} = 3 V		25	100	0	nA
Open loop gain	V_{CM}=0V; V_{CAOUT}=2V to 5V		90		90	dB
CMRR	V_{CM}=0V to 1.5V; V_{CAOUT}=3V	60	80		80	dB
V_{OUT} high	I_L = -120uA	5.6	6.3	6.8	6.5	V
V_{OUT} low	I_L = 1mA	0.1	0.2	0.5	0.5	V
Gain band-width product			2.5		2.5	Mhz
Voltage Reference Section						
Input voltage	T_A = 0°C to 70°C	7.387	7.5	7.61	7.5	V
	T_A = -40°C to 85°C	7.369	7.5	7.63	7.5	V
Load reg-ulation	I_{REF} = 1 mA to 2 mA	0	3	10	3	mV
Line reg-ulation	V_{CC} = 10.8 V to 15 V	0	20	50	0	mV
Short circuit current	V_{REF} = 0 V	-20	-25		-25	mA
Oscillator Section						
Initial accur-acy	T_A = 25°C	85	100	115	91	kHz
Voltage sta-	VCC = 10.8	-1		1	-	%

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bility	V to 15 V					
Total variation	Line, Temp	80		120	-	kHz
Ramp peak voltage		4.5	5	5.5	5	V
Ramp amplitude voltage	(peak to peak)	3.5	4	4.5	4	V
Peak Current Limit Section						
PKLMT reference voltage		-15		15	-	mv
PKLMT propagation delay		150	350	500	-	ns
Multiplier Section						
High line, low power	I_{AC} = 500 uA ; V_{FF} = 4.7 V ; V_{AOUT} = 1.25 V	0	-6	-20	-5.7	uA
High line, high power	I_{AC} = 500 uA ; V_{FF} = 4.7 V ; V_{AOUT} = 5 V	-75	-90	-110	-90	uA
Low line, low power	I_{AC} = 150 uA ; V_{FF} = 1.4 V ; V_{AOUT} = 1.25 V	-10	-19	-50	-19	uA
Low line, high power	I_{AC} = 150 uA ; V_{FF} = 1.4 V ; V_{AOUT} = 5 V	-260	-300	-360	-306	uA
IAC limited	I_{AC} = 150 uA ; V_{FF} = 1.3 V ; V_{AOUT} = 5 V	-250	-300	-400	-300	uA
Gain constant (K)	I_{AC} = 300 uA ; V_{FF} = 3 V ; V_{AOUT} = 2.5 V	0.5	1	1.5	1	uA
Zero current	I_{AC} = 150 uA ; V_{FF} = 1.4 V ; V_{AOUT} = 0.25 V		0	-2	0	uA

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	I_{AC} = 500 uA ; V_{FF} = 4.7 V ; V_{AOUT} = 0.25 V		0	-2	0	uA
	I_{AC} = 500 uA ; V_{FF} = 4.7 V ; V_{AOUT} = 0.5 V		0	-3	0	uA
Power limit	I_{AC} = 150 uA ; V_{FF} = 1.4 V ; V_{AOUT} = 5 V	-360	-420	-500	-420	uW
PARAMET-ER	**TEST CONDITIO-NS**	**MIN**	**TYP**	**MAX**	**MODE-L**	**UNIT-S**
Feed-Forward Section						
VFF output current	Iac=300uA	-140	-150	-160	-150	uA
Soft Start Section						
SS charge current		-6	-10	-16	-10	uA
Gate Driver Section						
Pull up res-istance	I_O = -100 mA		7	12	7	Ohm
Pull down resistance	I_O = 100 mA		3	10	3	Ohm
Output rise time	C_L = 1nF ; R_L =10 ohm		25	50	25	ns
Output fall time	C_L = 1nF ; R_L =10 ohm		10	50	10	ns
Maximum duty cycle		93	95	100	92	%
Zero Power Section						
Zero power comparator threshold	Measured on Vaout	0.2	0.33	0.50	0.33	V

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Example circuit :

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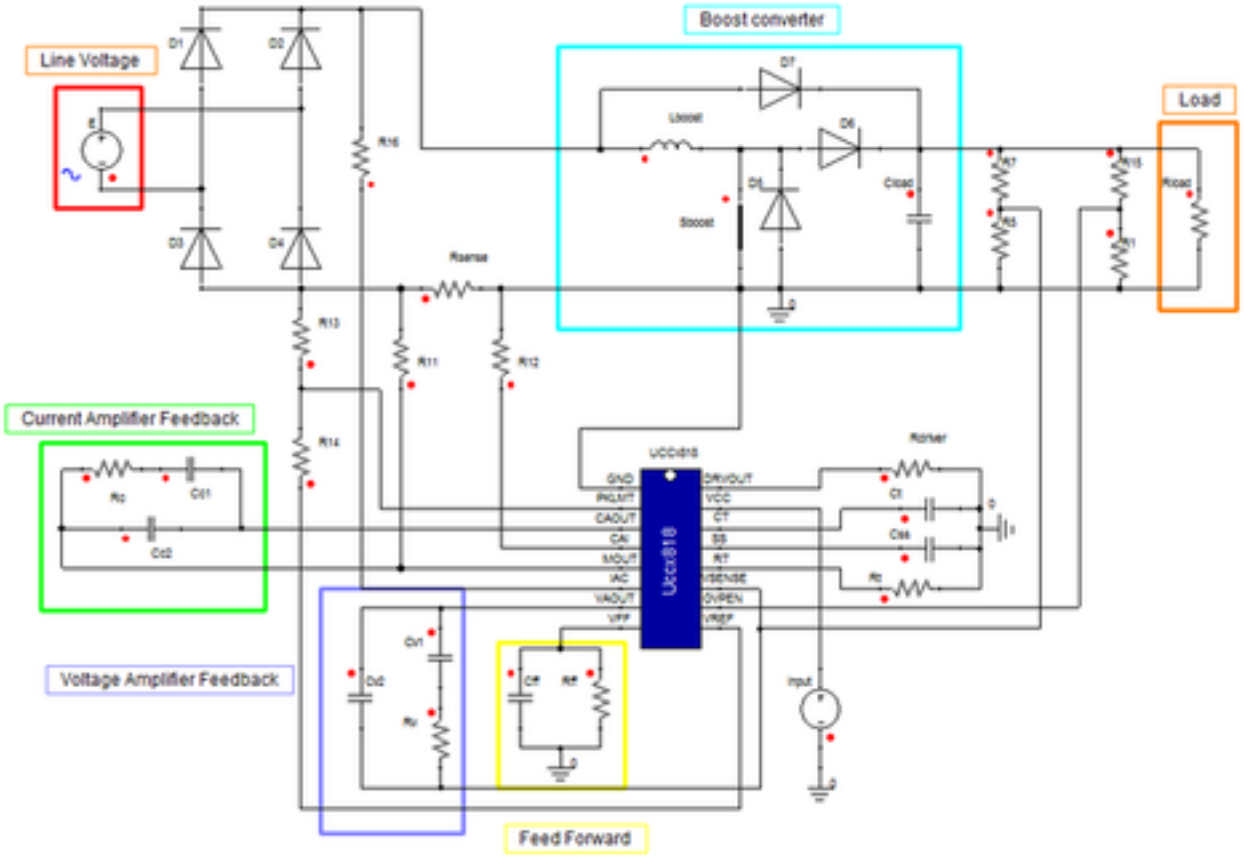

Figure 2. Example Circuit

Simulation results :

Output Voltage :

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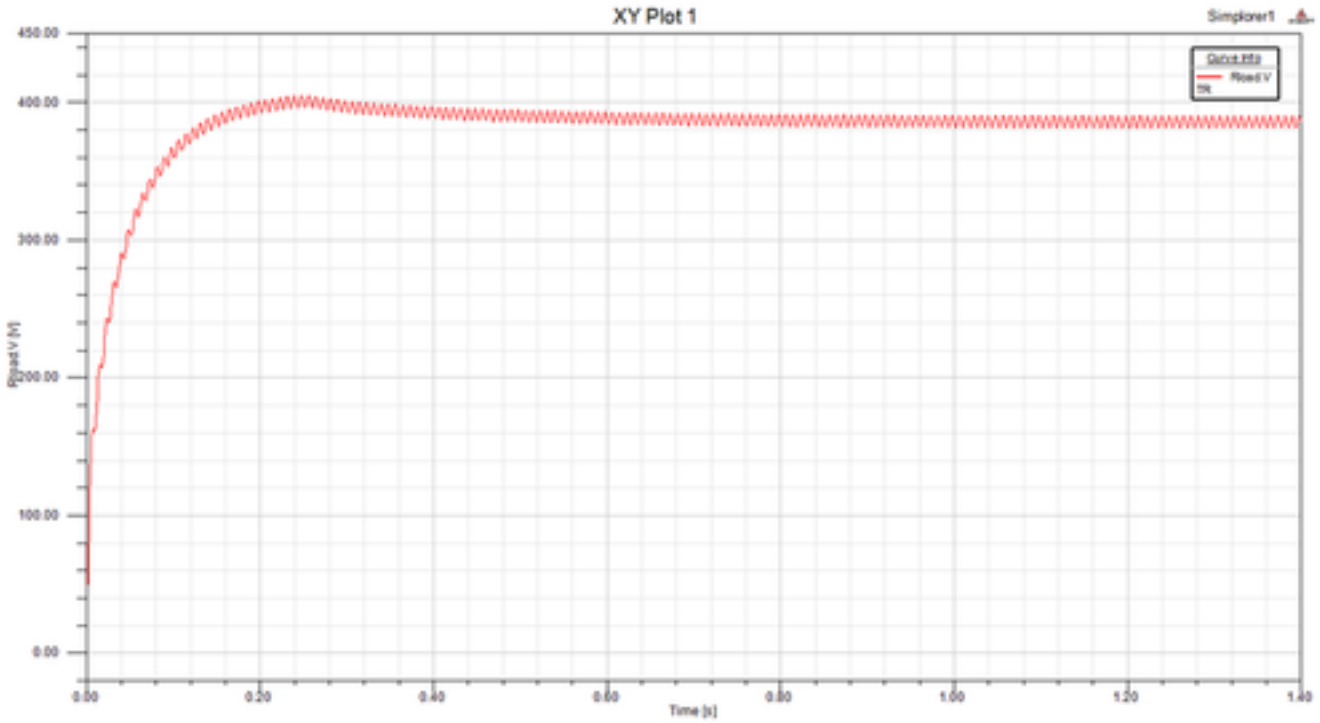

Power factor correction:

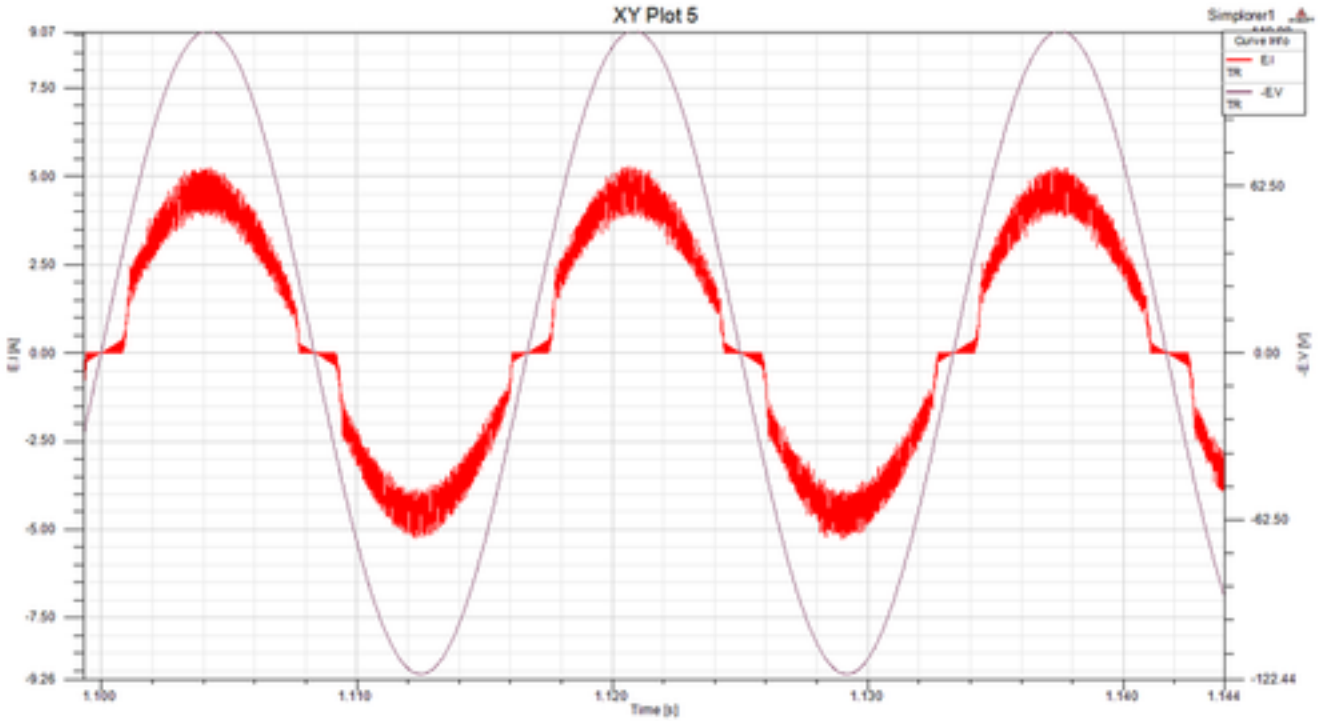

Figure 3. Simulation results

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UCx854: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

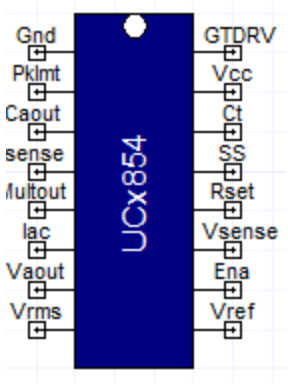

Figure 1. Component symbol

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Description

The *UCC1854* provides active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. To do this, the *UCC1854* contains a voltage amplifier, an analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the *UCC1854* contains a power MOSFET compatible gate driver, 7.5V reference, line anticipator, load-enable comparator, low-supply detector, and over-current comparator.

The *UCC1854* uses average current-mode control to accomplish fixed frequency current control with stability and low distortion. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients.

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The *UCC1854*'s high reference voltage and high oscillator amplitude minimize noise sensitivity while fast PWM elements permit chopping frequencies above 200kHz. The *UCC1854* can be used in single and three phase systems with line voltages that vary from 75 to 275 volts and line frequencies across the 50Hz to 400Hz range. To reduce the burden on the circuitry that supplies power to this device, the *UCC1854* features low starting supply current.

The model consist of state machines to model internal logic, operational amplifiers and transconductance amplifiers (modeled by a controlled current source) and voltage sources and voltmeters to model inputs and outputs.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	GND	Ground
2	PKLMT	Peak CurrentLimit
3	CA Out	Current Amplifier Output
4	ISENSE	Current Sense Input
5	Mult Out	Multiplier Output
6	Iac	Current
7	VA Out	Voltage Amplifier Output
8	Vrms	
9	Vref	Voltage Reference
10	ENA	Enable
11	Vsense	
12	Rset	
13	SS	Soft Start
14	Ct	Timing Capacitor
15	Vcc	Voltage Supply
16	GT Drv	Gate Driver

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Parameters

Comparison between model and real component.

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Table 2

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
OVERALL						
Supply Current, Off	ENA=0V		1.5	2.0		mA
Supply Current, On			10	16		mA
Vcc Turn-on Threshold		14.5	16	17.5	16	V
Vcc Turn-off Threshold		9	10	11	10	V
ENA Threshold, Rising		2.4	2.55	2.7	2.55	V
ENA Threshold Hysteresis		0.2	0.25	0.3	0.25	V
ENA Input Current	ENA=0V	-5.0	-0.2	5.0	-0.2	uA
Vrms Input Current	Vrms=5V	-1.0	-0.01	1.0	0	uA
VOLTAGE AMPLIFIER						
Voltage Amp Offset Voltage	VA Out=5V	-8		8	0	mV
Vsense Bias Current		-500	-25	500	0	nA
Voltage Amp Gain		70	100		100	dB
Voltage Amp Output Swing			0.5/5.-8		0.5/5.8	V
Voltage Amp Short Circuit Current	VA Out=0V	-36	-20	-5	-20	mA
SS Current	SS=2.5V	-20	-14	-6	-14	uA
CURRENT AMPLIFIER						
Current Amp Offset Voltage		-4		4	0	mV

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Isense Bias Current		-500	-120	500	0	nA
Input Range, Isense, Mult Out		-0.3/2.-5			-0.3/2.5	V
Current Amp Gain		80	110		110	dB
Current Amp Out-put Swing			0.5/16		0.5/16	V
Current Amp Short Circuit Cur-rent	CA Out=0V	-36	-20	-5	-20	mA
Current Amp Gain-BW Product	CA Out=0V	400	800		-	kHz
REFERENCE						
Ref Output Voltage	IREF=0mA, TA=25oC	7.4	7.5	7.6	7.5	V
	IREF=0mA, OverTemp	7.35	7.5	7.65	7.5	V
Vref Load Regulation	Iref=10mA	-15	5	15	5	mV
Vref Line Regulation	15V<VCC <35V	-10	2	10	0	mV
Vref Short Circuit Cur-rent	REF=0V	-50	-28	-12	-28	mA
MULTIPLIER						
Mult Out Current Iac Limited	IAC =100mA, RSET=10k, VRMS =1.25V	-220	-200	-180	-200	uA
PARAMET-ER	**TEST CONDITIO-NS**	**MIN**	**TYP**	**MA-X**	**MODE-L**	**UNIT-S**
Mult OutCurrent Zero	IAC=0mA, RSET=15k	-2.0	-0.2	2.0	-0.2	uA
Mult Out Current RSET Lim-ited	IAC =450mA, RSET=15k, VRMS=1V, VA Out =	-280	-255	-220	-255	uA

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	6V					
Mult OutCurrent	IAC=50mA, VRMS=2V, VA=4V	-50	-42	-33	-42	uA
	IAC =100mA, VRMS=2V, VA=2V	-38	-27	-12	-27	uA
	IAC =200mA, VRMS=2V, VA=4V	-165	-150	-105	-150	uA
	AC =300mA, VRMS=1V, VA=2V	-250	-225	-150	-255	uA
	IAC =100mA, VRMS=1V, VA=2V	-95	-80	-60	-80	uA
Multiplier GainCon-stant			-1.0		-1	V
OSCILLATOR						
Oscillator Frequency	RSET=15k	46	55	62	55	kHz
	RSET=8.2k	86	102	118	102	kHz
CT Ramp Peak-to-Valley Amplitude		4.9	5.4	5.9	5.4	V
CT Ramp Valley Voltage		0.8	1.1	1.3	1.1	V
GATE DRIVER						
Maximum GT Drv Out-put Voltage	0mA load on GT Drv, 18V<VCC <35V	13	14.5	18	Vcc	V
GT Drv Out-put Voltage High	-200mA load on GT Drv, VCC=15V	12	12.8		13.6	V
GT Drv Out-put Voltage Low, Off	VCC=0V, 50mA load on GT Drv		0.9	1.5	0	V
GT Drv Out-	200mA		1.0	2.2	0	V

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put Voltage Low	load on GT Drv					
	10mA load on GT Drv		0.1	0.4	0	V
Peak GT DrvCurrent	10nF from GT DrvtoGnd		1.0		-	A
GT Drv Rise/Fall Time	1nF from GT DrvtoGnd		35		35	ns
GT Drv Maximum Duty Cycle	VCA Out=7V		95		100	%
CURRENT LIMIT						
PKLMT Off-set Voltage			-10		-10	mV
PKLMT Input Cur-rent	PKLMT=-0.1V		-200	-100	0	uA
PKLMT to GT Drv Delay	PKLMT fall-ing from 50mV to -50mV			175	175	ns

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Example circuit :

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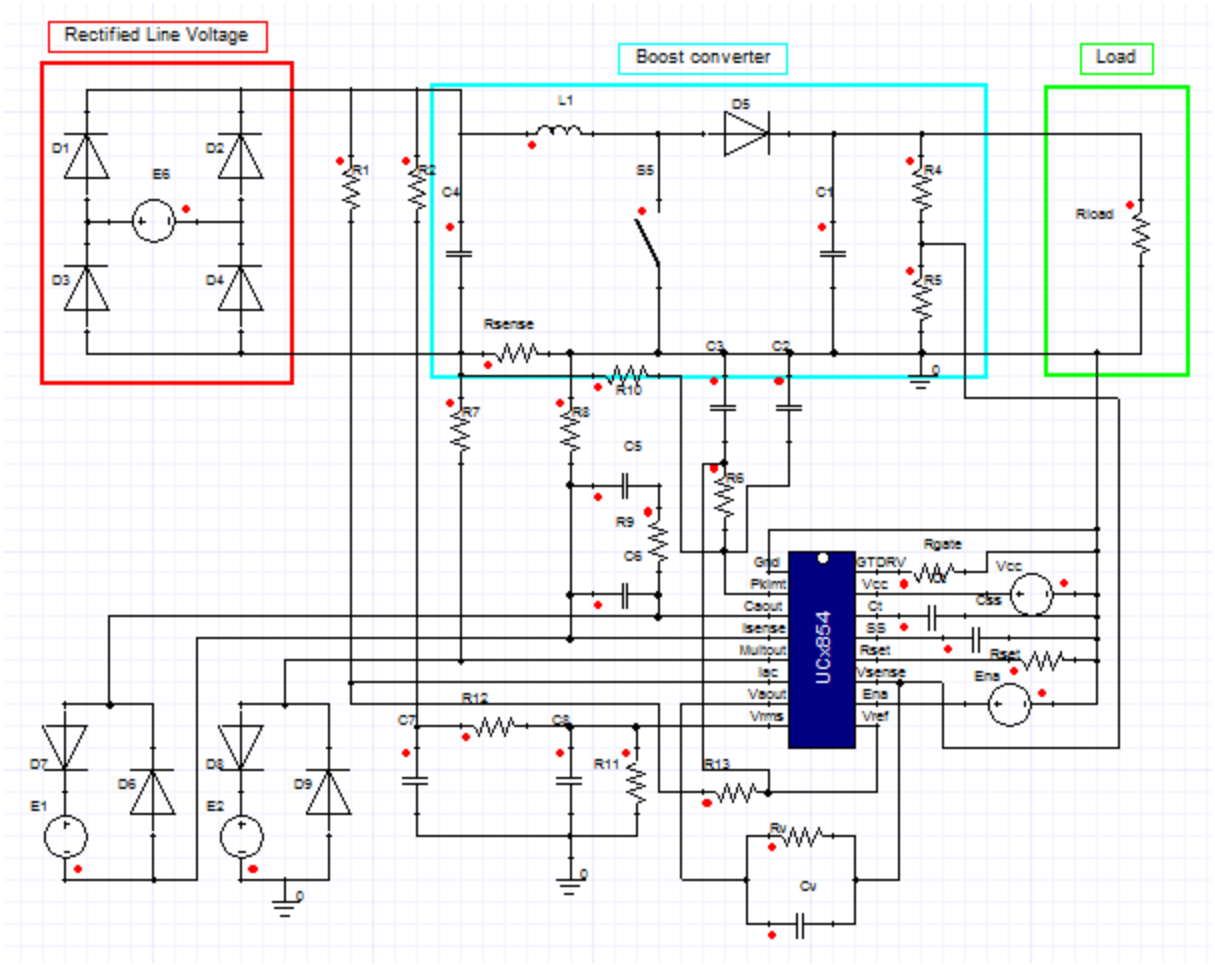

Figure 2. Example Circuit

Simulation results (Output Voltage):

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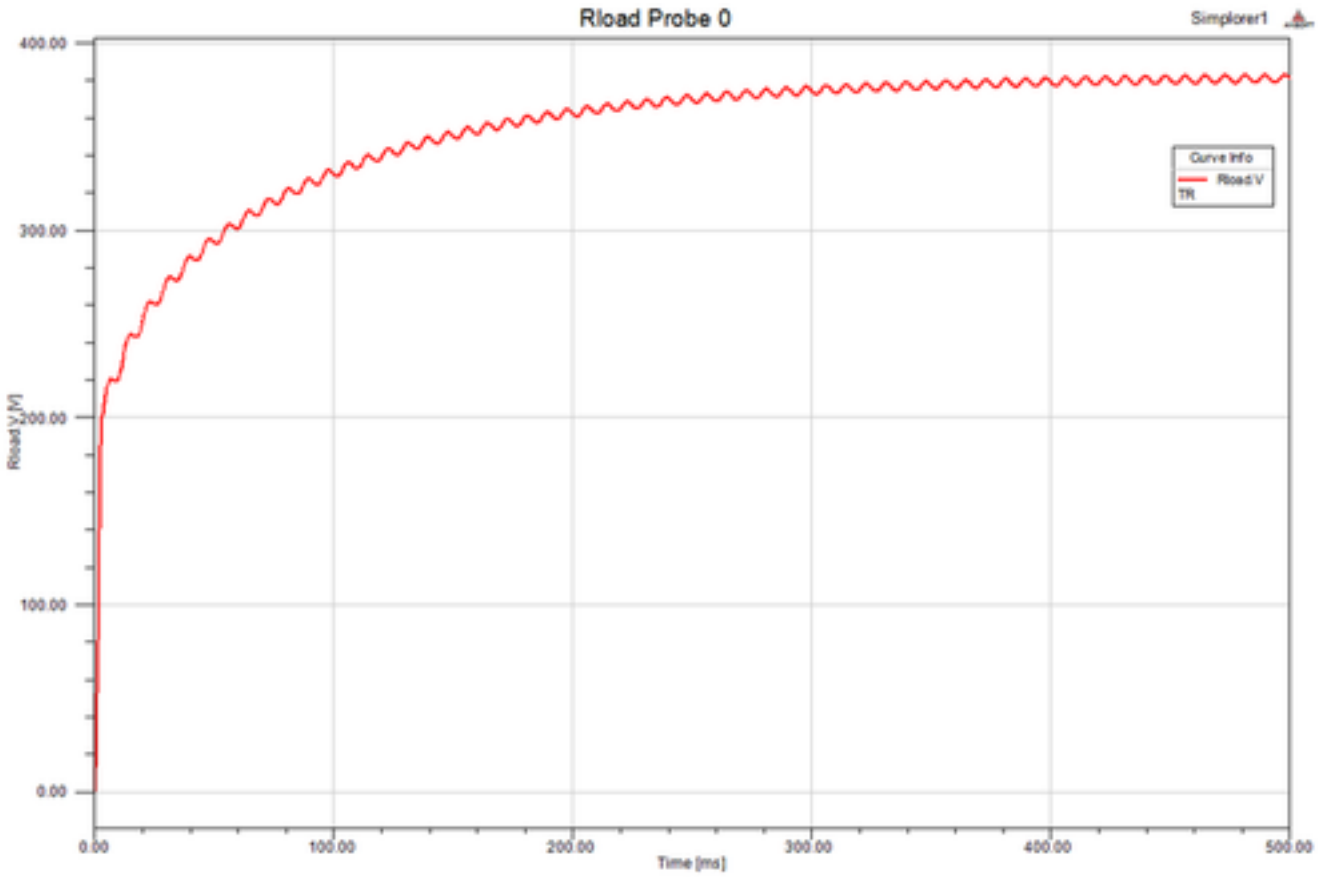

Figure 3. Simulation results

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References

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Protection

Protection consists of the following types of models:

• LT4356_1

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LT4356_1: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

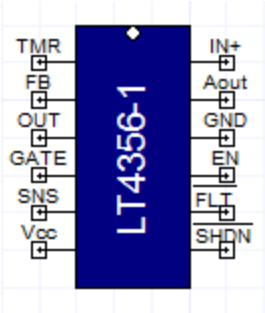

Figure 1. Component symbol

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Description

The LT4356 surge stopper protects loads from high voltage transients. It regulates the output during an overvoltage event, such as load dump in automobiles, by controlling the gate of an external N-channel MOSFET. The output is limited to a safe value thereby allowing the loads to continue functioning. The LT4356 also monitors the voltage drop between the VCC and SNS pins to protect against overcurrent faults. An internal amplifier limits the current sense voltage to 50mV. In either fault condition, a timer is started inversely proportional to MOSFET stress. If the timer expires, the FLT pin pulls low to warn of an impending power down. If the condition persists, the MOSFET is turned off. After a cool down period, the GATE pin pulls up turning on the MOSFET again.

The auxiliary amplifier may be used as a voltage detection comparator or as a linear regulator controller driving an external PNP pass transistor.

Back-to-back FETs can be used in lieu of a Schottky diode for reverse input protection, reducing voltage drop and power loss. A shutdown pin reduces the quiescent current to less than 7µA for

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the LT4356-1 during shutdown. The LT4356-2 differs from the LT4356-1 during shutdown by reducing the quiescent current to 60µA and keeping alive the auxiliary amplifier for uses such as an under voltage lockout or always-on regulator.

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Table 1

Name	Description
Aout	Amplifier Output. Open collector output of the auxiliary amplifier. It is capable of sinking up to 2mA from 80V. The negative input of the amplifier is internally connected to a 1.25V reference.
EN	Open-Collector Enable Output. The EN pin goes high impedance when the voltage at the OUT pin is above (VCC – 0.7V), indicating the external MOSFET is fully on. The state of the pin is latched until the OUT pin voltage resets at below 0.5V and goes back up above 2V. The internal NPN is capable of sinking up to 3mA of current from 80V to drive an LED or opto-coupler.
FB	Voltage Regulator Feedback Input. Connect this pin to the center tap of the output resistive divider connected between the OUT pin and ground. During an overvoltage condition, the GATE pin is servoed to maintain a 1.25V threshold at the FB pin. This pin is clamped internally to 7V. Tie to GND to disable the OV clamp
notFLT	Open-Collector Fault Output. This pin pulls low after the voltage at the TMR pin has reached the fault threshold of 1.25V. It indicates the pass transistor is about to turn off because either the supply voltage has stayed at an elevated level for an extended period of time (voltage fault) or the device is in an overcurrent condition (current fault). The internal NPN is capable of sinking up to 3mA of current from 80V to drive an LED or opto-coupler.
GATE	N-Channel MOSFET Gate Drive Output. The GATE pin is pulled up by an internal charge pump current source and clamped to 14V above the OUT pin. Both voltage and current amplifiers control the GATE pin to regulate the output voltage and limit the current through the MOSFET.
GND	Device Ground.
IN+	Positive Input of the Auxiliary Amplifier. This amplifier can be used as a level detection comparator with external hysteresis or linear regulator controlling an external PNP transistor. This pin is clamped internally to 7V. Connect to ground if unused.
OUT	Output Voltage Sense Input. This pin senses the voltage at the source of the N-channel MOSFET and sets the fault timer current. When the OUT pin voltage reaches

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	0.7V away from VCC, the EN pin goes high impedance.
notSHDN	Shutdown Control Input. The LT4356 can be shut down to a low current mode by pulling the SHDN pin below 0.4V. Pull this pin above 2.1V or disconnect it and allow the internal current source to turn the part back on. The leakage current to ground at the pin should be limited to no more than 1µA if no pull up device is used to turn the part on. The SHDN pin can be pulled up to 100V or below GND by 60V without damage. In shutdown, the auxiliary amplifier turns off in the LT4356-1 but continues operating in the LT4356-2.
SNS	Current Sense Input. Connect this pin to the output of the current sense resistor. The current limit circuit controls the GATE pin to limit the sense voltage between VCC and SNS pins to 50mV. At the same time the sense amplifi er also starts a current source to charge up the TMR pin. This pin can be pulled below GND by up to 60V, though the voltage difference with the VCC pin must be limited to less than 30V. Connect to VCC if unused.
TMR	Fault Timer Input. Connect a capacitor between this pin and ground to set the times for early warning, fault and cool down periods. The current charging up this pin during fault conditions depends on the voltage difference between the VCC and OUT pins. When VTMR reaches 1.25V, the FLT pin pulls low to indicate the detection of a fault condition. If the condition persists, the pass transistor turns off when VTMR reaches the threshold of 1.35V. As soon as the fault condition disappears, the pull up current stops and a 2µA current starts to pull the TMR pin down. When VTMR reaches the retry threshold of 0.5V, the GATE pin pulls high turning back on the pass transistor.
Vcc	Positive Supply Voltage Input. The positive supply input ranges from 4V to 80V for normal operation. It can also be pulled below ground potential by up to 60V during a reverse battery condition, without damaging the part. The supply current is reduced to 7µA with all the functional blocks off.

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Example:

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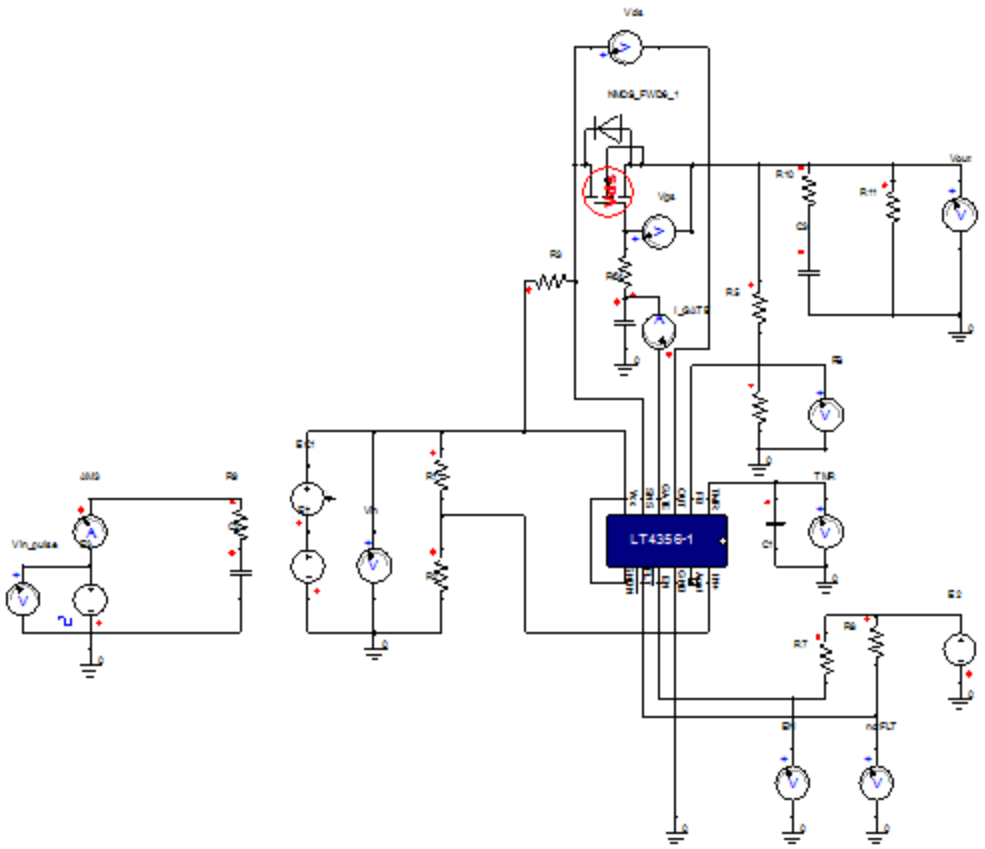

Figure 2. Example connection 4A, 12V Overvoltage Output Regulator

Simulation – signal diagrams

Figure 3 shows the transient waveforms of the main signal voltages; figure 4 shows the transient waveforms of the input and output voltages of the LT4356.

The first part of the transient corresponds to normal operation. The main switch is closed and the output voltage is equal to the input voltage. The EN pin and notFLT pin go to high impedance.

At t=100ms, there is an overvoltage fault created. The gate of the external mosfet is controlled to limit the output voltage to a safe value. When the voltage of the TMR pin reaches 1.25V the notFLT pin pulls low. . As the condition persists and the TMR pin voltage reaches 1.35V, the pass transistor turns off, and starting the cool down period.

After the fault condition has disappeared and a cool down period has transpired at 155ms, the GATE pin starts to pull high again.

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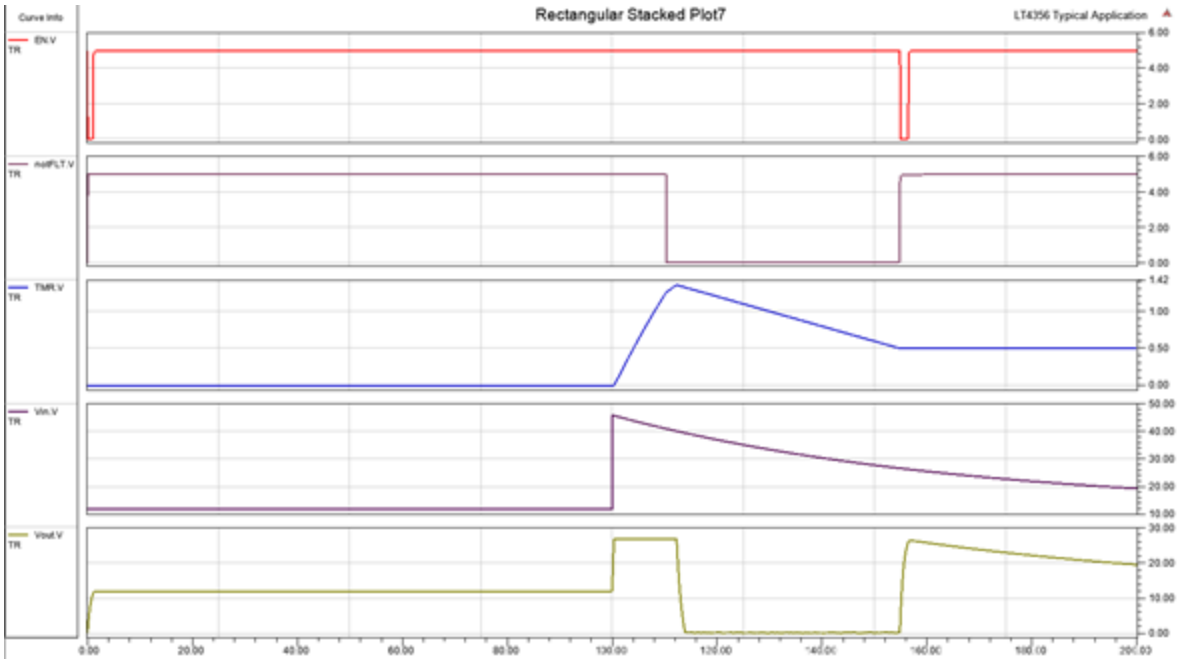

Figure 3. Main Signal Voltages

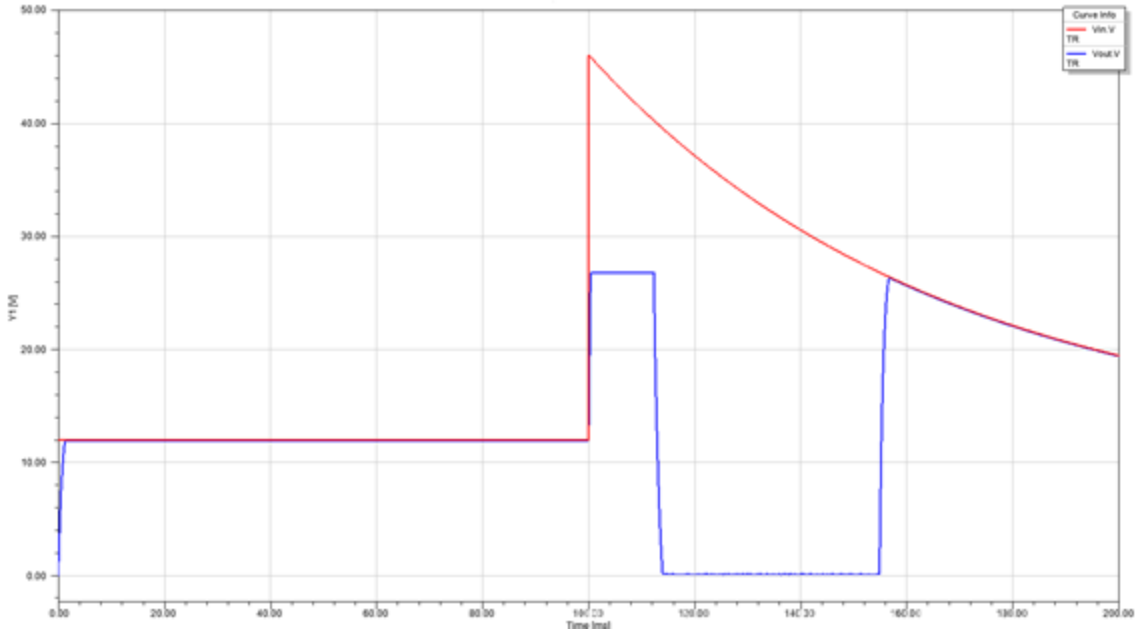

Figure 4. Input and Output Voltage

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References

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PWM Controllers

The PWM Controllers consist of the following types of models:

- ADP1821
- ADP1822
- ADP1823
- LM3478
- LM3489
- LT1241
- LT1242
- LT1243
- LT1244
- LT1245
- UCC28950
- UCCx5801
- UCCx5802
- UCCx5803
- UCCx5804
- UCCx800
- UCCx801
- UCCx802
- UCCx803
- UCCx804
- UCCx805
- UCCx806
- UCCx813_0
- UCCx813_1
- UCCx813_2
- UCCx813_3
- UCCx813_4
- UCCx813_5

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- UCCx895
- UCCx8C40
- UCCx8C41
- UCCx8C42
- UCCx8C43
- UCCx8C44
- UCCx8C45
- UCx524
- UCx525
- UCx823
- UCx824
- UCx825
- UCx842
- UCx843
- UCx844
- UCx845
- UCx846
- UCx8741
- UCx8742
- UCx875
- UCx876
- UCx9432

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ADP1821: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

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Description

The *ADP1821* is a versatile and inexpensive, synchronous, pulse-width-modulated (PWM), voltage-mode, step-down controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V. The *ADP1821* can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators.

The *ADP1821* is well suited for a wide range of high power applications, such as DSP and processor core power in telecommunications, medical imaging, high performance servers, and

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industrial applications. It operates from a 3.7 V to 5.5 V supply with a power input voltage ranging from 1.0 V to 24 V.

The *ADP1821* operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost. For noise sensitive applications, it can be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1.2 MHz. The *ADP1821* includes soft start protection to limit the inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET sensing.

The *ADP1821* operates over the -40°C to +125°C junction temperature range and is available in a 16-lead QSOP.

The model consists in states machines to model the logic of the integrated circuit, aswell as the delays and blankings. Voltmeters are used as inputs and sources as outputs.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	BST	High-Side Gate Driver Boost Capacitor Input. A capacitor between SW and BST powers the high-side gate driver, DH. The capacitor is charged through a diode from PVCC when the low-side MOSFET is on. Connect a 0.1 µF or greater ceramic capacitor from BST to SW and a Schottky diode from PVCC to BST to power the high-side gate driver.
2	DH	High-Side Gate Driver Output. Connect DH to the gate of the external high-side, N-channel MOSFET switch. DH is powered from the capacitor between SW and BST, and its voltage swings between VSW and VBST.
3	SW	Power Switch Node. Connect the source of the high-side, N-channel MOSFET switch and the drain of the low-side, N-channel MOSFET synchronous rectifier to SW. SW powers the output

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		through the output LC filter.
4	SYNC	Frequency Synchronization Input. Drive SYNC with an external 300 kHz to 1.2 MHz signal to synchronize the converter switching frequency to the applied signal. The maximum SYNC frequency is limited to 2 times the nominal internal frequency selected by FREQ. Do not leave SYNC unconnected; when not used, connect SYNC to GND.
5	FREQ	Frequency Select Input. FREQ selects the converter switching frequency. Drive FREQ low to select 300 kHz, or high to select 600 kHz. Do not leave FREQ unconnected.
6	SHDN	Active Low, DC-to-DC Shutdown Input. Drive SHDN high to turn on the converter and low to turn it off. Connect SHDN to VCC for automatic startup.
7	PWGD	Open-Drain, Power-Good Output. PWGD sinks current to GND when the output voltage is above or below the regulation voltage. Connect a pull-up resistor from PWGD to VDD for a logical power-good indicator.
8	GND	Analog Ground. Connect GND to PGND at a single point as close as possible to the internal circuitry (IC).
9	SS	Soft Start Control Input. A capacitor from SS to GND controls the soft start period. When the output is overloaded, SS is discharged to prevent excessive input current while the output recovers. Connect a 1 nF capacitor to a 1 µF capacitor from SS to GND to set the soft start period. See the Soft Start section.
10	FB	Voltage Feedback Input. Connect to a resistive voltage divider from the output to FB to set the output voltage. See the Setting the Output Voltage section.
11	COMP	Compensation Node. Connect a resistor-capacitor network from COMP to FB to compensate the regulation control system. See the Compensation section.
12	VCC	Internal Power Supply Input. VCC powers the internal circuitry. Bypass VCC to GND with a 0.1 µF or greater capacitor connected as close as possible to the IC.
13	CSL	Low-Side Current Sense Input. Connect CSL to SW through a resistor to set the current limit. See the Setting the Current Limit section.
14	PGND	Power Ground. Connect GND to PGND at a single point as close as possible to the IC.
15	DL	Low-Side Gate Driver Output. Connect DL to the

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		gate of the low-side, N-channel MOSFET synchronous rectifier. The DL voltage swings between PGND and PVCC.
16	PVCC	Internal Gate Driver Power Supply Input. PVCC powers the low-side gate driver, DL. Bypass PVCC to PGND with a 1 µF or greater capacitor connected as close as possible to the IC.

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
POWER SUPPLY						
Input Voltage		3.7		5.5	5	V
Undervoltage Lockout Threshold	V_{VCC} rising	2.4	2.7	3.0	2.7	V
Undervoltage Lockout Hysteresis			0.1		0.1	V
Quiescent Current			1	2	1	mA
Shutdown Current	SHDN = GND			10	10	uA
Power Stage Supply Voltage		1.0		24	15	V
ERROR AMPLIFIER						
FB Regulation Voltage		594	600	606	600	mV
FB Input Bias Current		-100	1	100	0	nA
Error Amplifier Open-Loop Voltage Gain			70		70	dB
COMP Output Sink Current			600		-	uA
COMP Output Source Current			110		-	uA

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COMP Clamp High Voltage			2.4		2.4	V
COMP Clamp Low Voltage			0.75		0.75	V
PWM CONTROLLER						
PWM Peak Ramp Voltage			1.25		1.25	V
DL Minimum On Time	FREQ-Q=GND (300 kHz)	120	170	220	170	ns
DL Maximum On Time	FREQ-Q=GND (300 kHz)	140	170	200	170	ns
DH Maximum Duty Cycle	FREQ-Q=GND (300 kHz)	85	90		95	%
DH Minimum Duty Cycle	FREQ-Q=GND (300 kHz)		1	3	0	%
SOFT START						
SS Pull-Up Resistance	SS = GND		95		100	kohm
SS Pull-Down Resistance	V_{SS} = 0.6 V	1.65	2.5	4.2	2.5	kohm
OSCILLATOR						
Oscillator Frequency	FREQ-Q=GND	250	310	375	310	kHz
	FREQ-Q=VCC	470	570	720	570	kHz
Synchronization Range	FREQ-Q=GND	300		600	-	kHz
	FREQ-Q=VCC	600		1200	-	kHz
SYNC Minimum Pulse Width				80	80	ns
CURRENT SENSE						
CSL Threshold	Relative to PGND	-30		30		mV

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Voltage						
CSL Output Current	V_{CSL} = 0 V	42	50	54	50	uA
Current Sense Blank-ing Period			160		160	ns

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Examples

Example circuit :

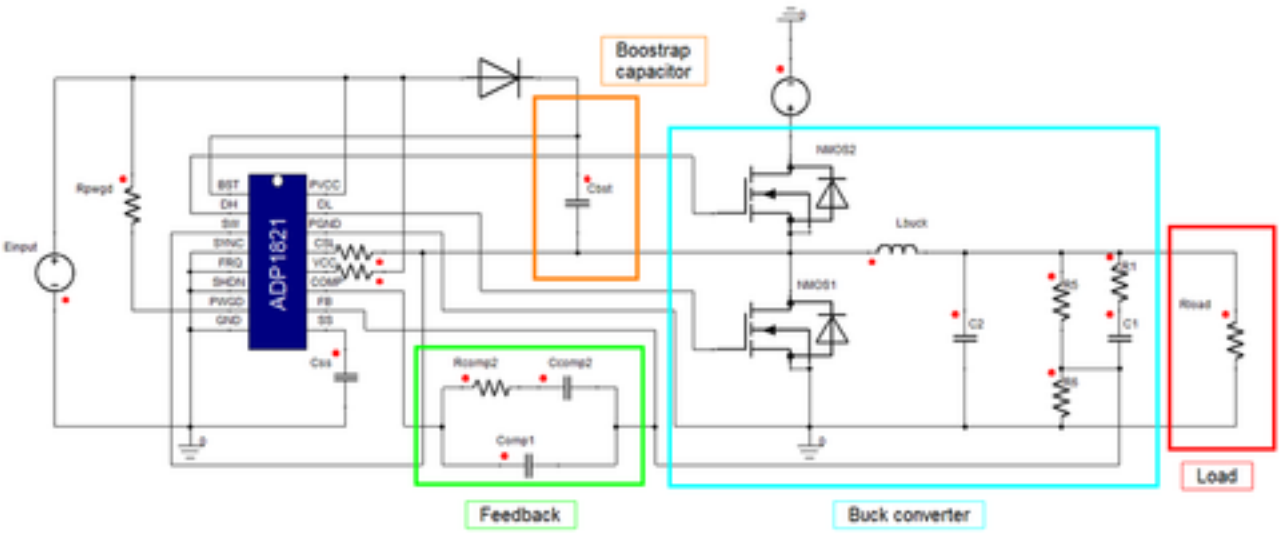

Figure 2. Example Circuit

Simulation results :

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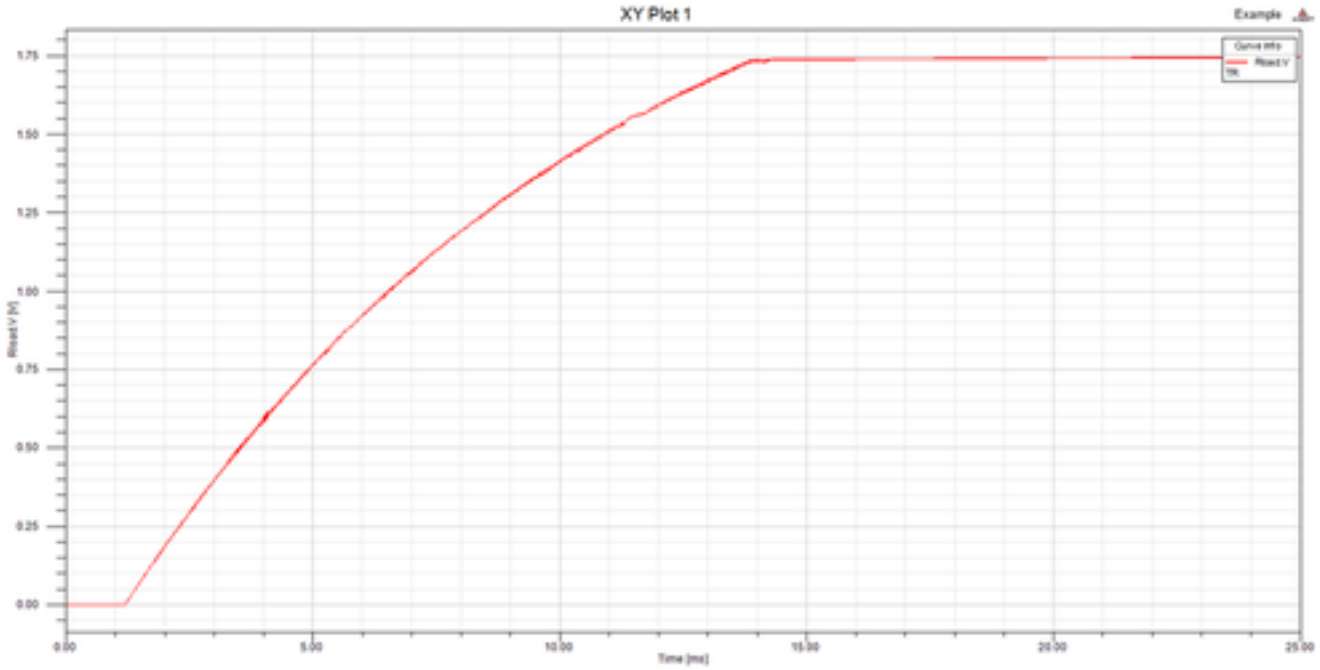

Figure 3. Simulation results

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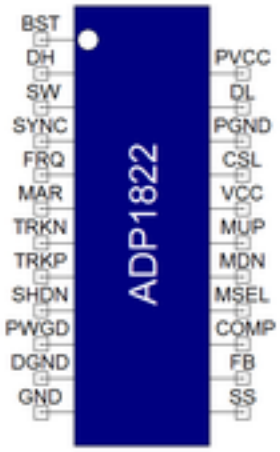
ADP1822: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *ADP1822* regulated output can track another power supply and can be dynamically adjusted up or down with the controller's margining-control inputs, making it ideal for high reliability applications. It is well suited for a wide range of high power applications, such as DSP power and processor core power in telecommunications, medical imaging, high performance servers, and industrial applications. It operates from a 3.7 V to 5.5 V supply with power input voltage ranging from 1.0 V to 24 V.

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The *ADP1822* can operate at any frequency between 300 kHz and 1.2 MHz, either by synchronizing with an external source or an internally generated, logic-controlled clock of 300 kHz or 600 kHz. It includes an adjustable soft start to allow sequencing and quick power-up while preventing input inrush current. Output reverse-current protection at startup prevents excessive output voltage excursions. The adjustable, virtually lossless current-limit scheme reduces external part count and improves efficiency.

The *ADP1822* operates over the -40°C to +125°C junction temperature range and is available in a 24-lead QSOP package.

The model consists in states machines to model the logic of the integrated circuit, aswell as the delays and blankings. Voltmeters are used as inputs and sources as outputs.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	BST	High-Side Gate Driver Boost Capacitor Input. A capacitor between SW and BST powers the high-side gate driver, DH. The capacitor is charged through a diode from PVCC when the low-side MOSFET is on. Connect a 0.1 µF or greater ceramic capacitor from BST to SW and a Schottky diode from PVCC to BST to power the high-side gate driver.
2	DH	High-Side Gate Driver Output. Connect DH to the gate of the external high-side, N-channel MOSFET switch. DH is powered from the capacitor between SW and BST, and its voltage swings between VSW and VBST.
3	SW	Power Switch Node. Connect the source of the high-side, N-channel MOSFET switch and the drain of the low-side, N-channel MOSFET synchronous rectifier to SW. SW powers the output through the output LC filter.
4	SYNC	Frequency Synchronization Input. Drive SYNC with an external 300 kHz to 1.2 MHz signal to synchronize the converter switching frequency to the applied signal. The maximum SYNC frequency is limited to 2 times the nominal internal frequency selected by FREQ. Do not leave SYNC unconnected; when not used, connect SYNC to GND.
5	FREQ	Frequency Select Input. FREQ selects the converter switching frequency. Drive FREQ low to select 300 kHz, or high to select 600 kHz. Do not leave FREQ unconnected.
6	MAR	Margin Control Input. MAR is used with MSEL to control output voltage margining. MAR chooses between high voltage and low voltage margining when MSEL is driven high. If not used, connect MAR to GND.
7	TRKN	Tracking Comparator Negative Input. Drive TRKN from the voltage that the ADP1822 output voltage tracks. TRKN voltage is limited to VCC. See the Output Voltage Tracking section.
8	TRKP	Tracking Comparator Positive Input. Drive TRKP from the output voltage. TRKP voltage is limited to VCC. See the Output Voltage Tracking section.
9	SHDN	Active Low, DC-to-DC Shutdown Input. Drive SHDN high to turn on the converter and low to

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		turn it off. Connect SHDN to VCC for automatic startup.
10	PWGD	Open-Drain, Power-Good Output. PWGD sinks current to GND when the output voltage is above or below the regulation voltage. Connect a pull-up resistor from PWGD to VDD for a logical power-good indicator.
11	DGND	Digital Ground. Connect DGND to GND at a single point as close as possible to the IC.
12	GND	Analog Ground. Connect GND to PGND at a single point as close as possible to the internal circuitry (IC).
13	SS	Soft Start Control Input. A capacitor from SS to GND controls the soft start period. When the output is overloaded, SS is discharged to prevent excessive input current while the output recovers. Connect a 1 nF capacitor to a 1 µF capacitor from SS to GND to set the soft start period. See the Soft Start section.
14	FB	Voltage Feedback Input. Connect to a resistive voltage divider from the output to FB to set the output voltage. See the Setting the Output Voltage section.
15	COMP	Compensation Node. Connect a resistor-capacitor network from COMP to FB to compensate the regulation control system. See the Compensation section.
16	MSEL	Margin Select Input. Drive MSEL high to activate the voltage margining feature. Drive MSEL low to regulate the output voltage to the nominal value. If not used, connect MSEL to GND.
17	MDN	Margin Down Input. Connect a resistor from MDN to the output voltage to set the low margining voltage. See the Setting the Voltage Margin section.
18	MUP	Margin Up Input. Connect a resistor from MUP to GND to set the high margining voltage. See the Setting the Voltage Margin section.
19	VCC	Internal Power Supply Input. VCC powers the internal circuitry. Bypass VCC to GND with a 0.1 µF or greater capacitor connected as close as possible to the IC.
20	CSL	Low-Side Current Sense Input. Connect CSL to SW through a resistor to set the current limit. See the Setting the Current Limit section.
21	PGND	Power Ground. Connect GND to PGND at a single point as close as possible to the IC.
22	DL	Low-Side Gate Driver Output. Connect DL to the gate of the low-side, N-channel MOSFET syn-

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		chronous rectifier. The DL voltage swings between PGND and PVCC.
23	PVCC	Internal Gate Driver Power Supply Input. PVCC powers the low-side gate driver, DL. Bypass PVCC to PGND with a 1 µF or greater capacitor connected as close as possible to the IC.

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
POWER SUPPLY						
Input Voltage		3.7		5.5	5	V
Undervoltage Lockout Threshold	V_{VCC} rising	2.4	2.7	3.0	2.7	V
Undervoltage Lockout Hysteresis			0.1		0.1	V
Quiescent Current			1	2	1	mA
Shutdown Current	SHDN = GND			10	10	uA
Power Stage Supply Voltage		1.0		24	15	V
ERROR AMPLIFIER						
FB Regulation Voltage		594	600	606	600	mV
FB Input Bias Current		-100	1	100	0	nA
Error Amplifier Open-Loop Voltage Gain			70		70	dB
COMP Output Sink Current			600		-	uA
COMP Output Source Current			110		-	uA
PWM CONTROLLER						
PWM Peak Ramp Voltage			1.25		1.25	V
DL Minimum On Time	FREQ-Q=GND (300 kHz)	120	170	220	170	ns
DL Maximum On Time	FREQ-Q=GND (300 kHz)	140	170	200	170	ns

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SOFT START						
SS Pull-Up Resistance	SS = GND		95		100	kohm
SS Pull-Down Resistance	V_{SS} = 0.6 V	1.65	2.5	4.2	2.5	kohm
OSCILLATOR						
Oscillator Frequency	FREQ=GND	250	310	375	310	kHz
	FREQ=VCC	470	570	720	570	kHz
Synchronization Range	FREQ=GND	300		600	-	kHz
	FREQ=VCC	600		1200	-	kHz
SYNC Minimum Pulse Width				80	80	ns
CURRENT SENSE						
CSL Threshold Voltage	Relative to PGND	-30		30		mV
CSL Output Current	V_{CSL} = 0 V	42	50	54	50	uA
Current Sense Blanking Period			160		160	ns

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Table 3

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
GATE DRIVERS						
DH Rise Time	C_{GATE} = 3 nF		16		7	ns
DH Fall Time	C_{GATE} = 3 nF		12		5.5	ns
DL Rise Time	C_{GATE} = 3 nF		19		7	ns
DL Fall Time	C_{GATE} = 3 nF		13		5.5	ns
Driver R_{ON}, Sourcing Current	1 A, 0.7 µs pulse		2		2	Ohm
Driver RON, Sinking Current	1 A, 0.7 µs pulse		1.5		1.5	Ohm
DL Low to DH High Dead Time			33		33	ns
DH Low to DL High Dead Time			42		42	ns
VOLTAGE MARGINING						
High Output Voltage Margin Resistance	MUP to FB, VMAR = VMSEL = 5 V		20		20	Ohm
Low Output Voltage Margin Resistance	MDN to FB, VMAR = 5 V, VMSEL = 0 V		20		20	Ohm
LOGIC THRESHOLDS (SHDN, SYNC, FREQ, MAR, MSEL)						
Input High Voltage	V_{VCC}=3.7 V to 5.5 V	2.0			2	V
Input Low Voltage	V_{VCC}=3.7 V to 5.5 V			0.8	0.8	V
SYNC, FREQ Input Leakage Current	SYNC-C=FREQ=GND		0.1	1	0	uA
SHDN MAR, MSEL Pull-Down Resistance			100		100	kohm
THERMAL SHUTDOWN						

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Thermal Shutdown Threshold			145		X	°C
Thermal Shutdown Hysteresis			10		X	°C
PWGD OUTPUT						
FB Over-voltage Threshold	V_{FB} rising		750		750	mV
FB Over-voltage Hys-teresis			35		35	mV
FB Under-voltage Threshold	V_{FB} rising		550		550	mV
FB Under-voltage Hys-teresis			35		35	mV
PWGD Off Current	V_{PWGD} = 5 V			1	-	uA
PWGD Low Voltage	I_{PWGD} = 10 mA		150	500	-	mV

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Example circuit :

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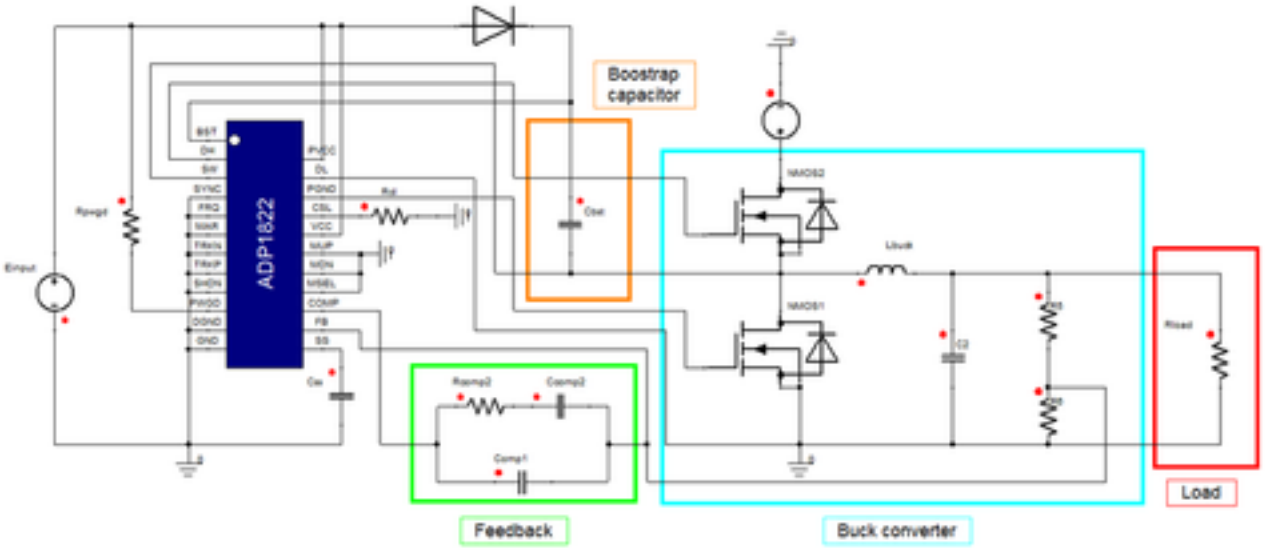

Figure 2. Example Circuit

Simulation results :

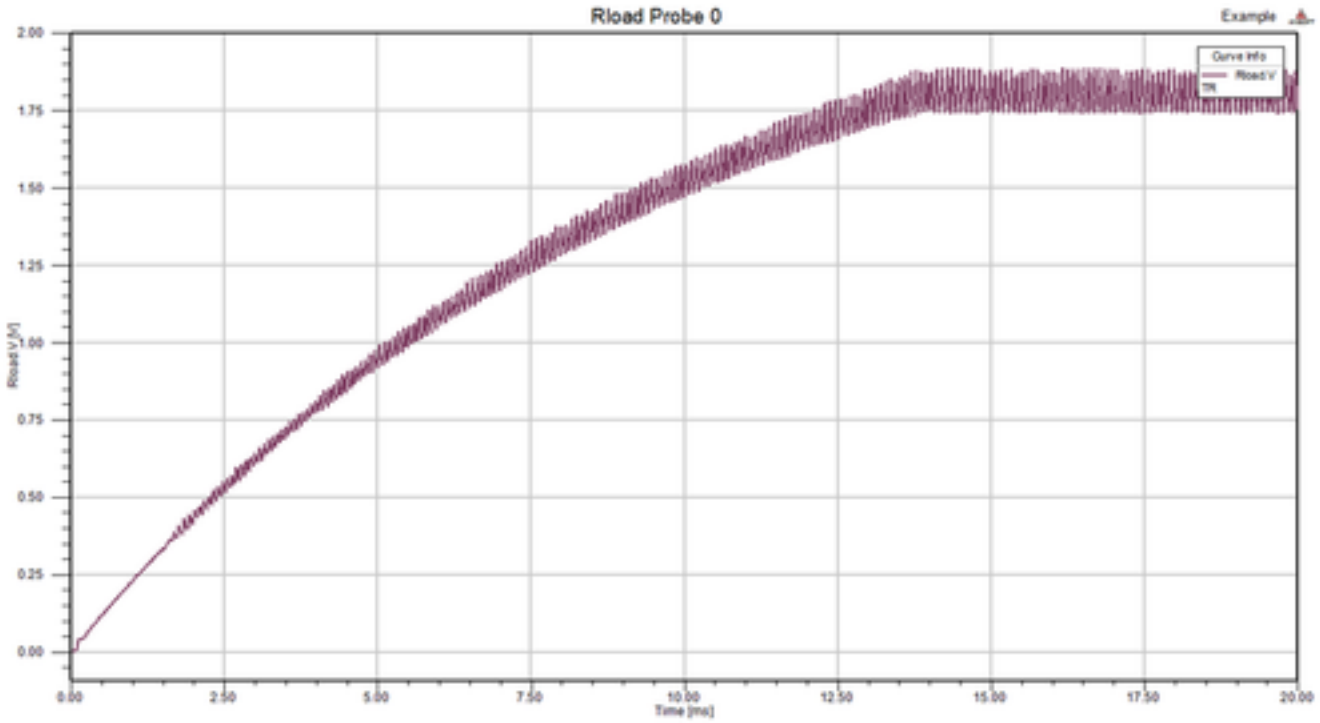

Figure 3. Simulation results

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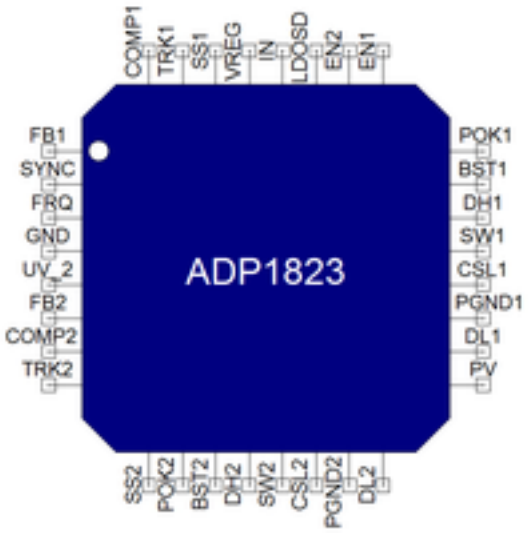
ADP1823: Analog Devices

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *ADP1823* is a versatile, dual, interleaved, synchronous, PWM buck controller that generates two independent output rails from an input of 3.7 V to 20 V, with a power input voltage that ranges from 1 V to 24 V. Each controller can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators. The two channels operate 180° out of phase, reducing stress on the input capacitor and allowing smaller, low cost components. The *ADP1823* is ideal for a wide range of high power applications, such as DSP and processor core I/O power, and general-purpose power in telecommunications, medical imaging, PCs, gaming, and industrial applications.

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The *ADP1823* operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost. For noise sensitive applications, it can also be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1 MHz. The *ADP1823* includes soft start protection to prevent inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme using external MOSFET sensing.

For applications requiring power supply sequencing, the *ADP1823* also provides tracking inputs that allow the output voltages to track during startup, shutdown, and faults. This feature can also be used to implement DDR memory bus termination.

The *ADP1823* is specified over the -40°C to +125°C junction temperature range and is available in a 32-lead LFCSP.

The model consists in states machines to model the logic of the integrated circuit, aswell as the delays and blankings. Voltmeters are used as inputs and sources as outputs.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	FB1	Feedback Voltage Input for Channel 1. Connect a resistor divider from the buck regulator output to GND and tie the tap to FB1 to set the output voltage.
2	SYNC	Frequency Synchronization Input. Accepts external signal between 600 kHz and 1.2 MHz or between 1.2 MHz and 2 MHz depending on whether FREQ is low or high, respectively. Connect SYNC to ground if not used.
3	FREQ	Frequency Select Input. Low for 300 kHz or high for 600 kHz.
4	GND	Ground. Connect to a ground plane directly beneath the ADP1823. Tie the bottom of the feedback dividers to this GND.
5	UV2	Input to the POK2 Undervoltage and Overvoltage Comparators. For the default

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		thresholds, connect UV2 directly to FB2. For some tracking applications, connect UV2 to an extra tap on the FB2 voltage divider string.
6	FB2	Feedback Voltage Input for Channel 2. Connect a resistor divider from the buck regulator output to GND and tie the tap to FB2 to set the output voltage.
7	COMP2	Error Amplifier Output for Channel 2. Connect an RC network from COMP2 to FB2 to compensate Channel 2.
8	TRK2	Tracking Input for Channel 2. To track a primary voltage, drive TRK2 from a voltage divider to the primary voltage. If the tracking function is not used, connect TRK2 to VREG.
9	SS2	Soft Start Control Input. Connect a capacitor from SS2 to GND to set the soft start period.
10	POK2	Open-Drain Power OK Output for Channel 2. Sinks current when UV2 is out of regulation. Connect a pull-up resistor from POK2 to VREG.
11	BST2	Boost Capacitor Input for Channel 2. Powers the high-side gate driver, DH2. Connect a 0.22 µF to 0.47 µF ceramic capacitor from BST2 to SW2 and a Schottky diode from PV to BST2.
12	DH2	High-Side (Switch) Gate Driver Output for Channel 2.
13	SW2	Switch Node Connection for Channel 2.
14	CSL2	Current Sense Comparator Inverting Input for Channel 2. Connect a resistor between CSL2 and SW2 to set the current-limit offset.
15	PGND2	Ground for Channel 2 Gate Driver. Connect to a ground plane directly beneath the ADP1823.
16	DL2	Low-Side (Synchronous Rectifier) Gate Driver Output for Channel 2.
17	PV	Positive Input Voltage for Gate Driver DL1 and Gate Driver DL2. Connect PV to VREG and bypass to ground with a 1 µF capacitor.
18	DL1	Low-Side (Synchronous Rectifier) Gate Driver Output for Channel 1.
19	PGND1	Ground for Channel 1 Gate Driver. Connect to a ground plane directly beneath the ADP1823.
20	CSL1	Current Sense Comparator Inverting Input for Channel 1. Connect a resistor between CSL1 and SW1 to set the current-limit offset.
21	SW1	Switch Node Connection for Channel 1.
22	DH1	High-Side (Switch) Gate Driver Output for Channel 1.
23	BST1	Boost Capacitor Input for Channel 1. Powers the high-side gate driver, DH1. Connect a 0.22 µF to

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		0.47 µF ceramic capacitor from BST1 to SW1 and a Schottky diode from PV to BST1.
24	POK1	Open-Drain Power OK Output for Channel 1. Sinks current when FB1 is out of regulation. Connect a pull-up resistor from POK1 to VREG.
25	EN1	Enable Input for Channel 1. Drive EN1 high to turn on the Channel 1 controller, and drive it low to turn off the Channel 1 controller. Enabling starts the internal LDO. Tie to IN for automatic startup.
26	EN2	Enable Input for Channel 2. Drive EN2 high to turn on the Channel 2 controller, and drive it low to turn off the Channel 2 controller. Enabling starts the internal LDO. Tie to IN for automatic startup.
27	LDOSD	LDO Shut-Down Input. Only used to shut down the LDO in those applications where IN is tied directly to VREG. Otherwise, connect LDOSD to GND or leave it open because it has an internal 100 kΩ pull-down resistor.
28	IN	Input Supply to the Internal Linear Regulator. Drive IN with 5.5 V to 20 V to power the ADP1823 from the LDO. For input voltages between 3.7 V and 5.5 V, tie IN to VREG and PV.
29	VREG	Output of the Internal Linear Regulator (LDO). The internal circuitry and gate drivers are powered from VREG. Bypass VREG to the ground plane with a 1 µF ceramic capacitor.
30	SS1	Soft Start Control Input. Connect a capacitor from SS1 to GND to set the soft start period.
31	TRK1	Tracking Input for Channel 1. To track a primary voltage, drive TRK1 from a voltage divider to the primary voltage. If the tracking function is not used, connect TRK1 to VREG.
32	COMP1	Error Amplifier Output for Channel 1. Connect an RC network from COMP1 to FB1 to compensate Channel 1.

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS

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POWER SUPPLY						
Input Voltage	PV = VREG using internal regulator	5.5		20	5	V
	IN = PV = VREG not using internal regulator	3.7		5.5	5	V
Undervoltage Lockout Threshold	V_{VCC} rising	2.4	2.7	3.0	2.7	V
Undervoltage Lockout Hysteresis			0.1		0.1	V
IN Quiescent Current			1	2	1	mA
IN Shutdown Current	EN1 = EN2 = GND			10	10	uA
ERROR AMPLIFIER						
FB1, FB2 Regulation Voltage		597	600	603	600	mV
FB1, FB2 Input Bias Current				100	0	nA
Open-Loop Voltage Gain			70		70	dB
Gain-Bandwidth Product			20		-	Mhz
COMP1, COMP2 Output Sink Current			600		-	uA
COMP1, COMP2 Output Source Current			120		-	uA
COMP Clamp High Voltage			2.4		2.4	V
COMP Clamp Low Voltage			0.75		0.75	V
LINEAR REGULATOR						

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VREG Output Voltage		4.85	5.0	5.15	5	V
VREG Load Regulation	IVREG = 0 mA to 100 mA, IN = 12 V		−40			mV
VREG Line Regulation	IN = 7 V to 20 V, IVREG = 20 mA		1			mV
VREG Current Limit	VREG = 4 V		220			mA
VREG Short-Circuit Current	VREG < 0.5 V	50	140	200		mA
IN to VREG Dropout Voltage	IVREG = 100 mA, IN < 5 V		0.7	1.4	-	V
VREG Minimum Output Capacitance		1				uF
PWM CONTROLLER						
PWM Peak Ramp Voltage			1.25		1.25	V
DH Maximum Duty Cycle	FREQ-Q=GND (300 kHz)	85	90		95	%
DH Minimum Duty Cycle	FREQ-Q=GND (300 kHz)		1	3	0	%

Table 3

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
SOFT START						
SS Pull-Up Resistance	SS = GND		95		100	kohm
SS Pull-Down Resistance	V_{SS} = 0.6 V	1.65	2.5	4.2	2.5	kohm
SS1, SS2 to FB1, FB2 Off-	SS1, SS2 = 0 mV to 500		−45		0	mV

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set Voltage	mV					
SS1, SS2 Pull-Up Voltage			0.8		0.8	0.8
TRACKING						
TRK1, TRK2 Common-Mode Input Voltage Range	TRK1, TRK2 = 0 mV to 500 mV	0		600	0/600	mV
TRK1, TRK2 to FB1, FB2 Offset Voltage		-5		5	0	mV
TRK1, TRK2 Input Bias Current				100	0	nA
OSCILLATOR						
Oscillator Frequency	FREQ-Q=GND	250	310	375	310	kHz
	FREQ-Q=VCC	470	570	720	570	kHz
Synchronization Range	FREQ-Q=GND	300		600	-	kHz
	FREQ-Q=VCC	600		1200	-	kHz
SYNC Minimum Pulse Width				80	80	ns
CURRENT SENSE						
CSL Threshold Voltage	Relative to PGND	-30		30		mV
CSL Output Current	V_{CSL} = 0 V	42	50	54	50	uA
Current Sense Blanking Period			100		100	ns
GATE DRIVERS						
DH Rise Time	C_{GATE} = 3 nF		15		7	ns
DH Fall Time	C_{GATE} = 3 nF		10		5.5	ns
DL Rise Time	C_{GATE} = 3 nF		15		7	ns
DL Fall Time	C_{GATE} = 3 nF		10		5.5	ns

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DH to DL, DL to DH Dead Time			40		40	ns
THERMAL SHUTDOWN						
Thermal Shut-down Threshold			145		X	°C
Thermal Shut-down Hys-teresis			10		X	°C

Table 4

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
LOGIC THRESHOLDS (SHDN, SYNC, FREQ)						
SYNC, FREQ, LDOSD Input High Voltage		2.2			2.2	V
SYNC, FREQ, LDOSD Input Low Voltage				0.4	0.4	V
SYNC, FREQ Input Leakage Cur-rent	SYNC, FREQ = 0 V to 5.5 V			1	0	uA
LDOSD Pull-Down Resist-ance			100		100	kOhm
EN1, EN2 Input High Voltage	IN = 3.7 V to 20 V	2			2	V
EN1, EN2 Input Low Voltage	IN = 3.7 V to 20 V			0.8	0.8	V
EN1, EN2 Current Source	EN1, EN2 = 0 V to 3.0 V	-0.05	-0.6	-1.5	0.6	uA
EN1, EN2 Input Imped-ance to 5 V Zener	EN1, EN2 = 5.5 V to 20 V		100		100	kOhm
POWER GOOD						

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FB1, UV2 Overvoltage Threshold	VFB1, VUV2 rising		750		750	mV
FB1, UV2 Overvoltage Hysteresis			50		50	mV
FB1, UV2 Undervoltage Threshold	VFB1, VUV2 rising		550		550	mV
FB1, UV2 Undervoltage Hysteresis			50		50	mV
POK1, POK2 Propagation Delay			8		0	us
POK1, POK2 Off Leakage Current	VPOK1, VPOK2 = 5.5 V			1	0	uA
POK1, POK2 Output Low Voltage	IPOK1, IPOK2 = 10 mA		150	500	150	mV
UV2 Input Bias Current			10	100	0	nA

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Examples

Example circuit :

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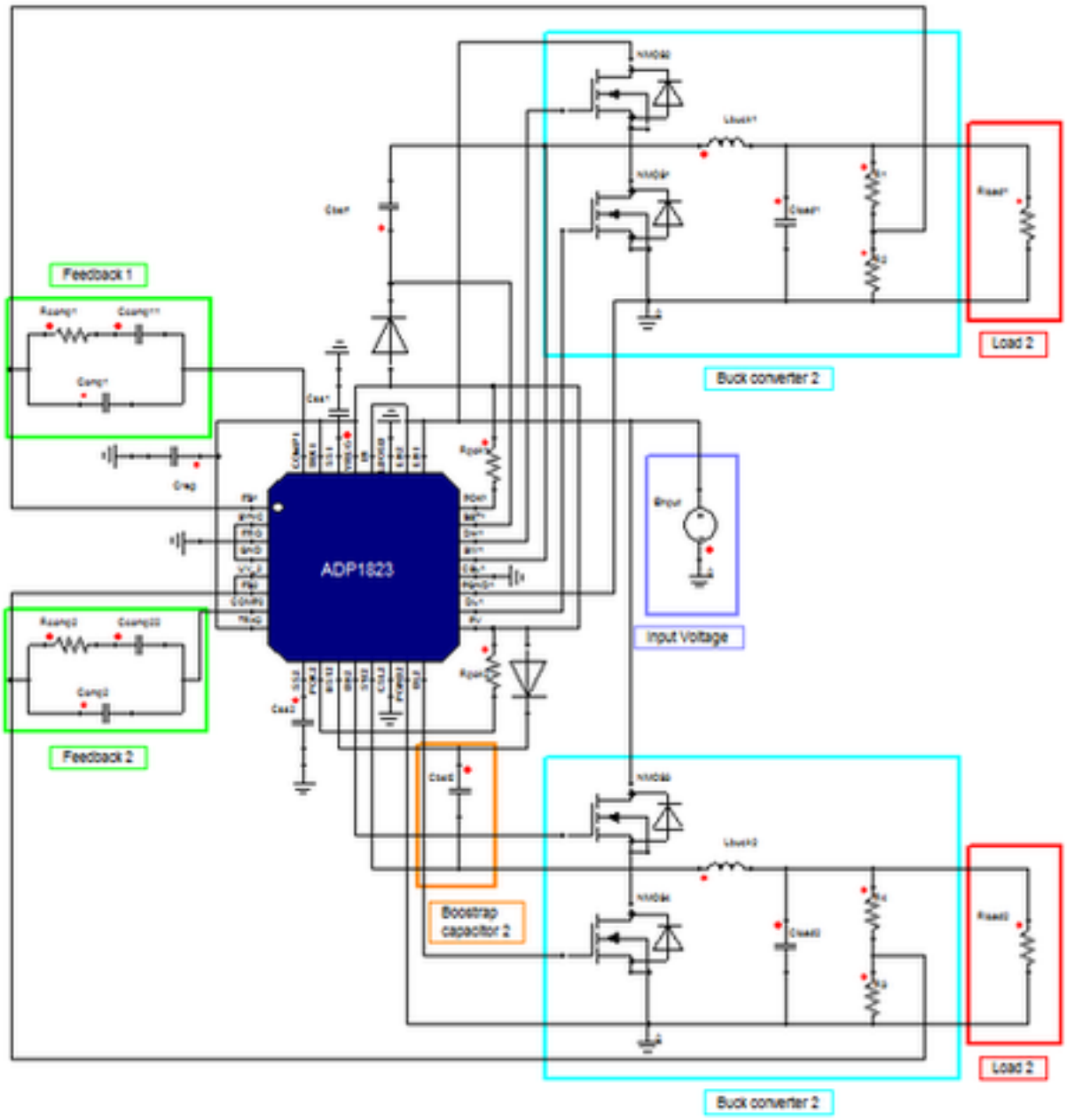

Figure 2. Example Circuit

Simulation results :

Output 1 :

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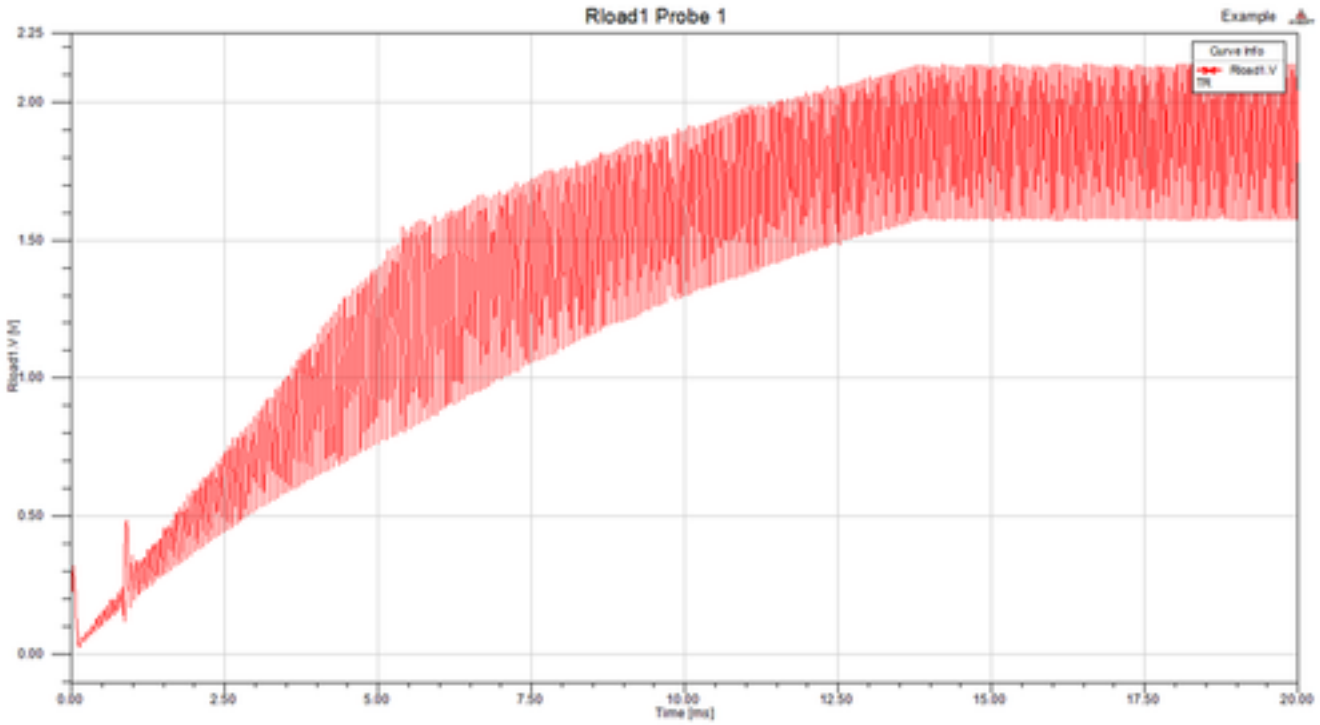

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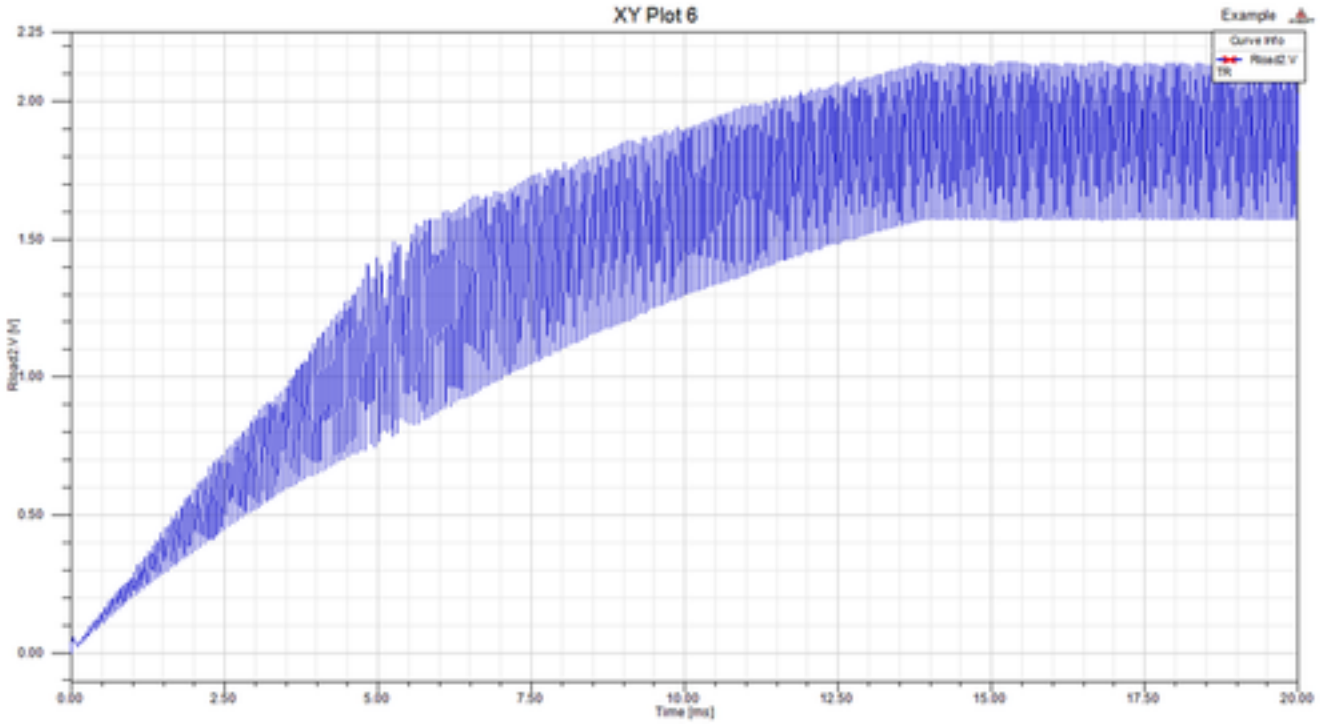

Figure 3. Simulation results

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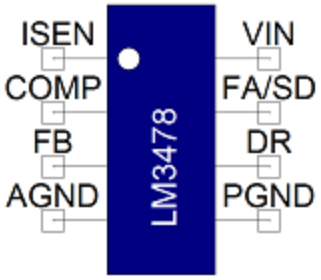
LM3478: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM3478* is a versatile Low-Side N-Channel MOSFET controller for switching regulators. It is suitable for use in topologies requiring a low side MOSFET, such as boost, flyback, SEPIC, etc. Moreover, the LM3478 can be operated at extremely high switching frequency in order to reduce the overall solution size. The switching frequency of the *LM3478* can be adjusted to any value between 100kHz and 1MHz by using a single external resistor. Current mode control provides superior bandwidth and transient response, besides cycle-by-cycle current limiting. Output current can be programmed with a single external resistor.

The *LM3478* has built in features such as thermal shutdown, short-circuit protection, over voltage protection, etc. Power saving shutdown mode reduces the total supply current to 5µA and allows power supply sequencing. Internal soft-start limits the inrush current at start-up.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	ISEN	Ground
2	COMP	VoltageamplifierInverting Input
3	FB	Compensation
4	AGND	SoftStart
5	PGND	Standby
6	DR	Bootstrap
7	FA/SD	High Side Driver Output
8	VIN	Power Ground

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Parameters

Comparison between model and real component.

Table 2

PARAMET-ER	TEST CONDITIO-NS	MIN	TYP	MAX	MODE-L	UNIT-S
Feedback Voltage	Vcomp = 1.4 V 2.97 < Vin < 40V	1.22-8	1.26	1.29-2	1.26	V
Feedback Voltage line Regulation	2.97 < Vin < 40V		0.00-1		-	%/V
Output Voltage	Ieao Source/		+/- 0.5		-	%/A

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Load Regulation	Sink					
Input Under-Voltage Lock-out			2.85	2.97	2.85	V
Input Under-Voltage Lock-out Hysteresis		130	170	210	170	mV
Nominal Switching Frequency	Rfa = 40 kOhm	350	400	440	400	kHz
Driver Switch On Resistance (top)	Idr = 0.2 A, Vin =5V		16		16	Ohm
Driver Switch On Resistance (bottom)	Idr = 0.2 A		4.5		4.5	Ohm
Maximum Driver Voltage Swing	Vin < 7.2V		Vin		Vin	V
	Vin > 7.2V		7.2		7.2	V
Maximum Duty Cycle			100		100	%
Minimum On Time		210	325	600	325	ns
Supply Current Non Switching			2.7	3.3	2.7	mA
Quiescent Current in Shutdown Mode	Vfa/sd = 5V Vin = 5V		5	10	-	uA
Current Sense Threshold Voltage	Vin = 5V	125	156	190	156	mV
Short-Circuit Current Limit Sense Voltage	Vin = 5V	250	343	415	343	mV
Internal Compensation Ramp Voltage	Vin = 5V	52	92	132	92	mV

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Output Over-Voltage Protection	Vcomp = 1.4 V	25	50	100	50	mV
Output Over-Voltage Protection Hysteresis	Vcomp = 1.4 V	20	60	110	60	mV

Table 3

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Error Amplifier Transconductance	Vcomp = 1.4 V Ieao = 100uA (Source/Sink)	600	800	1000	800	uS
Error Amplifier Voltage Gain	Vcomp = 1.4 V Ieao = 100uA (Source/Sink	26	28	44	32	V/V
Error Amplifier Output Current (Source/Sink)	Vcomp = 1.4 V Vfb = 0V	50	110	180	110	uA
	Vcomp = 1.4 V Vfb = 1.4V	-85	-140	-185	-140	uA
Error Amplifier Output Voltage Swing	Upper limit Vfb = 0V	1.8	2.2	2.4	2.2	V
	Lower limit Vfb = 1.4V	0.2	0.56	1	0.56	V
Internal Soft-Start Delay	Vfb = 1.2V Vcomp Floating		4		4	ms
Drive pin Rise Time	Cgs = 3000pF, Vdr = 0 to		25		25	ns

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	3V					
Drive pin Fall Time	Cgs = 3000pF, Vdr = 0 to 3V		25		25	ns
Shutdown Threshold	High		1.27	1.4	1.27	V
	Low		0.65	0.3	0.65	V
Shutdown Pin Current	Vsd = 5V		-1		-1	uA
	Vsd = 0V		1		1	uA
Feedback Pin Current			15		0	nA
Thermal Shut-down			165		-	°C
Thermal Shut-down Hys-teresis			10		-	°C
Thermal Resist-ance			200		-	°C/W

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Example circuit :

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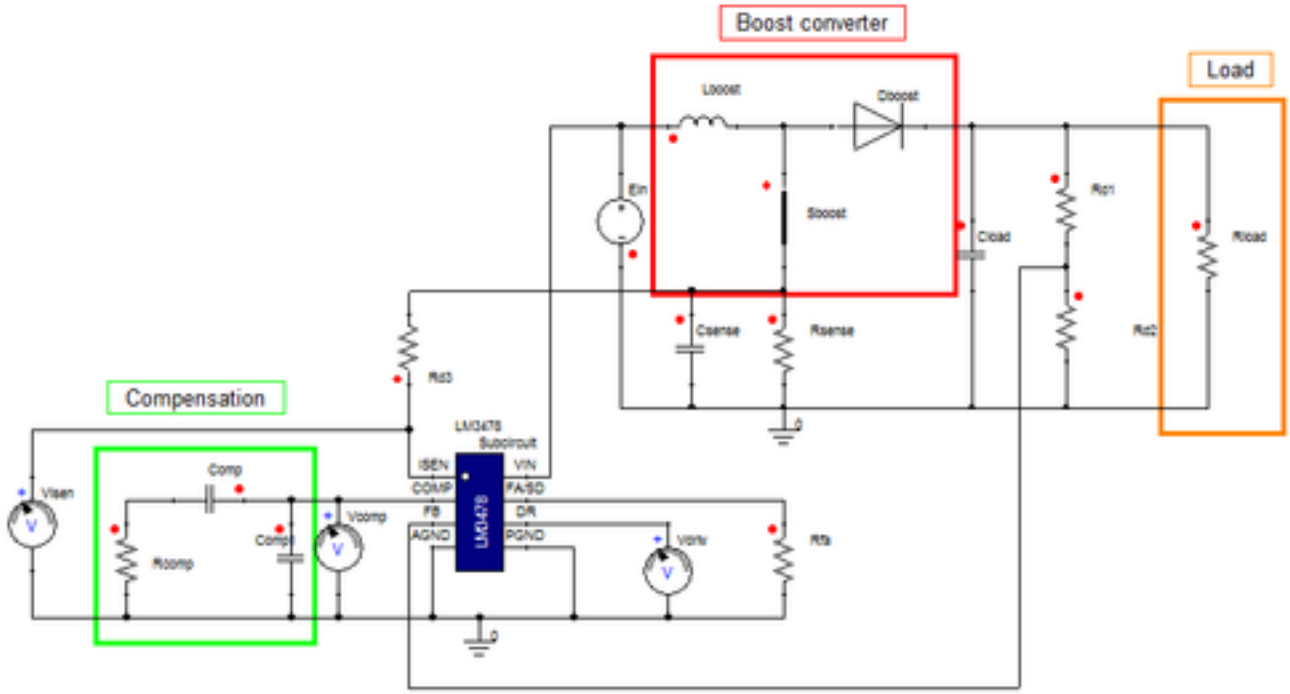

Figure 2. Example Circuit

Simulation results :

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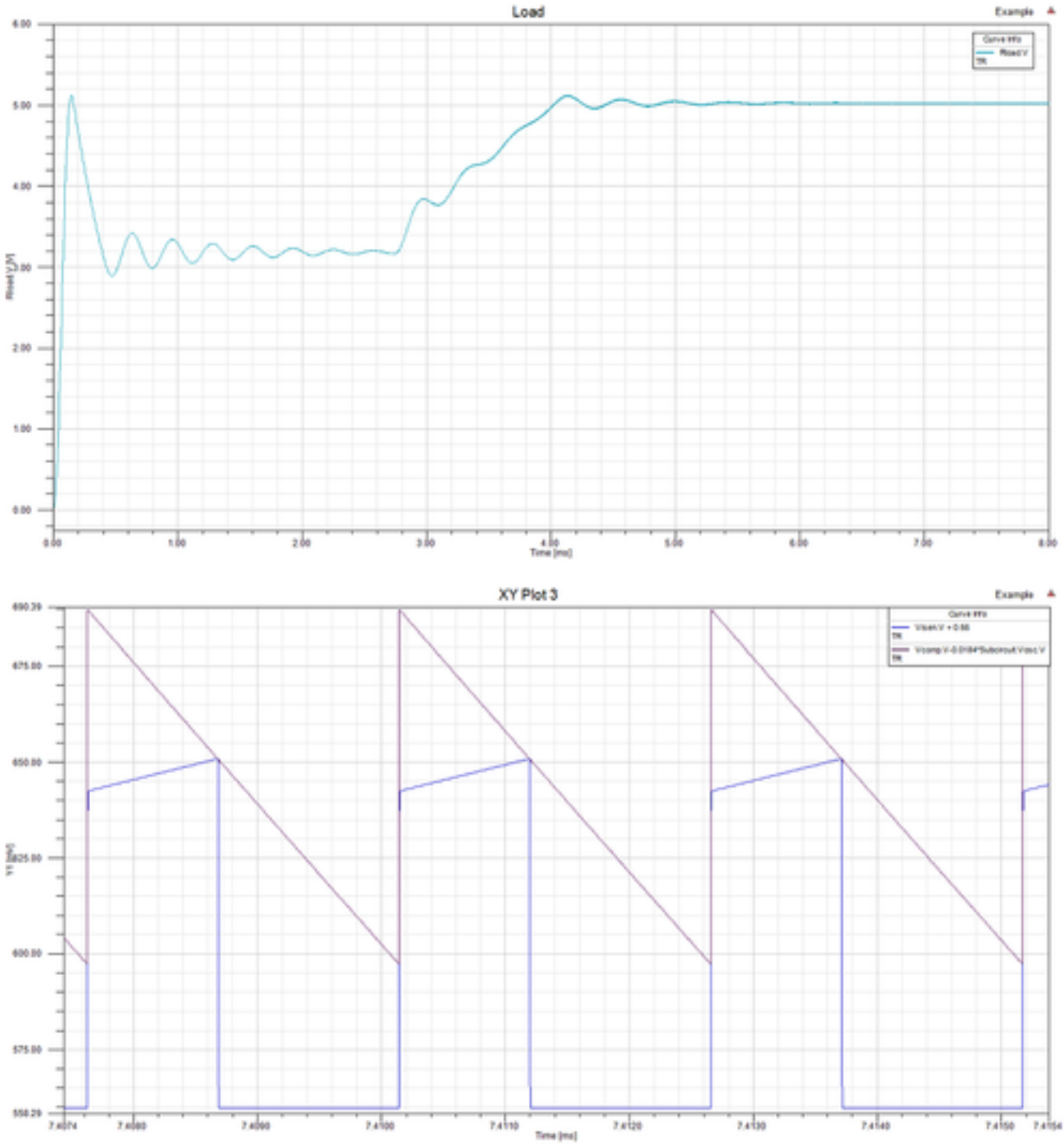

Figure 3. Simulation results

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References

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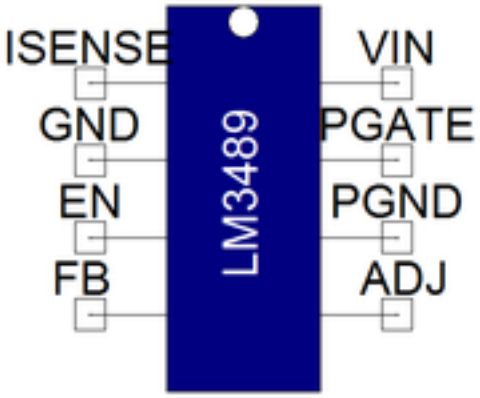
LM3489: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LM3489* is a versatile, dual, interleaved, synchronous, PWM buck controller that generates two independent output rails from an input of 3.7 V to 20 V, with a power input voltage that ranges from 1 V to 24 V. Each controller can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators. The two channels operate 180° out of phase, reducing stress on the input capacitor and allowing smaller, low cost components. The *LM3489* is ideal for a wide range of high power applications, such as DSP and processor core I/O power, and general-purpose power in telecommunications, medical imaging, PCs, gaming, and industrial applications.

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The *LM3489* operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost. For noise sensitive applications, it can also be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1 MHz. The *LM3489* includes soft start protection to prevent inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme using external MOSFET sensing.

For applications requiring power supply sequencing, the *LM3489* also provides tracking inputs that allow the output voltages to track during startup, shutdown, and faults. This feature can also be used to implement DDR memory bus termination.

The *LM3489* is specified over the -40°C to +125°C junction temperature range and is available in a 32-lead LFCSP.

This model is made up of two main parts: the electric circuit and the state machines that command it.

The electric circuit measures the following parameters:
-Input voltage
-Current sense voltage
-Current limit adjust voltage
-Enable pin voltage

As a function of these values, the main state machine sets the output gate voltage to a high or low value. The two auxiliary state machines control the enable and the current limit functions.

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Conservative Pins

Table 1

Pin #	Symbol	Description
1	ISENSE	The current sense input pin. This pin should be connected to the PFET drain terminal directly or through a series resistor up to 600 ohm for 28V>Vin>35V.
2	GND	Signal ground.
3	EN	Enable pin. Connect EN pin to ground to shutdown the part or float to enable operation

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		(Internally pulled high). This pin can also be used to perform UVLO function.
4	FB	The feedback input. Connect the FB to a resistor voltage divider between the output and GND for an adjustable output voltage.
5	ADJ	Current limit threshold adjustment. Connected to an internal 5.5µA current source. A resistor is connected between this pin and VIN. The voltage across this resistor is compared with the ISENSE pin voltage to determine if an over-current condition has occurred.
6	PGND	Power ground.
7	PGATE	Gate Drive output for the external PFET. PGATE swings between VIN and VIN-5V.
8	VIN	Power supply input pin.

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Comparison between model and real component.

Specifications in Standard type face are for TJ = 25°C, and in **bold type** face apply over the full **Operating Temperature Range** (TJ = -40°C to +125°C). Unless otherwise specified, VIN = 12V, VISNS = VIN - 1V, and VADJ = VIN - 1.1V. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Table 2

Symbol	**Parameter**	**Real component test conditions**	**LM3489**			**Model**	**Units**
			Min	**Typ**	**Max**		
I_{SHDN}	Shutdown input supply current	EN = 0V		7	**15**	7	µA
V_{EN}	Enable threshold voltage	Enable rising	**1.15**	1.5	**1.85**	1.5	V
V_{EN_HYST}	Enable threshold hysteresis		-	130	-	130	mV

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I_Q	Quiescent Current at ground pin	FB = 1.5V (Not Switching)	-	280	**400**	280	µA
V_{FB}	Feedback Voltage		1.22-3 **1.21-4**	1.23-9	1.25-5 **1.26-4**	1.239	V
V_{HYST}	Comparator Hysteresis		-	10 **14**	15 **20**	10	mV
V_{CL_OFFSET}	Current limitcomparator offset	V_{FB} = 1.0V	**-20**	0	**+20**	0	mV
I_{CL_ADJ}	Current limit ADJ current source	V_{FB} = 1.5V	**3.0**	5.5	**7.0**	5.5	µA
T_{CL}	Current limit one shot off time	V_{ADJ} = 11.5V V_{ISNS} = 11.0V V_{FB} = 1.0V	**6**	9	**14**	9	µs
R_{PGATE}	Driver resistance	Source I_{SOURCE} = 100mA	-	5.5	-	5.5	Ω
		Sink I_{SINK} = 100mA	-	8.5	-	8.5	
I_{PGATE}	Driver Output current	Source V_{IN} = 7V, PGATE = 3.5V	-	0.44	-	0.63	A
		Sink VIN = 7V, PGATE = 3.5V	-	0.1	-	0.17	
I_{FB}	FB pin BiasCur-	V_{FB} = 1.0V	-	300	**750**	0	nA

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	rent						
T_{ONMIN_NOR}	Minimum on time in normal operation	V_{ISNS} = V_{ADJ} + 0.1V Cload on OUT = 1000pF	-	100	-	100	ns
T_{ONMIN_CL}	Minimum on time in current limit	V_{ISNS} = V_{ADJ} - 0.1V VFB = 1.0V Cload on OUT = 1000pF	-	200	-	100	ns
$\%V_{FB}/\Delta V_{IN}$	Feed-back Voltage Line Regu-lation	$4.5 \leq V_{IN} \leq 35V$	-	0.01	-	0	%/V

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Example circuit :

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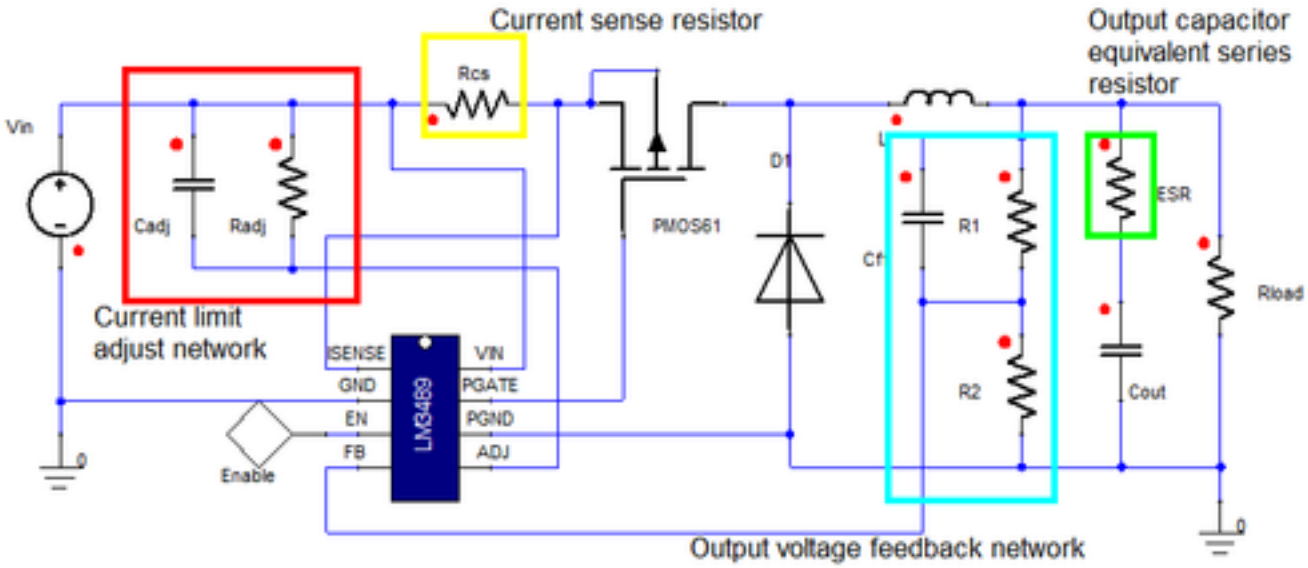

Figure 2. Example Circuit

In this example of connection, the *LM3489* is used to control a buck converter with a P-channel MOSFET. It is also needed auxiliary circuitry such as the current limit adjust network, the current sense resistor and the output voltage divider used in the feedback loop. An output capacitor equivalent series resistor has been added, since the operation frequency strongly depends on its value.

Simulation results :

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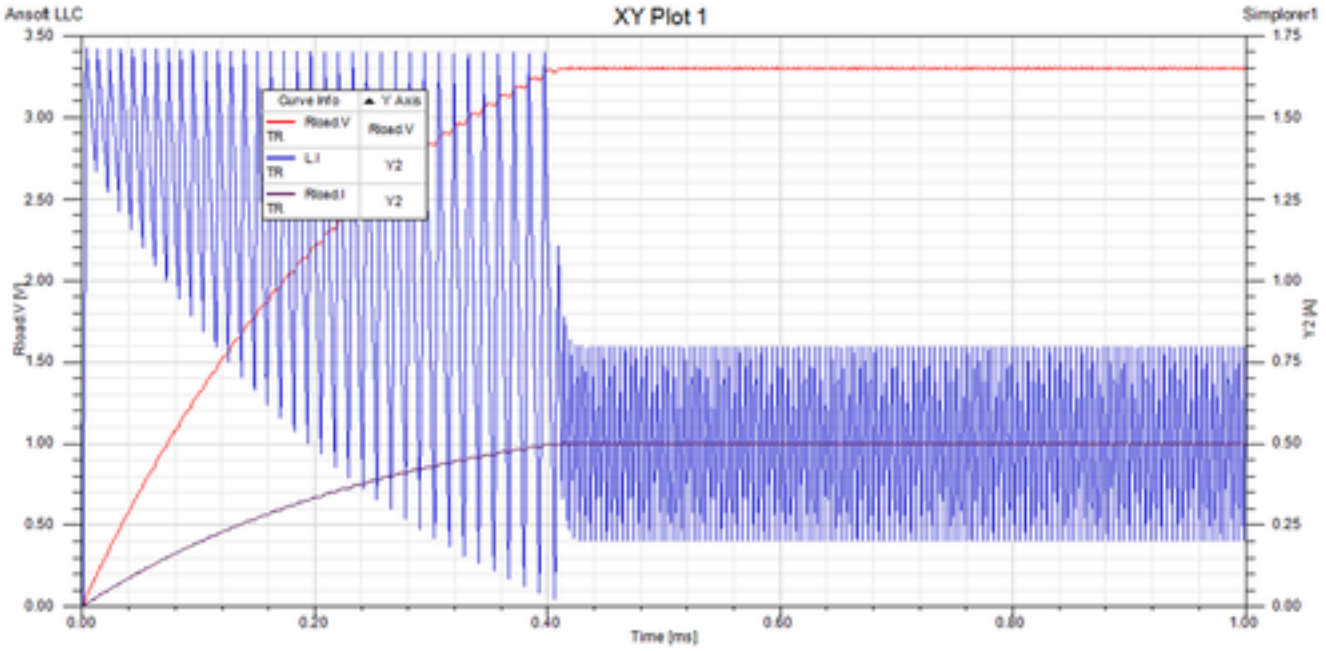

Figure 3. Simulation results(a)

In the above diagram we can see the transition between the start-up period and the normal operation, around 400us. Output voltage (red waveform) rises up to its regulated value, 3.3V. In the same way, output current (purple) reaches the 0.5A regulated value at the same time. The inductor current (blue) oscillation frequency is lower during start-up than during normal operation, as we can see in the following figure:

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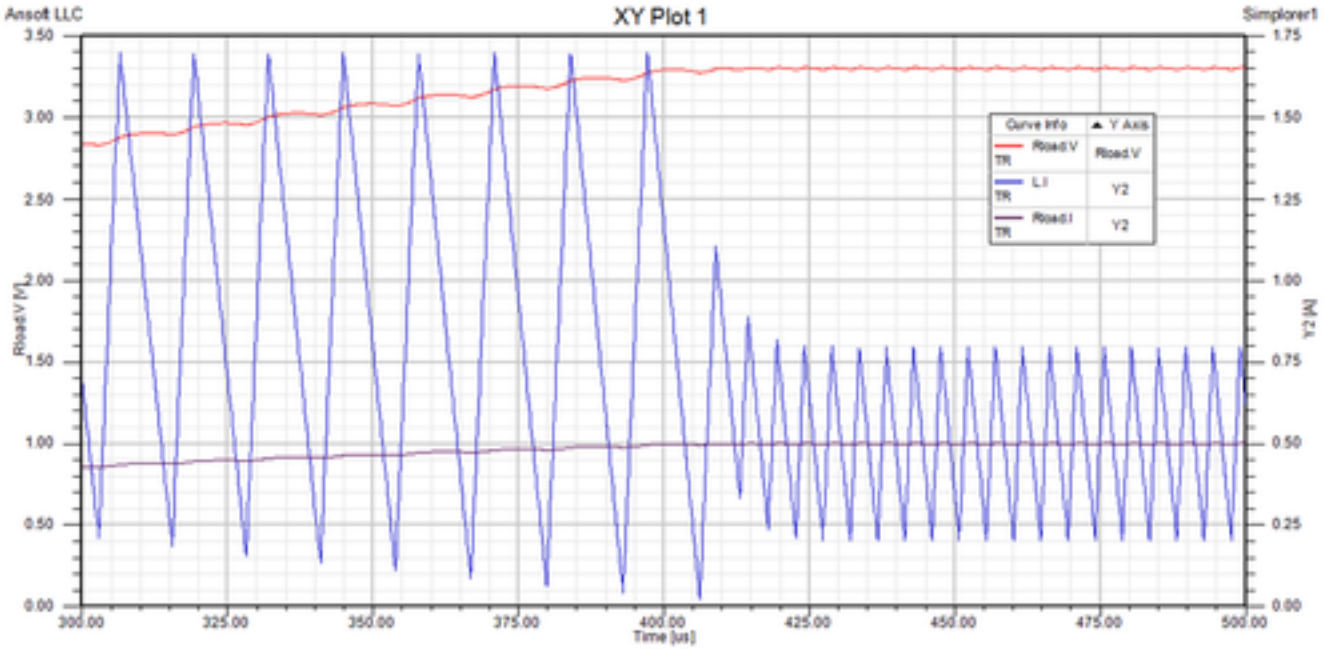

Figure 4. Simulation results(b)

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References

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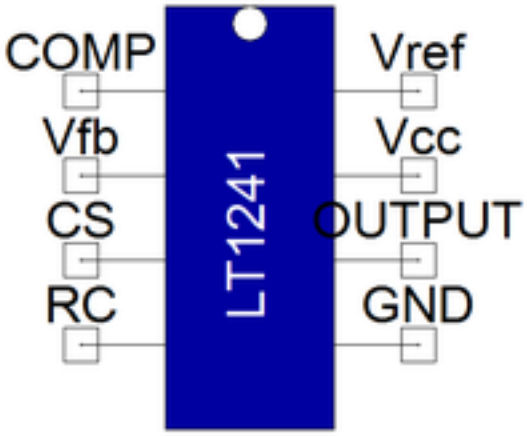
LT1241: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *LT124x* series devices are fixed frequency, current mode, pulse width modulators. These devices have both improved speed and lower quiescent current. The *LT124x* series is optimized for off-line and DC/DC converter applications. They contain a high gain error amplifier, current sensing comparator and a high current totem pole output stage ideally suited to driving power MOSFETs. Leading edge blanking has been added to the current sense comparator. The output stage is clamped to a maximum VOUT of 18V in the on state. The output and the reference output are actively pulled low during under-voltage lockout.

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This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:

• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is 100kΩ. A switch disconnects the voltmeter from the input during the first 100ns of a cycle providing leading edge blanking.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: voltage limited by a zener diode to 18V.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 7.6V, the protection activates and the output and the reference fall to zero), the oscillator, the output voltage and the leading edge blanking.

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Conservative Pins

Table 1

Symbol	Description
COMP	Output of the error amplifier
Vfb	Inverting input of the error amplifier
CS	Input to the current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vcc	Power input
OUTPUT	Output of the driver
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

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Table 2

PARAMETER	CONDITIONS	•	REAL Component			MODEL	UNITS
			MIN	TYP	MAX		
Reference section							
Output Voltage	IO = 1mA, TJ = 25 C		4.925	5.000	5.075	5.000	V
Line Regulation	12V < VCC < 25V	•		3	20	0	mV
Load Regulation	1mA < IVREF < 20mA	•		-6	-25	0	mV
Temperature Stability				0.1		0	mV/C
Total Output Variation	Line, Load, Temp	•	4.87		5.13	0	V
Output Noise Voltage	10Hz < F < 10kHz, TJ =25 C		50			0	V
Long Term Stability	TA = 125° C, 1000 Hrs.			5	25	0	mV
Output Short-Circuit Current		•	-30	-90	-180	X	mA
Oscillator section							
Initial Accuracy	RT = 10k, CT = 3.3nF, TJ = 25 C		47.5	50	52.5	50	kHz
	RT = 13.0k, CT = 500pF, TJ = 25 C		228	248	268	250	kHz
Voltage Stability	12V < VCC < 25V, TJ = 25 C				1	0	%
Temperature Stability	TMIN < TJ < TMAX			-0.05		0	%/C
Amplitude	TJ = 25 C (Pin 4)			1.7		1.7	V
Clock Ramp Reset Current	VOSC (Pin 4) = 2V, TJ = 25 C		7.9	8.2	8.5	X	mA
Error amplifier section							
Feedback Pin Input Voltage	VPIN1 = 2.5V	•	2.42	2.50	2.58	2.50	V
Input Bias Current	VFB = 2.5V	•			-2	0	µA
Open-Loop Voltage Gain	2 < VO < 4V	•	65	90		X	dB
Unity-Gain Bandwidth	TJ = 25 C		0.7	1.3	2	X	MHz
Power Supply Rejection Ratio	12V < VCC < 25V	•	60			60	dB
Output Sink Current	VPIN2 = 2.7V, VPIN1 = 1.1V	•	2	6		0	mA
Output Source Current	VPIN2 = 2.3V, VPIN1 = 5V	•	-0.5	-0.75		0	mA
Output Voltage High Level	VPIN2 = 2.3V, RL = 15k to GND	•	5	5.6		5.6	V
Output Voltage Low Level	VPIN2 = 2.7V, RL = 15k to Pin 8	•	0.2	1.1		0.2	V

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Current sense section							
Gain		●	2.85	3.00	3.15	3.00	V/V
Maximum Current Sense Input Threshold	VPIN3 < 1.1V	●	0.90	1.00	1.10	1.00	V
Power Supply Rejection Ratio		●		70		X	dB
Input Bias Current		●		-1	10	0	µA
Delay to Output		●		50	100	0	ns
Blanking Time				100		100	ns
Blanking Override Voltage				1.5		X	V
Output section							
Output Low Level	IOUT = 20mA	●		0.25	0.4	0.3	V
	IOUT = 200mA	●		0.75	2.2	0.3	V
Output High Level	IOUT = 20mA	●	12.0			Vcc	V
	IOUT = 200mA	●		11.75		Vcc	V
Rise Time	CL = 1nF, TJ = 25 C			50	80	X	ns
Fall Time	CL = 1.0nF, TJ = 25 C			30	60	X	ns
Output Clamp Voltage	IO = 1mA	●		18	19.5	18	V
Under-voltage Lockout							
Start-Up Threshold		●	9.0	9.6	10.2	9.6	V
Minimum Operating Voltage		●	7.0	7.6	8.2	7.6	V
Hysteresis			1.6	2.0		2.0	V
PWM							
Maximum Duty Cycle	TJ = 25 C		46	48		50	%
Minimum Duty Cycle		●	0			0	%
Total device							
Start-Up Current		●		170	250	X	µA
Operating Current		●		7	10	X	mA

The ● denotes those specifications which apply over the full operating temperature range.

X: not implemented

Note 1: Unless otherwise specified, VCC = 15V, RT = 10k, CT = 3.3nF.
Note 2: Low duty cycle pulse techniques are used during test to maintain junction temperature close to ambient.

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Examples

Example circuit :

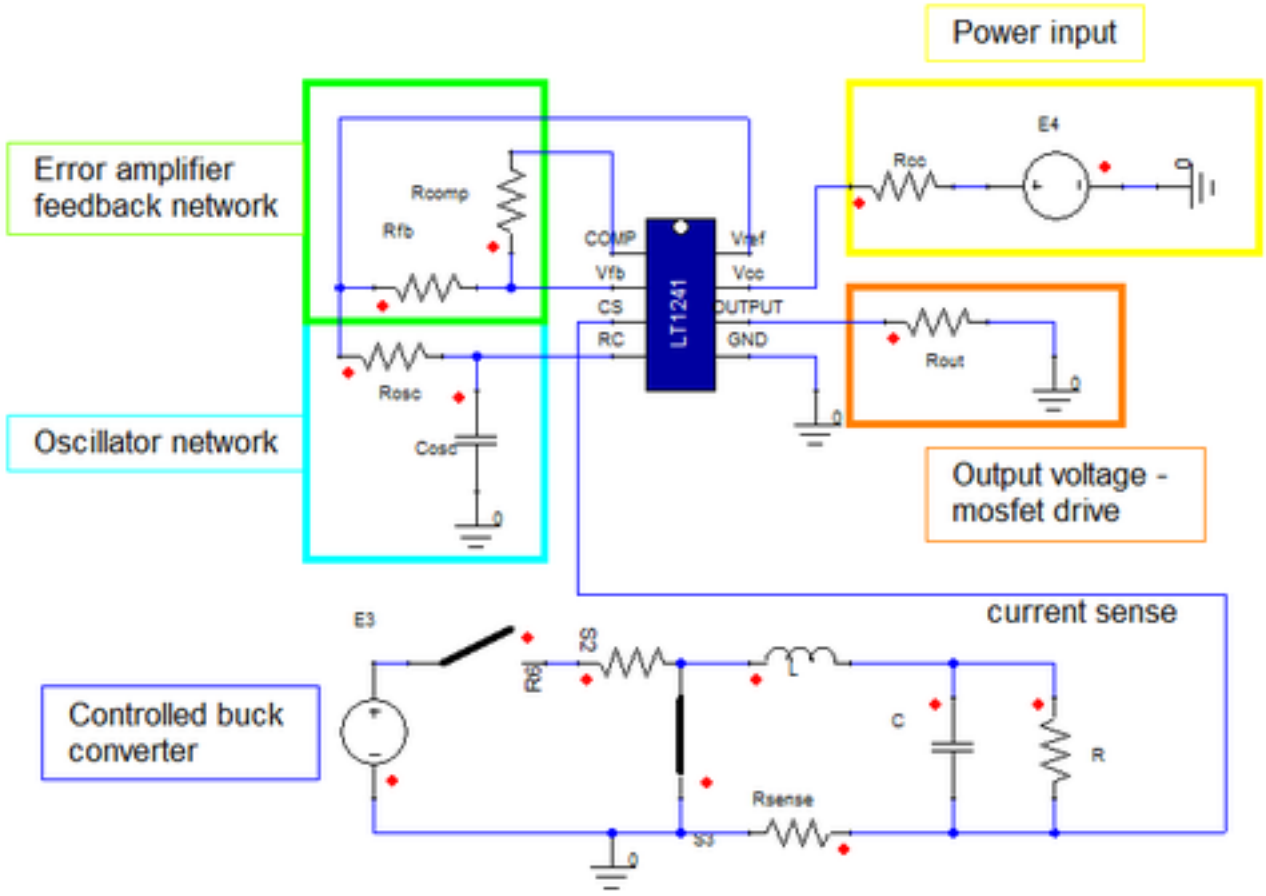

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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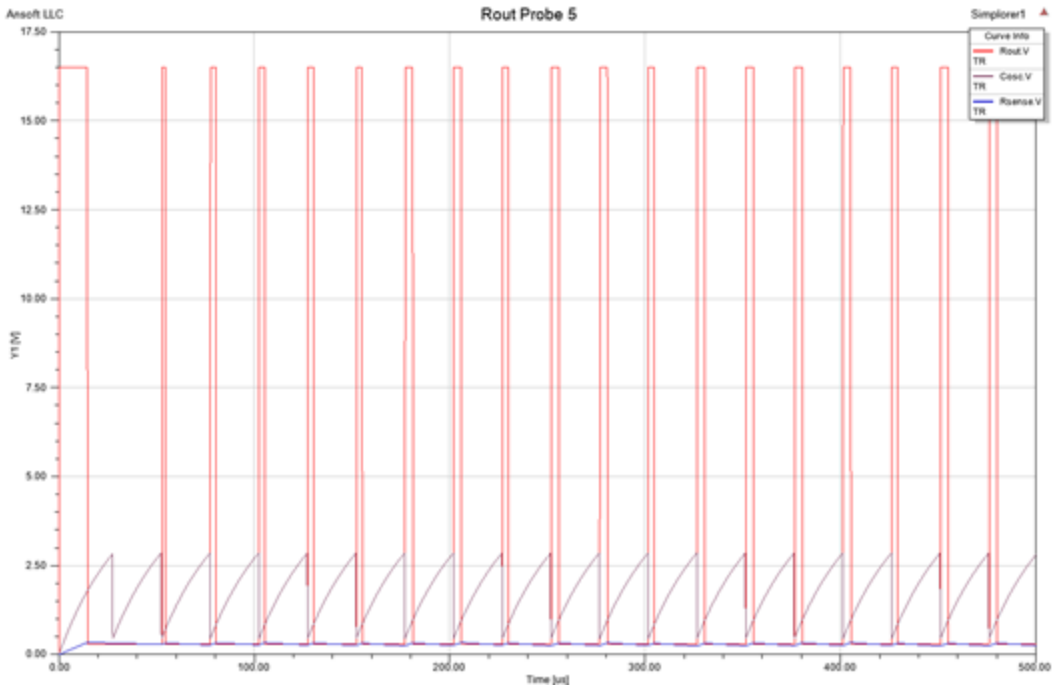

Purple: RC oscillator voltage

Red: output voltage

Figure 3. Simulation results

In this simulation, the oscillator frequency is set to 160 kHz approximately by using a 1nF capacitor and a 10kΩ resistor.

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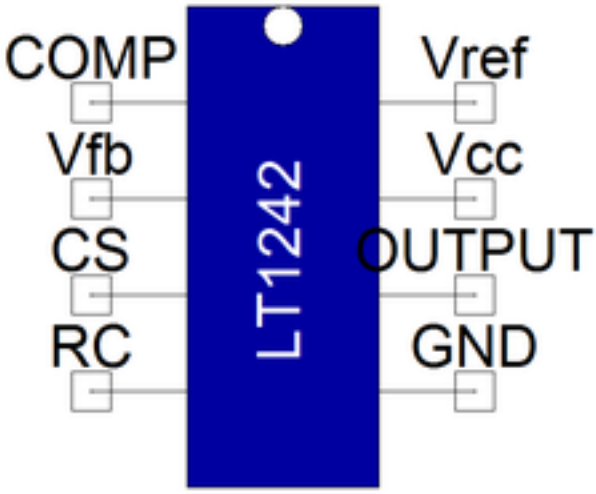
LT1242: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

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Table 1

Symbol	Description
COMP	Output of the error amplifier
Vfb	Inverting input of the error amplifier

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CS	Input to the current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vcc	Power input
OUTPUT	Output of the driver
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Table 2

PARAMETER	CONDITIONS	•	REAL Component			MODEL	UNITS
			MIN	TYP	MAX		
Reference section							
Output Voltage	IO = 1mA, TJ = 25 C		4.925	5.000	5.075	5.000	V
Line Regulation	12V < VCC < 25V	●		3	20	0	mV
Load Regulation	1mA < IVREF < 20mA	●		-6	-25	0	mV
Temperature Stability				0.1		0	mV/C
Total Output Variation	Line, Load, Temp	●	4.87		5.13	0	V
Output Noise Voltage	10Hz < F < 10kHz, TJ =25 C		50			0	V
Long Term Stability	TA = 125° C, 1000 Hrs.			5	25	0	mV
Output Short-Circuit Current		●	-30	-90	-180	X	mA
Oscillator section							
Initial Accuracy	RT = 10k, CT = 3.3nF, TJ =		47.5	50	52.5	50	kHz

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	25 C						
	RT = 13.0k, CT = 500pF, TJ = 25 C		228	248	268	250	kHz
Voltage Stability	12V < VCC < 25V, TJ = 25 C				1	0	%
Temperature Stability	TMIN < TJ < TMAX			-0.05		0	%/C
Amplitude	TJ = 25 C (Pin 4)			1.7		1.7	V
Clock Ramp Reset Current	VOSC (Pin 4) = 2V, TJ = 25 C		7.9	8.2	8.5	X	mA
Error amplifier section							
Feedback Pin Input Voltage	VPIN1 = 2.5V	●	2.42	2.50	2.58	2.50	V
Input Bias Current	VFB = 2.5V	●			-2	0	µA
Open-Loop Voltage Gain	2 < VO < 4V	●	65	90		X	dB
Unity-Gain Bandwidth	TJ = 25 C		0.7	1.3	2	X	MHz
Power Supply Rejection Ratio	12V < VCC < 25V	●	60			60	dB
Output Sink Current	VPIN2 = 2.7V, VPIN1 = 1.1V	●	2	6		0	mA
Output Source Current	VPIN2 = 2.3V, VPIN1 = 5V	●	-0.5	-0.75		0	mA
Output Voltage High Level	VPIN2 = 2.3V, RL = 15k to GND	●	5	5.6		5.6	V
Output Voltage Low Level	VPIN2 = 2.7V, RL = 15k to Pin 8	●	0.2	1.1		0.2	V
Current sense section							
Gain		●	2.85	3.00	3.15	3.00	V/V
Maximum Current Sense Input Threshold	VPIN3 < 1.1V	●	0.90	1.00	1.10	1.00	V
Power Supply Rejection Ratio		●		70		X	dB
Input Bias Current		●		-1	10	0	µA
Delay to Output		●		50	100	0	ns
Blanking Time				100		100	ns
Blanking Override Voltage				1.5		X	V
Output section							
Output Low Level	IOUT = 20mA	●		0.25	0.4	0.3	V
	IOUT = 200mA	●		0.75	2.2	0.3	V
Output High Level	IOUT = 20mA	●	12.0			Vcc	V
	IOUT = 200mA	●		11.75		Vcc	V
Rise Time	CL = 1nF, TJ = 25 C			50	80	X	ns

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Fall Time	CL = 1.0nF, TJ = 25 C			30	60	X	ns
Output Clamp Voltage	IO = 1mA	●		18	19.5	18	V
Under-voltage Lockout							
Start-Up Threshold		●	15	16	17	16	V
Minimum Operating Voltage		●	9	10	11	10	V
Hysteresis			5.5	6.0		6.0	V
PWM							
Maximum Duty Cycle	TJ = 25 C		94	96		96	%
Minimum Duty Cycle		●	0			0	%
Total device							
Start-Up Current		●		170	250	X	µA
Operating Current		●		7	10	X	mA

The ● denotes those specifications which apply over the full operating temperature range.

X: not implemented

Note 1: Unless otherwise specified, VCC = 15V, RT = 10k, CT = 3.3nF.
Note 2: Low duty cycle pulse techniques are used during test to maintain junction temperature close to ambient.

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Example circuit :

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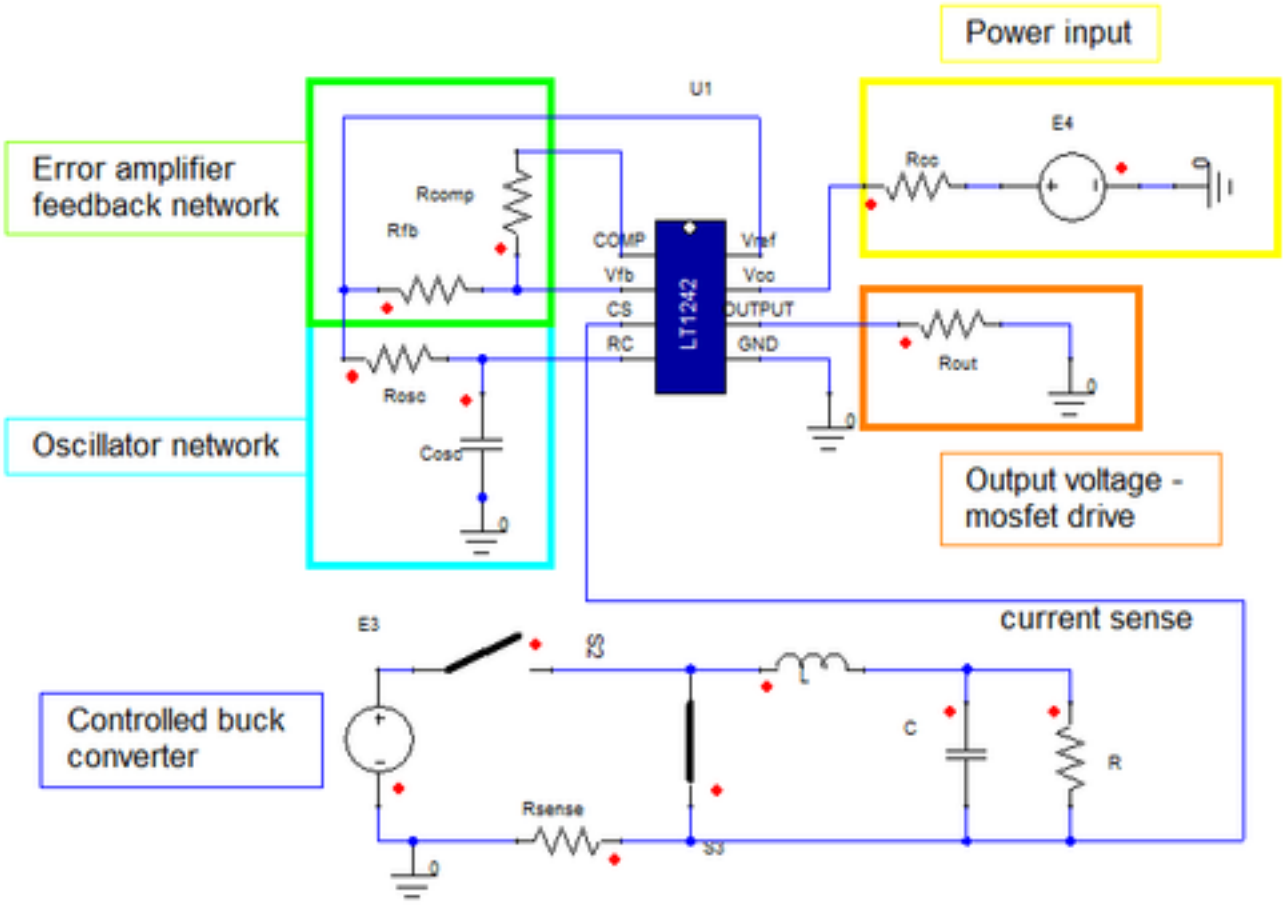

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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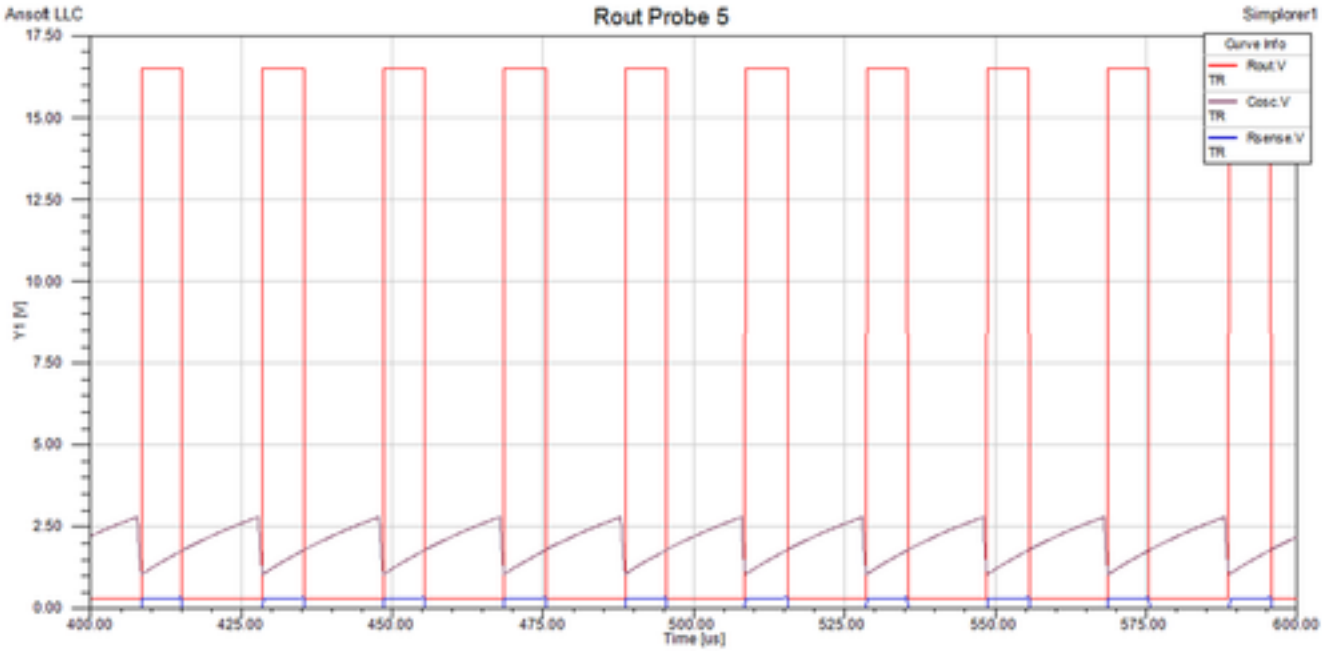

Purple: RC oscillator voltage

Red: output voltage

Figure 3. Simulation results

In this simulation, the oscillator frequency is set to 50 kHz approximately by using a 3.3nF capacitor and a 10kΩ resistor.

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LT1243: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

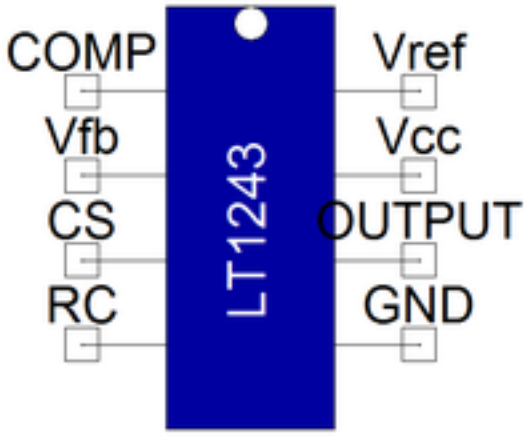

Figure 1. Component symbol

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Description

The *LT124x* series devices are fixed frequency, current mode, pulse width modulators. These devices have both improved speed and lower quiescent current. The *LT124x* series is optimized for off-line and DC/DC converter applications. They contain a high gain error amplifier, current sensing comparator and a high current totem pole output stage ideally suited to driving power MOSFETs. Leading edge blanking has been added to the current sense comparator. The output stage is clamped to a maximum VOUT of 18V in the on state. The output and the reference output are actively pulled low during under-voltage lockout.

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This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:

• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is 100kΩ. A switch disconnects the voltmeter from the input during the first 100ns of a cycle providing leading edge blanking.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: voltage limited by a zener diode to 18V.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 7.6V, the protection activates and the output and the reference fall to zero), the oscillator, the output voltage and the leading edge blanking.

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Symbol	Description
COMP	Output of the error amplifier
Vfb	Inverting input of the error amplifier

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CS	Input to the current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vcc	Power input
OUTPUT	Output of the driver
GROUND	Reference ground and power ground

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Comparison between model and real component.

Table 2

PARAMETER	CONDITIONS	•	REAL Component			MODEL	UNITS
			MIN	TYP	MAX		
Reference section							
Output Voltage	IO = 1mA, TJ = 25 C		4.925	5.000	5.075	5.000	V
Line Regulation	12V < VCC < 25V	●		3	20	0	mV
Load Regulation	1mA < IVREF < 20mA	●		-6	-25	0	mV
Temperature Stability				0.1		0	mV/C
Total Output Variation	Line, Load, Temp	●	4.87		5.13	0	V
Output Noise Voltage	10Hz < F < 10kHz, TJ =25 C		50			0	V
Long Term Stability	TA = 125° C, 1000 Hrs.			5	25	0	mV
Output Short-Circuit Current		●	-30	-90	-180	X	mA

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Oscillator section							
Initial Accuracy	RT = 10k, CT = 3.3nF, TJ = 25 C		47.5	50	52.5	50	kHz
	RT = 13.0k, CT = 500pF, TJ = 25 C		228	248	268	250	kHz
Voltage Stability	12V < VCC < 25V, TJ = 25 C				1	0	%
Temperature Stability	TMIN < TJ < TMAX			-0.05		0	%/C
Amplitude	TJ = 25 C (Pin 4)			1.7		1.7	V
Clock Ramp Reset Current	VOSC (Pin 4) = 2V, TJ = 25 C		7.9	8.2	8.5	X	mA
Error amplifier section							
Feedback Pin Input Voltage	VPIN1 = 2.5V	●	2.42	2.50	2.58	2.50	V
Input Bias Current	VFB = 2.5V	●			-2	0	µA
Open-Loop Voltage Gain	2 < VO < 4V	●	65	90		X	dB
Unity-Gain Bandwidth	TJ = 25 C		0.7	1.3	2	X	MHz
Power Supply Rejection Ratio	12V < VCC < 25V	●	60			60	dB
Output Sink Current	VPIN2 = 2.7V, VPIN1 = 1.1V	●	2	6		0	mA
Output Source Current	VPIN2 = 2.3V, VPIN1 = 5V	●	-0.5	-0.75		0	mA
Output Voltage High Level	VPIN2 = 2.3V, RL = 15k to GND	●	5	5.6		5.6	V
Output Voltage Low Level	VPIN2 = 2.7V, RL = 15k to Pin 8	●	0.2	1.1		0.2	V
Current sense section							
Gain		●	2.85	3.00	3.15	3.00	V/V
Maximum Current Sense Input Threshold	VPIN3 < 1.1V	●	0.90	1.00	1.10	1.00	V
Power Supply Rejection Ratio		●		70		X	dB
Input Bias Current		●		-1	10	0	µA
Delay to Output		●		50	100	0	ns
Blanking Time				100		100	ns
Blanking Override Voltage				1.5		X	V
Output section							
Output Low Level	IOUT = 20mA	●		0.25	0.4	0.3	V
	IOUT = 200mA	●		0.75	2.2	0.3	V

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Output High Level	IOUT = 20mA	●	12.0			Vcc	V
	IOUT = 200mA	●		11.75		Vcc	V
Rise Time	CL = 1nF, TJ = 25 C			50	80	X	ns
Fall Time	CL = 1.0nF, TJ = 25 C			30	60	X	ns
Output Clamp Voltage	IO = 1mA	●		18	19.5	18	V
Under-voltage Lockout							
Start-Up Threshold		●	7.8	8.4	9.0	16	V
Minimum Operating Voltage		●	7.0	7.6	8.2	10	V
Hysteresis			5.5	6.0		6.0	V
PWM							
Maximum Duty Cycle	TJ = 25 C		94	96		96	%
Minimum Duty Cycle		●	0			0	%
Total device							
Start-Up Current		●		170	250	X	µA
Operating Current		●		7	10	X	mA

The ● denotes those specifications which apply over the full operating temperature range.

X: not implemented

Note 1: Unless otherwise specified, VCC = 15V, RT = 10k, CT = 3.3nF.
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Example circuit :

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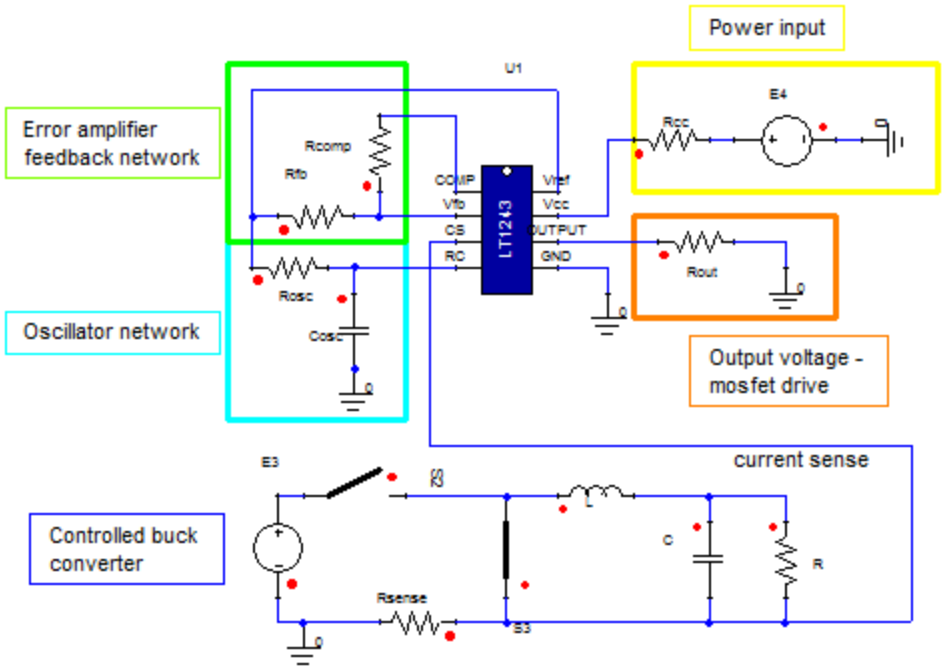
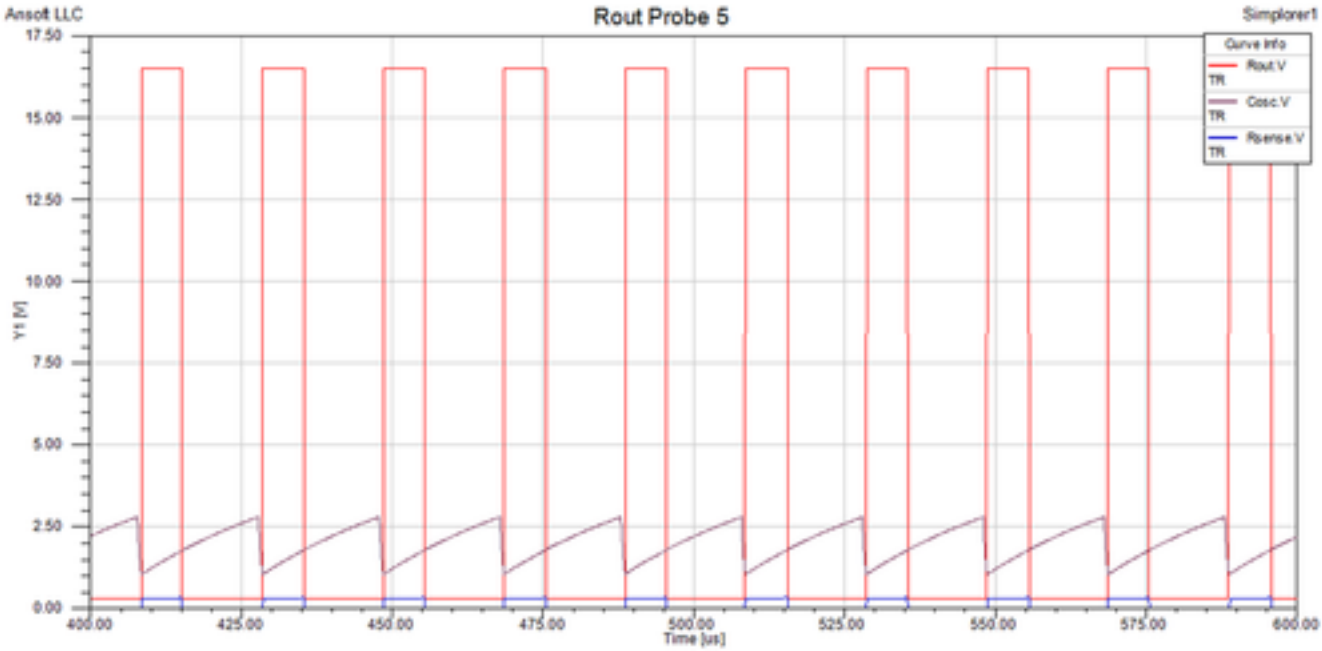


Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :



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Purple: RC oscillator voltage

Red: output voltage

Figure 3. Simulation results

In this simulation, the oscillator frequency is set to 50 kHz approximately by using a 3.3nF capacitor and a 10kΩ resistor.

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LT1244: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

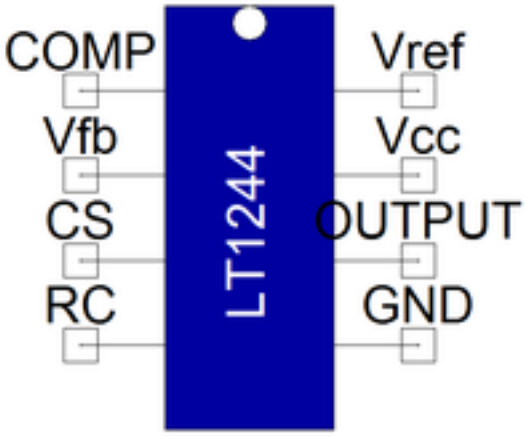

Figure 1. Component symbol

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Description

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Table 1

Symbol	Description
COMP	Output of the error amplifier
Vfb	Inverting input of the error amplifier

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CS	Input to the current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vcc	Power input
OUTPUT	Output of the driver
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Table 2

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			MIN	TYP	MAX		
Reference section							
Output Voltage	IO = 1mA, TJ = 25 C		4.925	5.000	5.075	5.000	V
Line Regulation	12V < VCC < 25V	●		3	20	0	mV
Load Regulation	1mA < IVREF < 20mA	●		-6	-25	0	mV
Temperature Stability				0.1		0	mV/C
Total Output Variation	Line, Load, Temp	●	4.87		5.13	0	V
Output Noise Voltage	10Hz < F < 10kHz, TJ =25 C		50			0	V
Long Term Stability	TA = 125° C, 1000 Hrs.			5	25	0	mV
Output Short-Circuit Current		●	-30	-90	-180	X	mA

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Oscillator section							
Initial Accuracy	RT = 10k, CT = 3.3nF, TJ = 25 C		47.5	50	52.5	50	kHz
	RT = 13.0k, CT = 500pF, TJ = 25 C		228	248	268	250	kHz
Voltage Stability	12V < VCC < 25V, TJ = 25 C				1	0	%
Temperature Stability	TMIN < TJ < TMAX			-0.05		0	%/C
Amplitude	TJ = 25 C (Pin 4)			1.7		1.7	V
Clock Ramp Reset Current	VOSC (Pin 4) = 2V, TJ = 25 C		7.9	8.2	8.5	X	mA
Error amplifier section							
Feedback Pin Input Voltage	VPIN1 = 2.5V	●	2.42	2.50	2.58	2.50	V
Input Bias Current	VFB = 2.5V	●			-2	0	µA
Open-Loop Voltage Gain	2 < VO < 4V	●	65	90		X	dB
Unity-Gain Bandwidth	TJ = 25 C		0.7	1.3	2	X	MHz
Power Supply Rejection Ratio	12V < VCC < 25V	●	60			60	dB
Output Sink Current	VPIN2 = 2.7V, VPIN1 = 1.1V	●	2	6		0	mA
Output Source Current	VPIN2 = 2.3V, VPIN1 = 5V	●	-0.5	-0.75		0	mA
Output Voltage High Level	VPIN2 = 2.3V, RL = 15k to GND	●	5	5.6		5.6	V
Output Voltage Low Level	VPIN2 = 2.7V, RL = 15k to Pin 8	●	0.2	1.1		0.2	V
Current sense section							
Gain		●	2.85	3.00	3.15	3.00	V/V
Maximum Current Sense Input Threshold	VPIN3 < 1.1V	●	0.90	1.00	1.10	1.00	V
Power Supply Rejection Ratio		●		70		X	dB
Input Bias Current		●		-1	10	0	µA
Delay to Output		●		50	100	0	ns
Blanking Time				100		100	ns
Blanking Override Voltage				1.5		X	V
Output section							
Output Low Level	IOUT = 20mA	●		0.25	0.4	0.3	V
	IOUT = 200mA	●		0.75	2.2	0.3	V
Output High Level	IOUT = 20mA	●	12.0			Vcc	V
	IOUT = 200mA	●		11.75		Vcc	V

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Rise Time	CL = 1nF, TJ = 25 C			50	80	X	ns
Fall Time	CL = 1.0nF, TJ = 25 C			30	60	X	ns
Output Clamp Voltage	IO = 1mA	●		18	19.5	18	V
Under-voltage Lockout							
Start-Up Threshold		●	15	16	17	16	V
Minimum Operating Voltage		●	9.0	10	11	10	V
Hysteresis			5.5	6.0		6.0	V
PWM							
Maximum Duty Cycle	TJ = 25 C		46	48		48	%
Minimum Duty Cycle		●	0			0	%
Total device							
Start-Up Current		●		170	250	X	µA
Operating Current		●		7	10	X	mA

The ● denotes those specifications which apply over the full operating temperature range.

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Example circuit :

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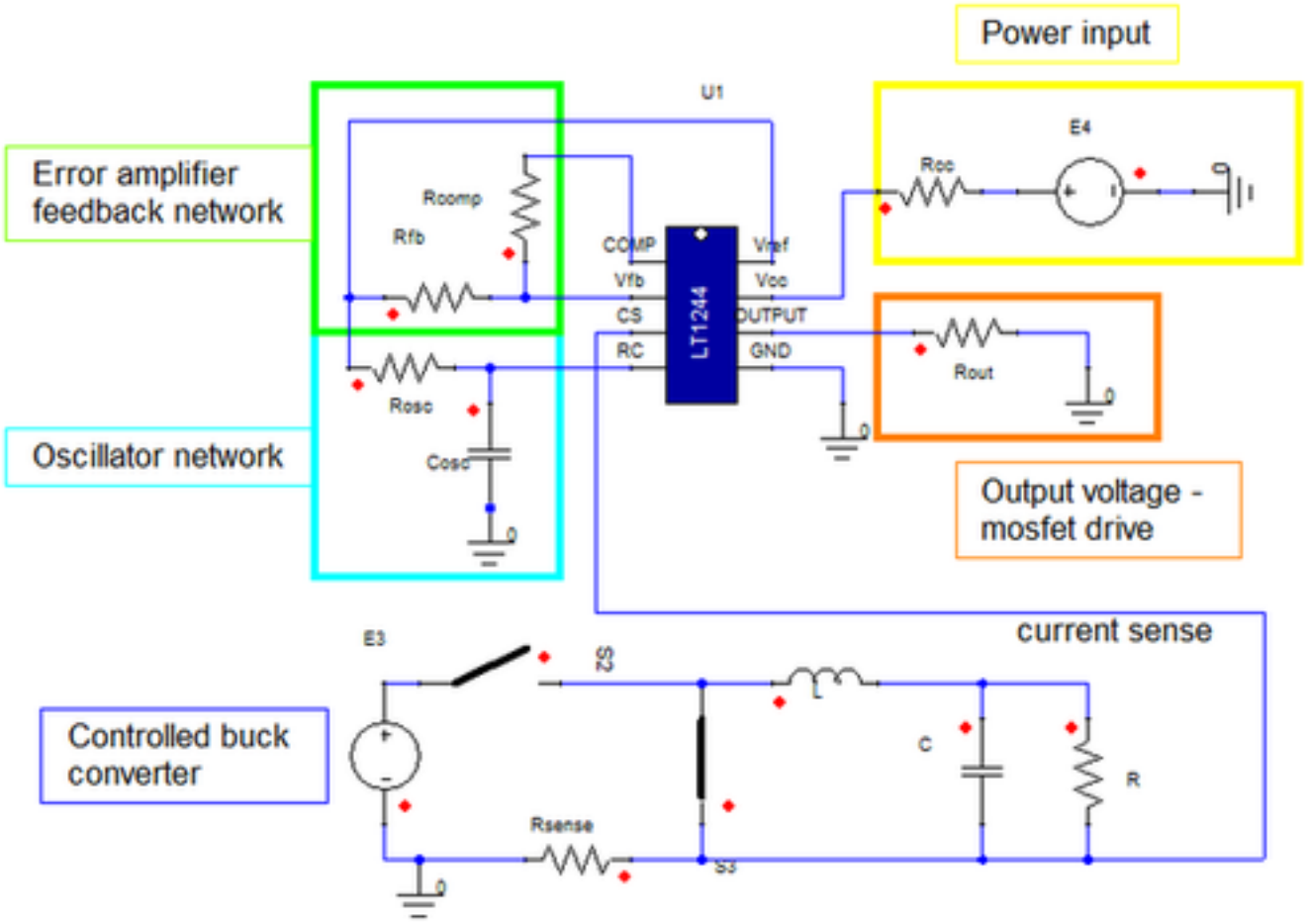

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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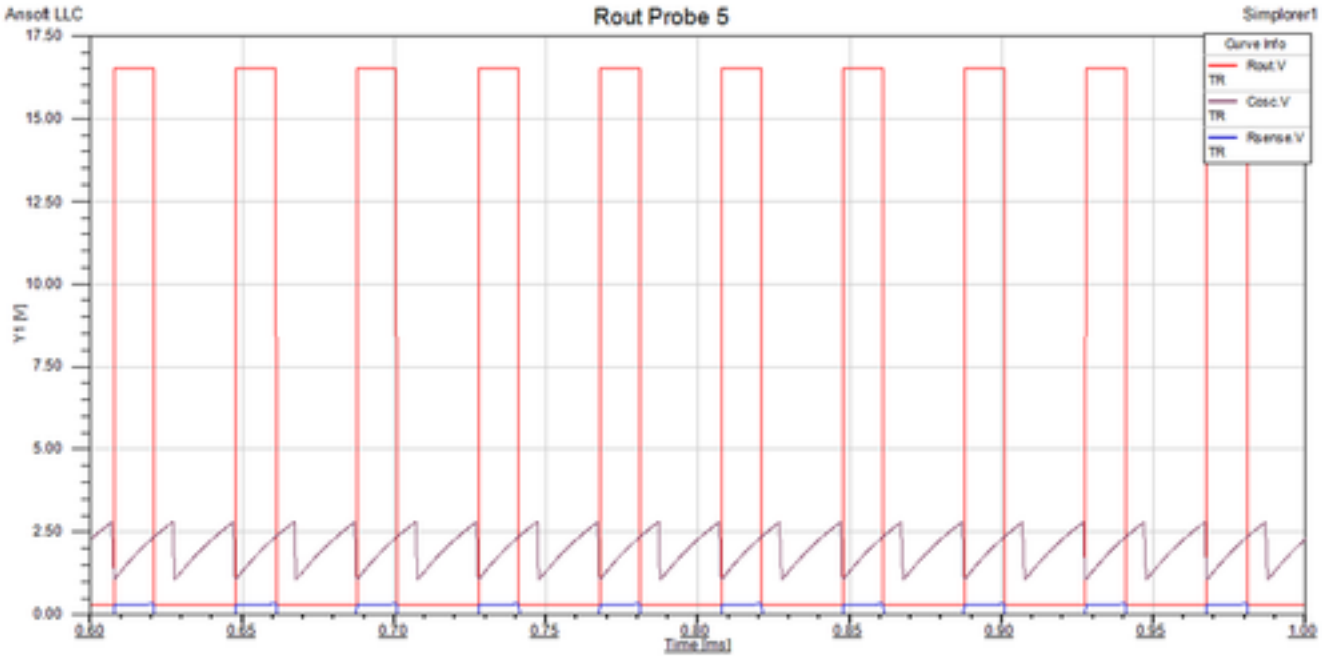

Purple: RC oscillator voltage

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Figure 3. Simulation results

In this simulation, the oscillator frequency is set to 50 kHz approximately by using a 3.3nF capacitor and a 10kΩ resistor.

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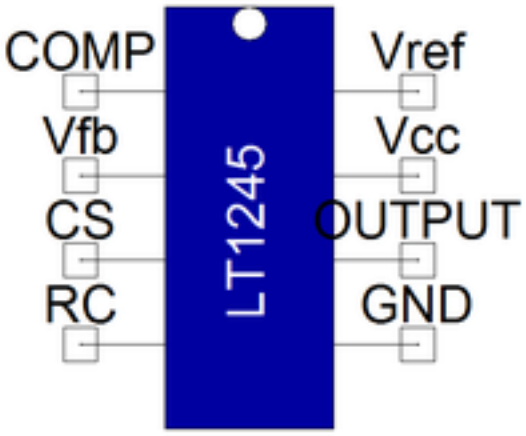
LT1245: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

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COMP	Output of the error amplifier
Vfb	Inverting input of the error amplifier

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CS	Input to the current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vcc	Power input
OUTPUT	Output of the driver
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Table 2

PARAMETER	CONDITIONS	•	REAL Component			MODEL	UNITS
			MIN	TYP	MAX		
Reference section							
Output Voltage	IO = 1mA, TJ = 25 C		4.925	5.000	5.075	5.000	V
Line Regulation	12V < VCC < 25V	●		3	20	0	mV
Load Regulation	1mA < IVREF < 20mA	●		-6	-25	0	mV
Temperature Stability				0.1		0	mV/C
Total Output Variation	Line, Load, Temp	●	4.87		5.13	0	V
Output Noise Voltage	10Hz < F < 10kHz, TJ =25 C		50			0	V
Long Term Stability	TA = 125° C, 1000 Hrs.			5	25	0	mV
Output Short-Circuit Current		●	-30	-90	-180	X	mA

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Oscillator section							
Initial Accuracy	RT = 10k, CT = 3.3nF, TJ = 25 C		47.5	50	52.5	50	kHz
	RT = 13.0k, CT = 500pF, TJ = 25 C		228	248	268	250	kHz
Voltage Stability	12V < VCC < 25V, TJ = 25 C			1		0	%
Temperature Stability	TMIN < TJ < TMAX			-0.05		0	%/C
Amplitude	TJ = 25 C (Pin 4)			1.7		1.7	V
Clock Ramp Reset Current	VOSC (Pin 4) = 2V, TJ = 25 C		7.9	8.2	8.5	X	mA
Error amplifier section							
Feedback Pin Input Voltage	VPIN1 = 2.5V	●	2.42	2.50	2.58	2.50	V
Input Bias Current	VFB = 2.5V	●			-2	0	µA
Open-Loop Voltage Gain	2 < VO < 4V	●	65	90		X	dB
Unity-Gain Bandwidth	TJ = 25 C		0.7	1.3	2	X	MHz
Power Supply Rejection Ratio	12V < VCC < 25V	●	60			60	dB
Output Sink Current	VPIN2 = 2.7V, VPIN1 = 1.1V	●	2	6		0	mA
Output Source Current	VPIN2 = 2.3V, VPIN1 = 5V	●	-0.5	-0.75		0	mA
Output Voltage High Level	VPIN2 = 2.3V, RL = 15k to GND	●	5	5.6		5.6	V
Output Voltage Low Level	VPIN2 = 2.7V, RL = 15k to Pin 8	●	0.2	1.1		0.2	V
Current sense section							
Gain		●	2.85	3.00	3.15	3.00	V/V
Maximum Current Sense Input Threshold	VPIN3 < 1.1V	●	0.90	1.00	1.10	1.00	V
Power Supply Rejection Ratio		●		70		X	dB
Input Bias Current		●		-1	10	0	µA
Delay to Output		●		50	100	0	ns
Blanking Time				100		100	ns
Blanking Override Voltage				1.5		X	V
Output section							
Output Low Level	IOUT = 20mA	●		0.25	0.4	0.3	V
	IOUT = 200mA	●		0.75	2.2	0.3	V

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Output High Level	IOUT = 20mA	●	12.0			Vcc	V
	IOUT = 200mA	●		11.75		Vcc	V
Rise Time	CL = 1nF, TJ = 25 C			50	80	X	ns
Fall Time	CL = 1.0nF, TJ = 25 C			30	60	X	ns
Output Clamp Voltage	IO = 1mA	●		18	19.5	18	V
Under-voltage Lockout							
Start-Up Threshold		●	7.8	8.4	9.0	16	V
Minimum Operating Voltage		●	7.0	7.6	8.2	10	V
Hysteresis			5.5	6.0		6.0	V
PWM							
Maximum Duty Cycle	TJ = 25 C		46	48		48	%
Minimum Duty Cycle		●	0			0	%
Total device							
Start-Up Current		●		170	250	X	µA
Operating Current		●		7	10	X	mA

The ● denotes those specifications which apply over the full operating temperature range.

X: not implemented

Note 1: Unless otherwise specified, VCC = 15V, RT = 10k, CT = 3.3nF.
Note 2: Low duty cycle pulse techniques are used during test to maintain junction temperature close to ambient.

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Example circuit :

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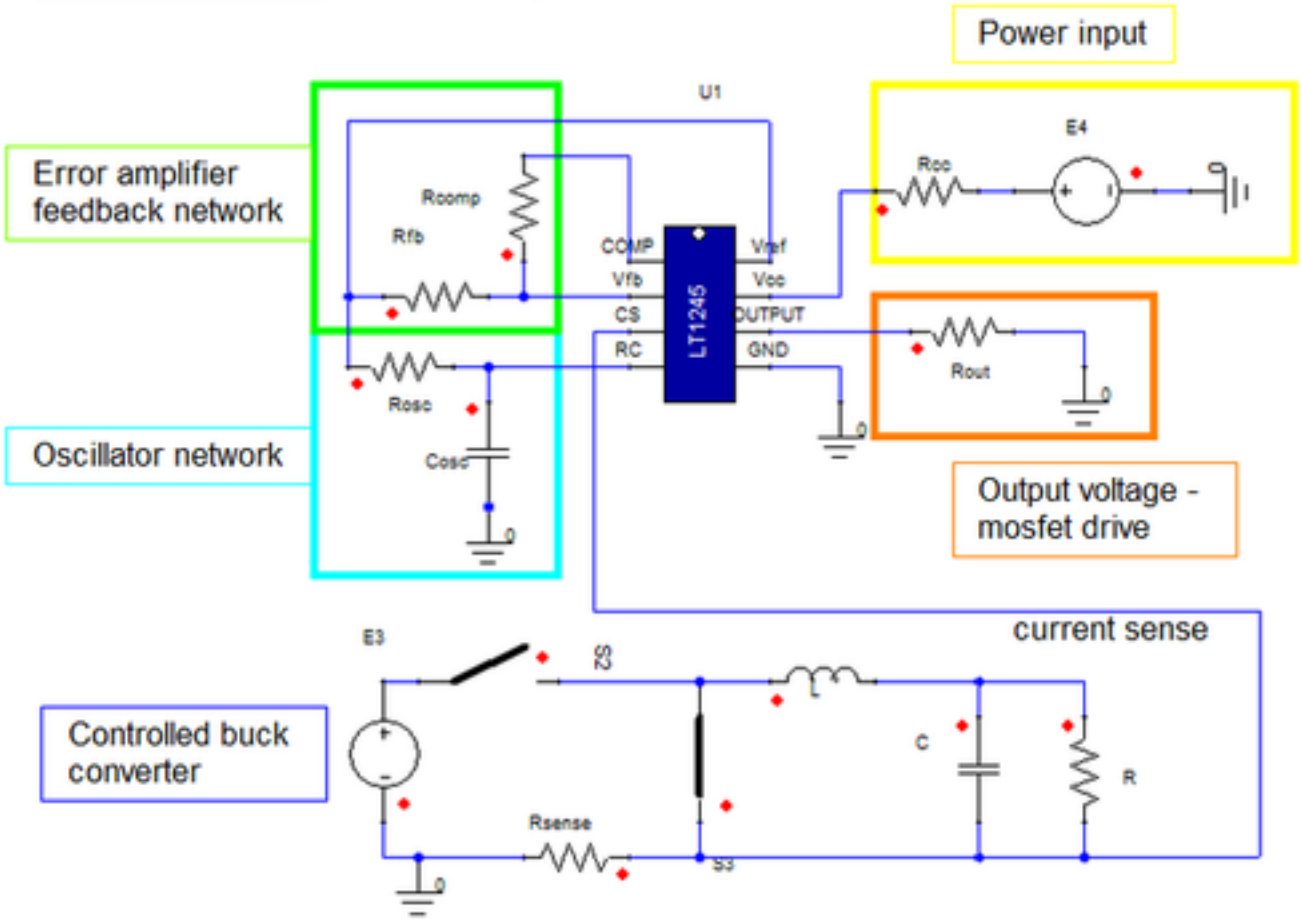

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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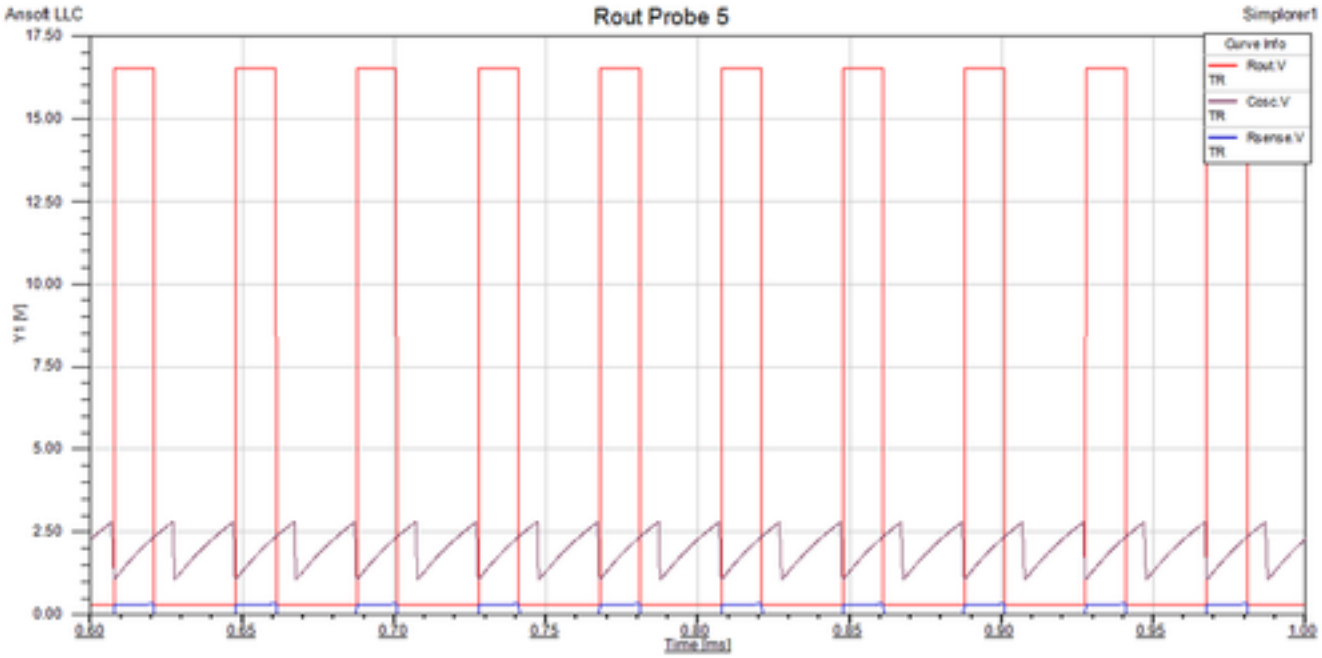

Purple: RC oscillator voltage

Red: output voltage

Figure 3. Simulation results

In this simulation, the oscillator frequency is set to 50 kHz approximately by using a 3.3nF capacitor and a 10kΩ resistor.

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References

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UCC28950: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

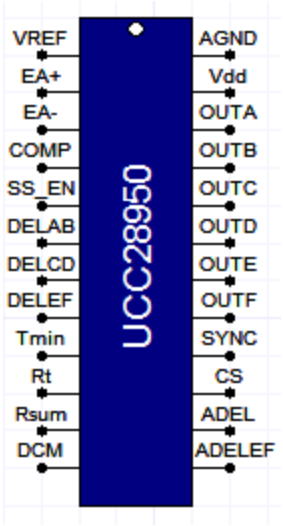

Figure 1. Component symbol

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Description

The UCC28950 enhanced phase-shifted controller builds upon Texas Instrument's industry standard UCx895 phase-shifted controller family with enhancements that offer best in class efficiency in today's high performance power systems. The UCC28950 implements advanced control of the full–bridge along with active control of the synchronous rectifier output stage.

The primary-side signals allow programmable delays to ensure ZVS operation over wide-load current and input voltage range, while the load current naturally tunes the secondary-side synchronous rectifiers switching delays, maximizing overall system efficiency.

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The UCC28950 also offers multiple light-load management features including burst mode and dynamic SR on/off control when transitioning in and out of Discontinuous Current Mode (DCM) ensuring ZVS operation is extended down to much lighter loads.

In addition, the UCC28950 includes support for current or voltage mode control. Programmable switching frequency up to 1 MHz and a wide set of protection features including cycle-by-cycle current limit, UVLO and thermal shutdown. A 90-degreephase-shifted interleaved synchronized operation can be easily arranged between two converters.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	VREF	5-V, ±1.5%, 20-mA reference voltage output.
2	EA+	Error amplifier non-inverting input.
3	EA-	Error amplifier inverting input.
4	COMP	Error amplifier output and input to the PWM comparator.
5	SS/EN	Soft-start programming, device enable and hic-cup mode protection circuit.
6	DELAB	Dead-time delay programming between OUTA and OUTB.
7	DELCD	Dead-time delay programming between OUTC and OUTD.
8	DELEF	Delay-time programming between OUTA to OUTF, and OUTB to OUTE.
9	TMIN	Minimum duty cycle programming in burst mode.
10	RT	Oscillator frequency set. Primary or secondary mode setting.
11	RSUM	Slope compensation programming. Voltage mode or peak current mode setting.
12	DCM	DCM threshold setting.
13	ADELEF	Delay-time programming between primary side and secondary side switches, TAFSET and TBESET.
14	ADEL	Dead-time programming for the primary switches over CS voltage range, TABSET and TCDSET.
15	CS	Current sense for cycle-by-cycle over-current protection and adaptive delay functions.
16	SYNC	Synchronization out from primary controller to input of secondary controller.
17	OUTF	0.2-A sink/source synchronous switching out-put.
18	OUTE	0.2-A sink/source synchronous switching out-put.
19	OUTD	0.2-A sink/source primary switching output.
20	OUTC	0.2-A sink/source primary switching output.
21	OUTB	0.2-A sink/source primary switching output.
22	OUTA	0.2-A sink/source primary switching output.

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23	VDD	Bias supply input.
24	GND	Ground. All signals are referenced to this node.

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Example circuit :

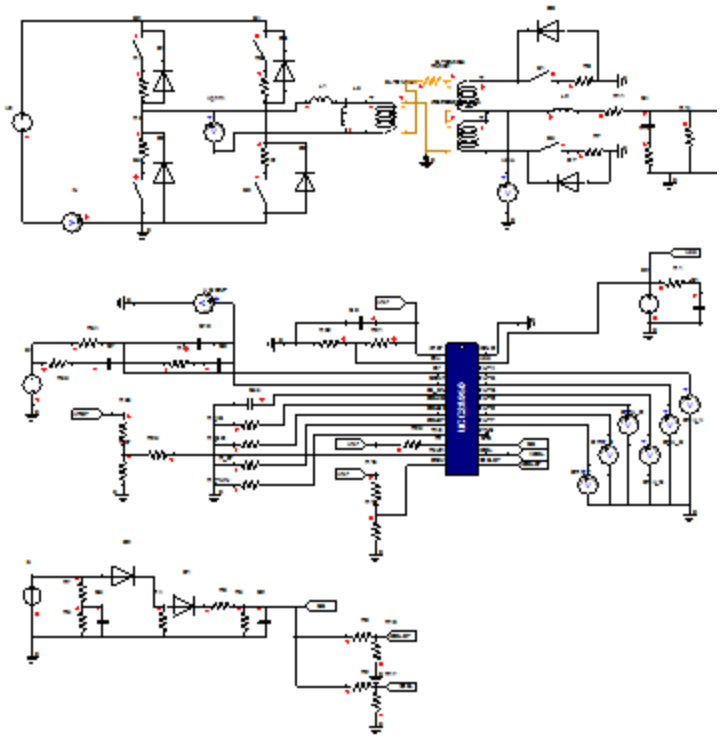

Figure 2. Example Circuit

The first part of the transient corresponds to the start-up protection; the voltages on the soft-start capacitor must be above 0.55V to generate an internal enable signal EN that initiates the soft start process.

During the soft start the duty cycle increases gradually from the minimum set by TMIN up to the steady state duty cycle required by the regulated output voltage.

After the voltage at the soft start pin reaches 3,7V at t= 3ms, soft-start is finished.

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Simulation results :

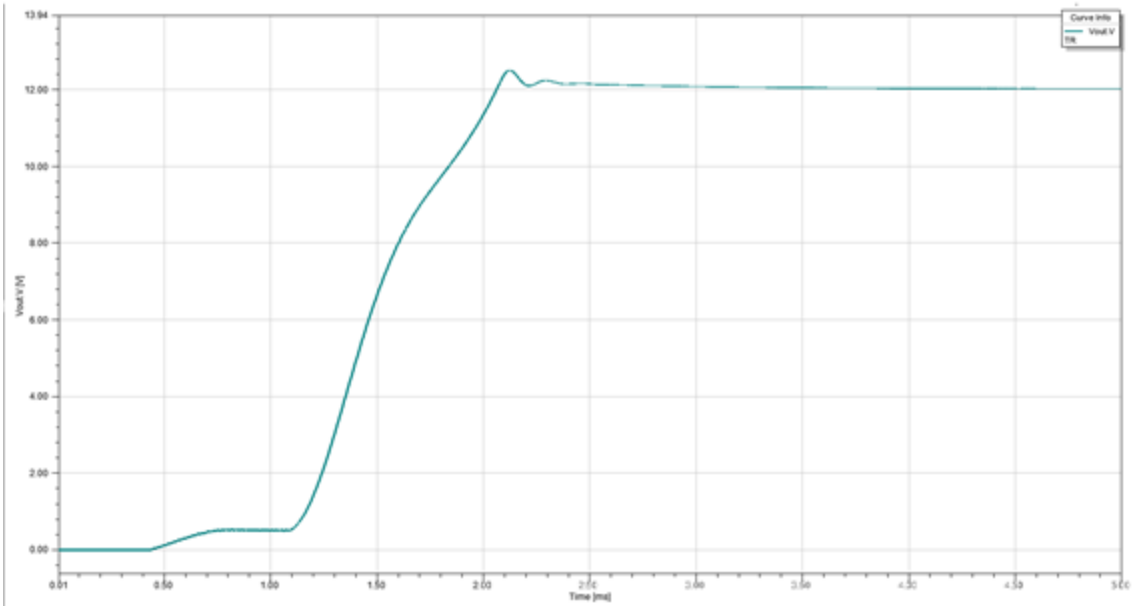

Figure 3: Output Voltage

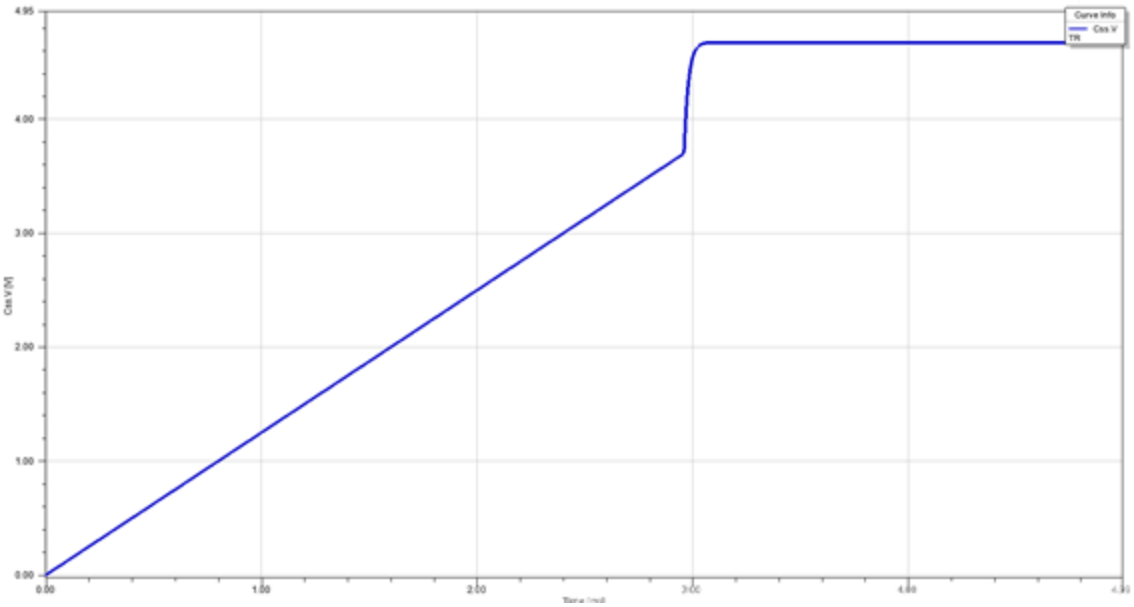

Figure 3. Soft Start Pin Voltage

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References

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UCCx5801: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

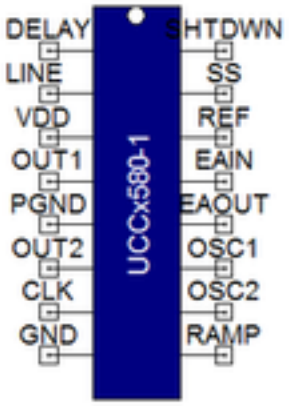

Figure 1. Component symbol

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Description

The *UCCx580* family of PWM controllers is designed to implement a variety of active clamp/reset and synchronous rectifier switching converter topologies. While containing all the necessary functions for fixed frequency, high performance pulse width modulation, the additional feature of this design is the inclusion of an auxiliary switch driver which complements the main power switch, and with a programmable deadtime or delay between each transition. The active clamp/reset technique allows operation of single ended converters beyond 50% duty cycle while reducing voltage stresses on the switches, and allows a greater flux swing for the power transformer. This approach also allows a reduction in switching losses by recovering energy stored in parasitic elements such as leakage inductance and switch capacitance.

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The oscillator is programmed with two resistors and a capacitor to set switching frequency and maximum duty cycle. A separate synchronized ramp provides a voltage feedforward pulse width modulation and a programmed maximum volt-second limit. The generated clock from the oscillator contains both frequency and maximum duty cycle information.

The main gate drive output (OUT1) is controlled by the pulse width modulator. The second output (OUT2) is intended to activate an auxiliary switch during the off time of the main switch, except that between each transition there is deadtime where both switches are off, programmed by a single external resistor. This design offers two options for OUT2, normal and inverted. In the -1 and -2 versions, OUT2 is normal and can be used to drive PMOS FETs. In the -3 and -4 versions, OUT2 is inverted and can be used to drive NMOS FETs. In all versions, both the main and auxiliary switches are held off prior to startup and when the PWM command goes to zero duty cycle. During fault conditions, OUT1 is held off while OUT2 operates at maximum duty cycle with a guaranteed off time equal to the sum of the two deadtimes.

Undervoltage lockout monitors supply voltage (VDD), the precision reference (REF), input line voltage (LINE), and the shutdown comparator (SHTDWN). If after any of these four have sensed a fault condition, recovery to full operation is initiated with a soft start. VDD thresholds, on and off, are 15V and 8.5V for the -2 and -4 versions, 9V and 8.5V for the -1 and -3 versions.

In this model we can differentiate two main parts: the electrical circuit and the logic which manages it.

The circuit consists of (from top left and counterclockwise):
- Oscillator circuitry
- Ramp circuitry
- Error amplifier
- Soft-start circuit
- Shutdown and line inputs
- Ground and power input
- Reference voltage source
- Output circuitry
- Delay setting circuit
- Output clock signal

The logic consists of six state machines. The main state machine, the one located at the bottom right, controls the main operation of the model. It opens and closes the outputs as a function of the ramp voltage, the output of the error amplifier and the programmed delays.

The other state machines control the oscillator, the undervoltage lockout feature, the line pin and the shutdown function.

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Netlist Syntax

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Conservative Pins

Table 1

Symbol	Description
DELAY	Delay programming pin.
LINE	Hysteretic comparator pin.
VDD	Chip power supply pin.
OUT1	Gate drive output for the main switch.
PGND	Ground connection for the gate drivers.
OUT2	Gate drive output for the auxiliary switch.
CLK	Oscillator clock output.
GND	Signal ground.
SHTDWN	Comparator input to stop the chip.
SS	Soft-start programming pin.
REF	Precision 5.0V reference pin.
EAIN	Inverting input to the error amplifier.
EAOUT	Output of the error amplifier.
OSC1	Oscillator programming pin (charge).
OSC2	Oscillator programming pin (discharge).
RAMP	Line feedforwardsawtooth signal.

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Parameters

Comparison between model and real component.

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Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx5801			MODEL	UNITS
		MIN	TYP	MAX		
Oscillator Section						
Frequency		370	400	430	395	kHz
CLK Pulse Width		650	750	850	650	ns
CLK V_{OH}	I_{CLK} = 3 mA	4.3	4.7		4.7	V
CLK V_{OL}	I_{CLK}Â = 3 mA		0.3	0.5	0.3	V
Ramp GeneratorSection						
Ramp V_{OL}	I_{RAMP} = 100 µA		50	100	0	mV
Flux Comparator Vth		3.16	3.33	3.50	3.33	V
Pulse WidthModulatorSection						
Minimum DutyCycle	OUT1, EAOUT = VOL			0	0	%
Maximum DutyCycle	OUT1, EAIN = 0 V	63	66	69	69	%
PWM Comparator Offset		0.1	0.4	0.9	0.4	V
Error AmplifierSection						
EAIN	EAOUT = EAIN	2.44	2.5	2.56	2.5	V
I_{EAIN}	EAOUT = EAIN		150	400	0	nA
EAOUT, VOL	EAIN = 2.6 V, I_{EAOUT} = 100 µA		0.3	0.5	0	V
EAOUT, VOH	EAIN = 2.4 V, I_{EAOUT} = 100 µA	4	5	55	5	V
AVOL		70	80		80	dB
Gain Bandwidth Product	f = 100 kHz (Note 1)	2	6		X	MHz

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Softstart/ShutdownSection						
Start DutyCycle	EAIN = 2.4 V		0		0	%
SS V_{OL}	I_{SS} = 100 µA		100	350	0	mV
SS Restart Threshold			400	550	300	mV
I_{SS}			-20	-35	-20	µA
SHTDWN V_{TH}		0.4	0.5	0.6	0.5	V
I_{SHTDWN}			50	150	0	nA
Undervoltage Lockout Section						
VDD On		8	9	10	9	V
VDD Off	-	7.5	8.5	9.5	8.5	V
LINE On		4.7	5	5.3	5	V
LINE Off		4.2	4.5	4.8	4.5	V
I_{LINE}	LINE = 6 V		50	150	0	nA
Supply Section						
VDD Clamp	I_{VDD} = 10 mA	14	15	16	15	V
I_{VDD} Start	VDD < VDD On		160	250	0	µA
I_{VDD} Operating	No Load		2.5	3.5	0	mA
Output Drivers Section						
OUT1 V_{SAT} High	I_{OUT1} = 50 mA		0.4	1.0	X	V
OUT1 V_{SAT} Low	I_{OUT1} =100 mA		0.4	1.0	X	V
OUT2 V_{SAT} High	I_{OUT2} = 30 mA		0.4	1.0	X	V
OUT2 V_{SAT} Low	$I_{OUT2Â}$ = 30 mA		0.4	1.0	X	V
OUT1 Fall Time	C_{OUT1} = 1nF, R_S = 3		20	50	0	ns
OUT1 Rise Time	$C_{OUT1Â}$ = 1nF, R_S = 3		40	80	0	ns
OUT2 Fall Time	C_{OUT2} = 300pF, R_S = 10		20	50	0	ns
OUT2 Rise	C_{OUT2} =		20	40	0	ns

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Time	300pF, R_S = 10					
Delay 1 OUT2 to OUT1	R3 = 100 k , COUT1 = COUT2 = 15 pF	90	120	160	115	ns
-	TA = TJ = 25°C	100	120	140	115	ns
Delay 2 OUT1 to OUT2	R3 = 100 k , COUT1 = COUT2 = 15 pF	110	170	250	167	ns
-	TA = TJ = 25°C	140	170	200	167	ns
Reference Section						
REF	I_{REF} = 0	4.87	5	5.12	5	V
Load Regulation	I_{REF} = 0 mAto 1 mA		1	20	0	mV
Line Regulation	VDD = 10 V to 14 V		1	20	0	mV

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Examples

Example circuit :

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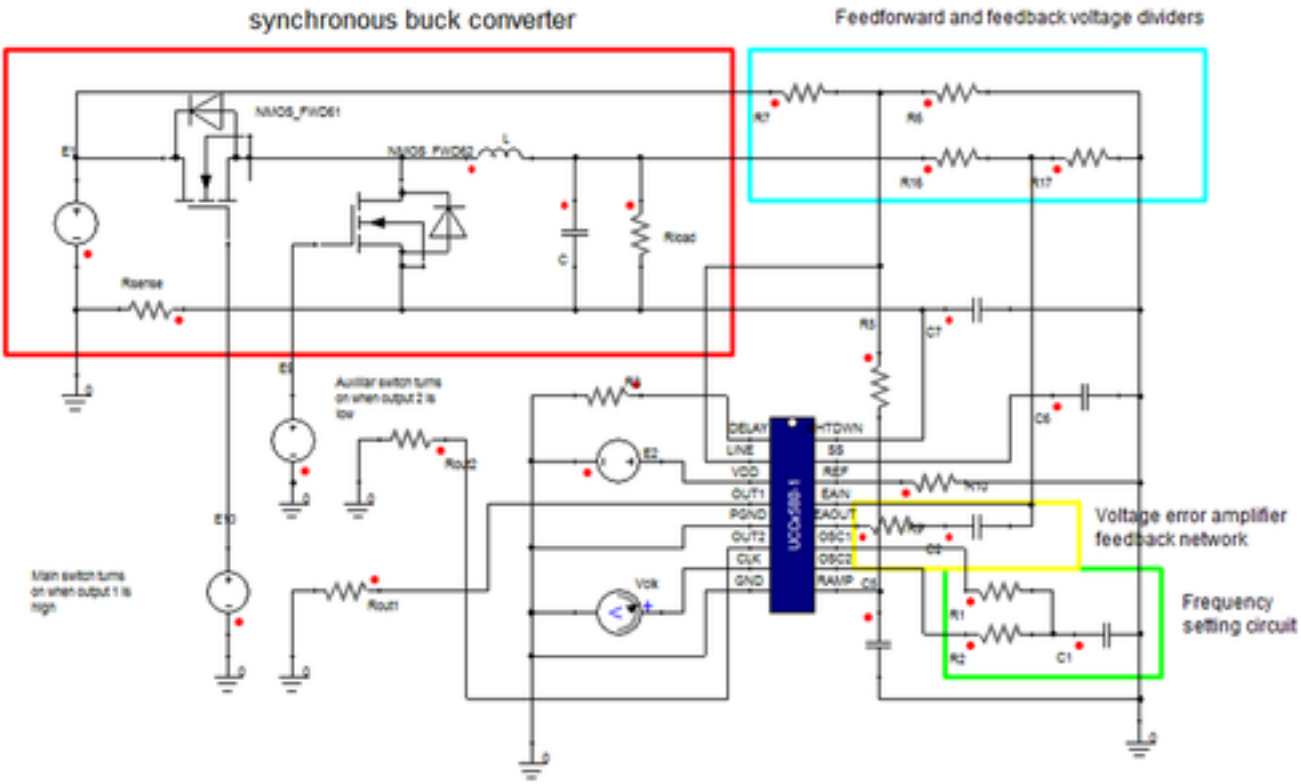

Figure 2. Example Circuit

In this example, the *UCCx580-1* is used to control a synchronous buck converter. In order to focus on the operation of the IC, MOSFETS are driven by dependant voltage sources, this way avoiding the use of a more complex circuitry. When output 1 is high, high side MOSFET is turned on and, as this IC is intended to drive a P-channel transistor with the second channel, when output 2 is low, low side MOSFET is turned on.

Simulation results :

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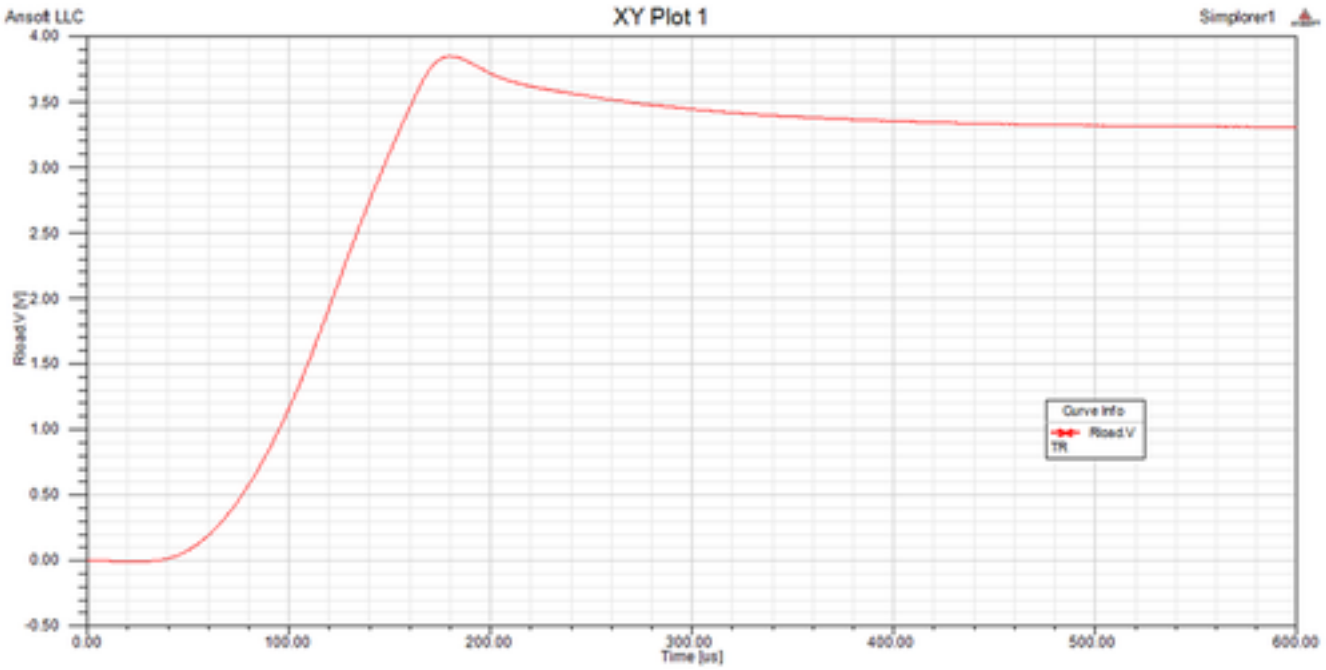
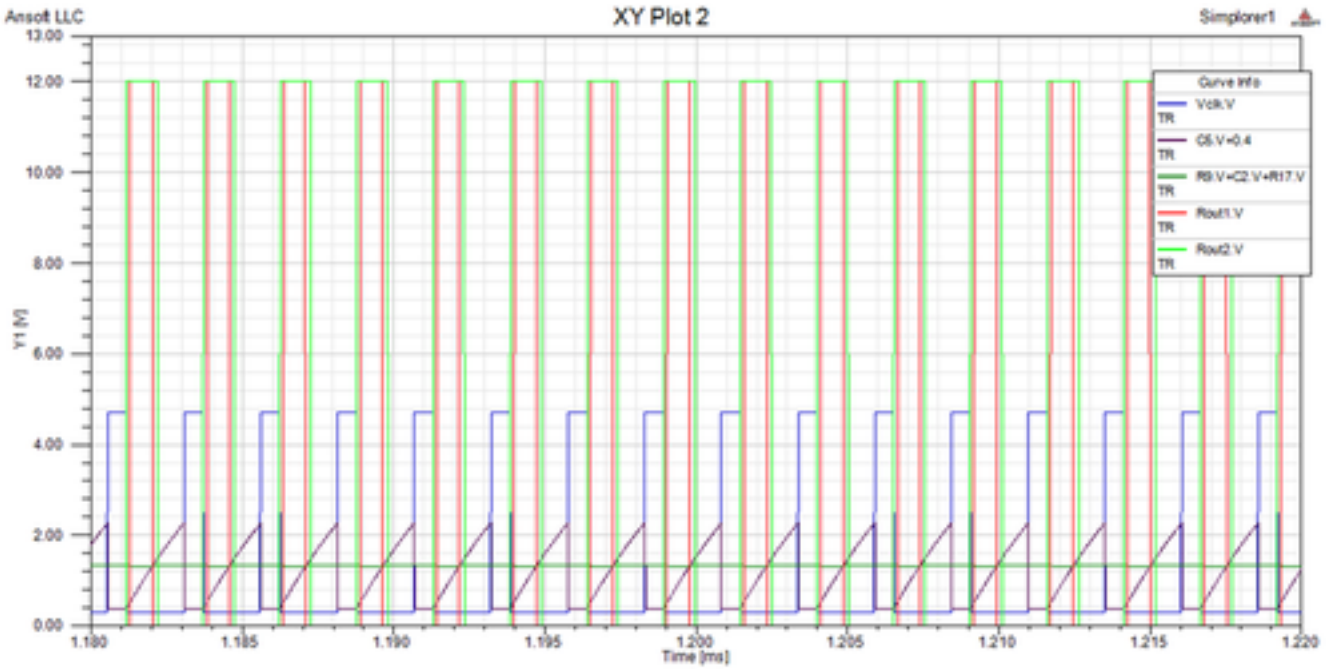


Figure 3. Simulation results(a)

In the diagram above, output voltage is shown. Note that after a transitory time of roughly 0.5ms, output matches the 3.3V regulated value.



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Red: output 1 voltage

Green: output 2 voltage

Blue: clock output

Purple: ramp voltage

Dark green: output of the error amplifier

Figure 4. Simulation results(b)

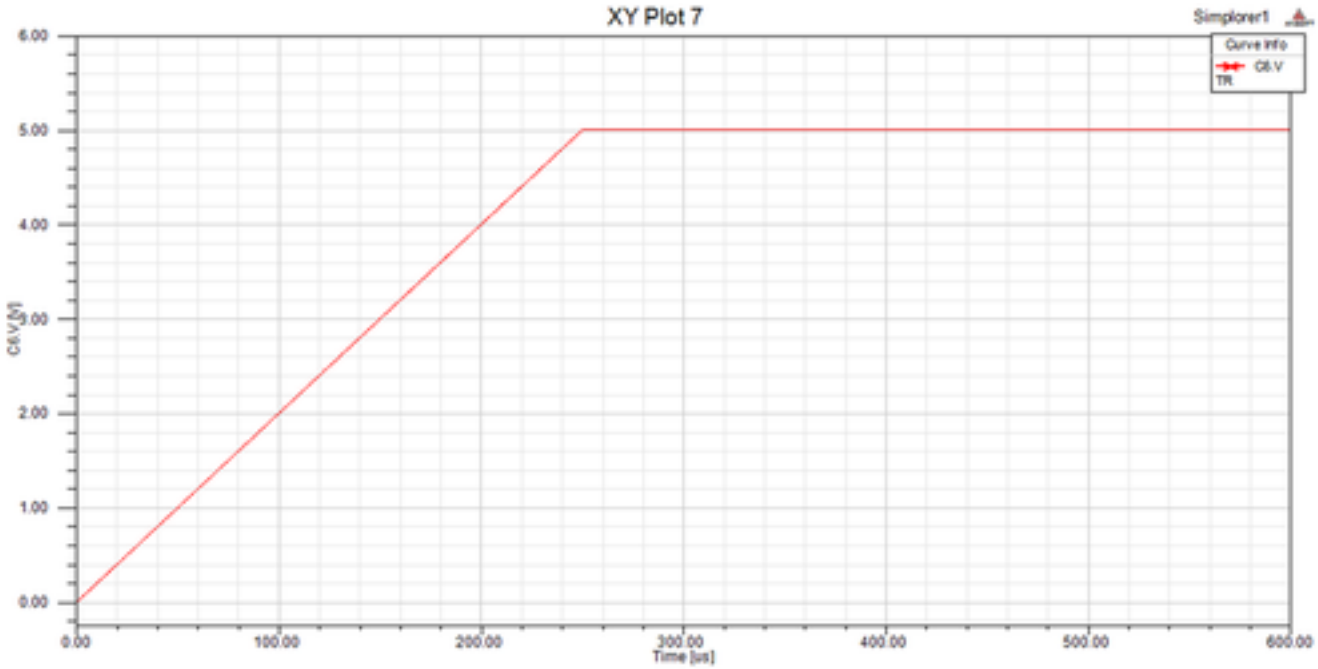

Figure 5. Simulation results(c)

In the figure above we can see the voltage on the soft-start capacitor. The aim of this function is to limit the voltage on the output of the error amplifier during the first moments after starting the device.

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References

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UCCx5802: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

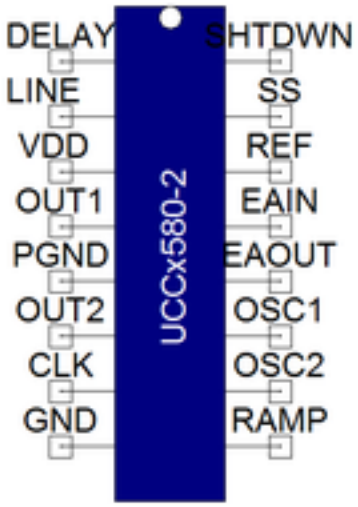

Figure 1. Component symbol

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Description

The *UCCx580* family of PWM controllers is designed to implement a variety of active clamp/reset and synchronous rectifier switching converter topologies. While containing all the necessary functions for fixed frequency, high performance pulse width modulation, the additional feature of this design is the inclusion of an auxiliary switch driver which complements the main power switch, and with a programmable deadtime or delay between each transition. The active clamp/reset technique allows operation of single ended converters beyond 50% duty cycle while reducing voltage stresses on the switches, and allows a greater flux swing for the power trans-

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former. This approach also allows a reduction in switching losses by recovering energy stored in parasitic elements such as leakage inductance and switch capacitance.

The oscillator is programmed with two resistors and a capacitor to set switching frequency and maximum duty cycle. A separate synchronized ramp provides a voltage feedforward pulse width modulation and a programmed maximum volt-second limit. The generated clock from the oscillator contains both frequency and maximum duty cycle information.

The main gate drive output (OUT1) is controlled by the pulse width modulator. The second output (OUT2) is intended to activate an auxiliary switch during the off time of the main switch, except that between each transition there is deadtime where both switches are off, programmed by a single external resistor. This design offers two options for OUT2, normal and inverted. In the -1 and -2 versions, OUT2 is normal and can be used to drive PMOS FETs. In the -3 and -4 versions, OUT2 is inverted and can be used to drive NMOS FETs. In all versions, both the main and auxiliary switches are held off prior to startup and when the PWM command goes to zero duty cycle. During fault conditions, OUT1 is held off while OUT2 operates at maximum duty cycle with a guaranteed off time equal to the sum of the two deadtimes.

Undervoltage lockout monitors supply voltage (VDD), the precision reference (REF), input line voltage (LINE), and the shutdown comparator (SHTDWN). If after any of these four have sensed a fault condition, recovery to full operation is initiated with a soft start. VDD thresholds, on and off, are 15V and 8.5V for the -2 and -4 versions, 9V and 8.5V for the -1 and -3 versions.

In this model we can differentiate two main parts: the electrical circuit and the logic which manages it.

The circuit consists of (from top left and counterclockwise):
- Oscillator circuitry
- Ramp circuitry
- Error amplifier
- Soft-start circuit
- Shutdown and line inputs
- Ground and power input
- Reference voltage source
- Output circuitry
- Delay setting circuit
- Output clock signal

The logic consists of six state machines. The main state machine, the one located at the bottom right, controls the main operation of the model. It opens and closes the outputs as a function of the ramp voltage, the output of the error amplifier and the programmed delays.

The other state machines control the oscillator, the undervoltage lockout feature, the line pin and the shutdown function.

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Conservative Pins

Table 1

Symbol	Description
DELAY	Delay programming pin.
LINE	Hysteretic comparator pin.
VDD	Chip power supply pin.
OUT1	Gate drive output for the main switch.
PGND	Ground connection for the gate drivers.
OUT2	Gate drive output for the auxiliary switch.
CLK	Oscillator clock output.
GND	Signal ground.
SHTDWN	Comparator input to stop the chip.
SS	Soft-start programming pin.
REF	Precision 5.0V reference pin.
EAIN	Inverting input to the error amplifier.
EAOUT	Output of the error amplifier.
OSC1	Oscillator programming pin (charge).
OSC2	Oscillator programming pin (discharge).
RAMP	Line feedforwardsawtooth signal.

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Comparison between model and real component.

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Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx5802			MODEL	UNITS
		MIN	TYP	MAX		
Oscillator Section						
Frequency		370	400	430	395	kHz
CLK Pulse Width		650	750	850	650	ns
CLK V_{OH}	I_{CLK} = 3 mA	4.3	4.7		4.7	V
CLK V_{OL}	I_{CLK}Â = 3 mA		0.3	0.5	0.3	V
Ramp GeneratorSection						
Ramp V_{OL}	I_{RAMP} = 100 µA		50	100	0	mV
Flux Comparator Vth		3.16	3.33	3.50	3.33	V
Pulse WidthModulatorSection						
Minimum DutyCycle	OUT1, EAOUT = VOL			0	0	%
Maximum DutyCycle	OUT1, EAIN = 0 V	63	66	69	69	%
PWM Comparator Offset		0.1	0.4	0.9	0.4	V
Error AmplifierSection						
EAIN	EAOUT = EAIN	2.44	2.5	2.56	2.5	V
I_{EAIN}	EAOUT = EAIN		150	400	0	nA
EAOUT, VOL	EAIN = 2.6 V, I_{EAOUT} = 100 µA		0.3	0.5	0	V
EAOUT, VOH	EAIN = 2.4 V, I_{EAOUT} = 100 µA	4	5	55	5	V
AVOL		70	80		80	dB
Gain Bandwidth Product	f = 100 kHz (Note 1)	2	6		X	MHz

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Softstart/ShutdownSection						
Start DutyCycle	EAIN = 2.4 V		0		0	%
SS V_{OL}	I_{SS} = 100 µA		100	350	0	mV
SS Restart Threshold			400	550	300	mV
I_{SS}			-20	-35	-20	µA
SHTDWN V_{TH}		0.4	0.5	0.6	0.5	V
I_{SHTDWN}			50	150	0	nA
Undervoltage Lockout Section						
VDD On		14	15	16	15	V
VDD Off		7.5	8.5	9.5	8.5	V
LINE On		4.7	5	5.3	5	V
LINE Off		4.2	4.5	4.8	4.5	V
I_{LINE}	LINE = 6 V		50	150	0	nA
Supply Section						
VDD Clamp	I_{VDD} = 10 mA	14	15	16	15	V
I_{VDD} Start	VDD < VDD On		160	250	0	µA
I_{VDD} Operating	No Load		2.5	3.5	0	mA
Output Drivers Section						
OUT1 V_{SAT} High	I_{OUT1} = 50 mA		0.4	1.0	X	V
OUT1 V_{SAT} Low	I_{OUT1} =100 mA		0.4	1.0	X	V
OUT2 V_{SAT} High	I_{OUT2} = 30 mA		0.4	1.0	X	V
OUT2 V_{SAT} Low	$I_{OUT2Â}$ = 30 mA		0.4	1.0	X	V
OUT1 Fall Time	C_{OUT1} = 1nF, R_S = 3		20	50	0	ns
OUT1 Rise Time	$C_{OUT1Â}$ = 1nF, R_S = 3		40	80	0	ns
OUT2 Fall Time	C_{OUT2} = 300pF, R_S = 10		20	50	0	ns

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OUT2 Rise Time	C_{OUT2} = 300pF, R_S = 10		20	40	0	ns
Delay 1 OUT2 to OUT1	R3 = 100 k , COUT1 = COUT2 = 15 pF	90	120	160	115	ns
	TA = TJ = 25°C	100	120	140	115	ns
Delay 2 OUT1 to OUT2	R3 = 100 k , COUT1 = COUT2 = 15 pF	110	170	250	167	ns
	TA = TJ = 25°C	140	170	200	167	ns
Reference Section						
REF	I_{REF} = 0	4.87	5	5.12	5	V
Load Regu-lation	I_{REF} = 0 mAto 1 mA		1	20	0	mV
Line Regu-lation	VDD = 10 V to 14 V		1	20	0	mV

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Example circuit :

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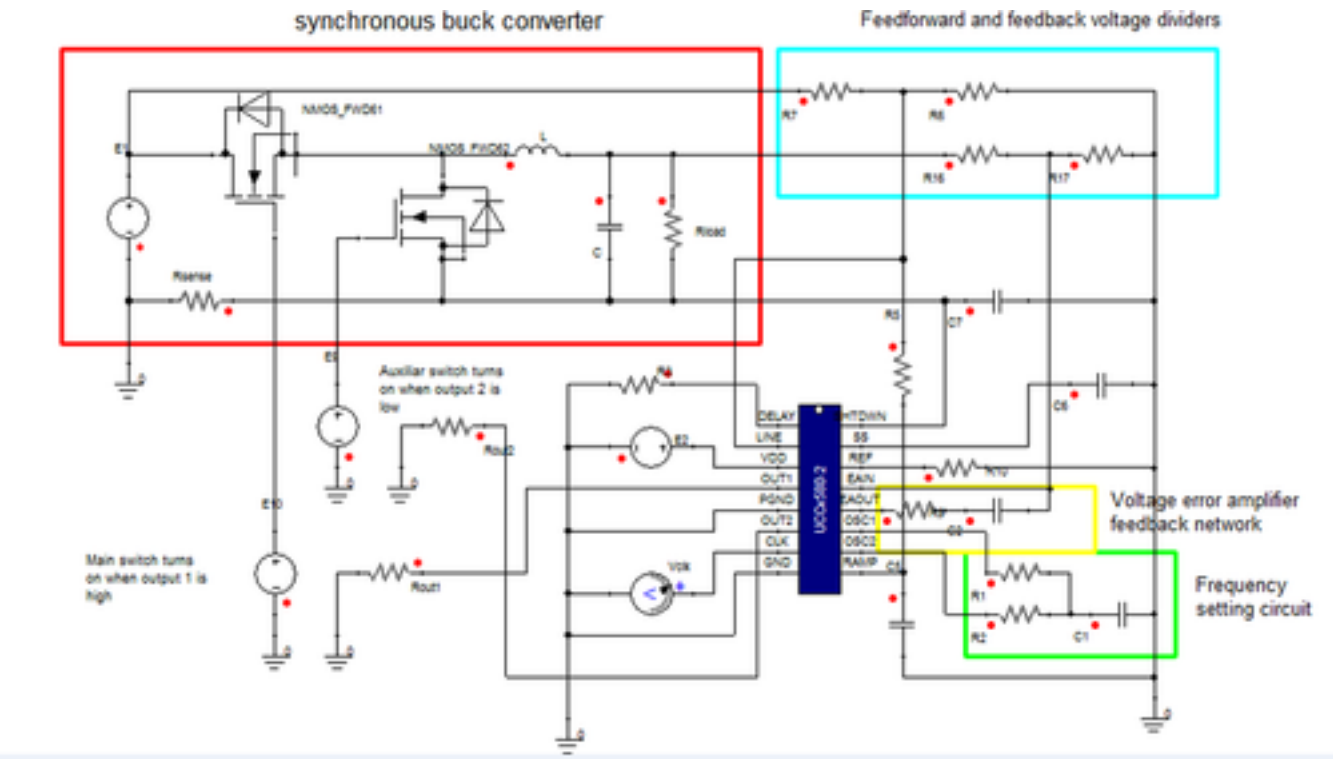

Figure 2. Example Circuit

In this example, the *UCCx580-2* is used to control a synchronous buck converter. In order to focus on the operation of the IC, MOSFETS are driven by dependant voltage sources, this way avoiding the use of a more complex circuitry. When output 1 is high, high side MOSFET is turned on and, as this IC is intended to drive a P-channel transistor with the second channel, when output 2 is low, low side MOSFET is turned on.

Simulation results :

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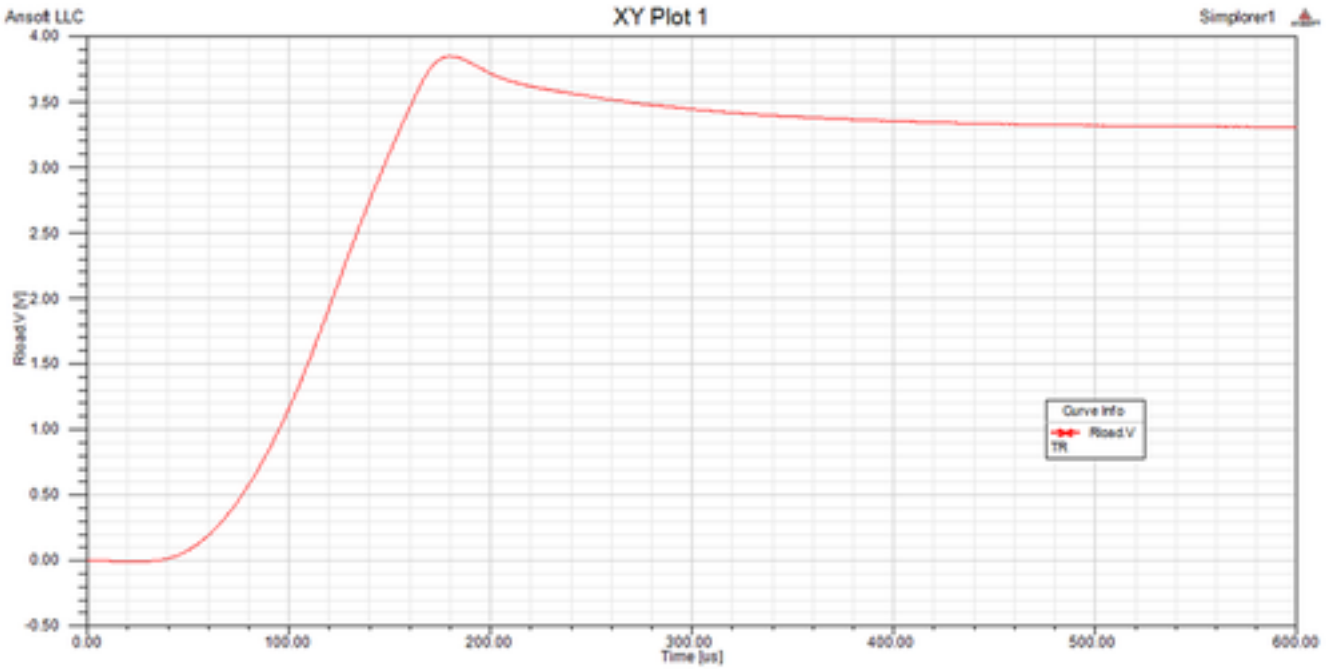
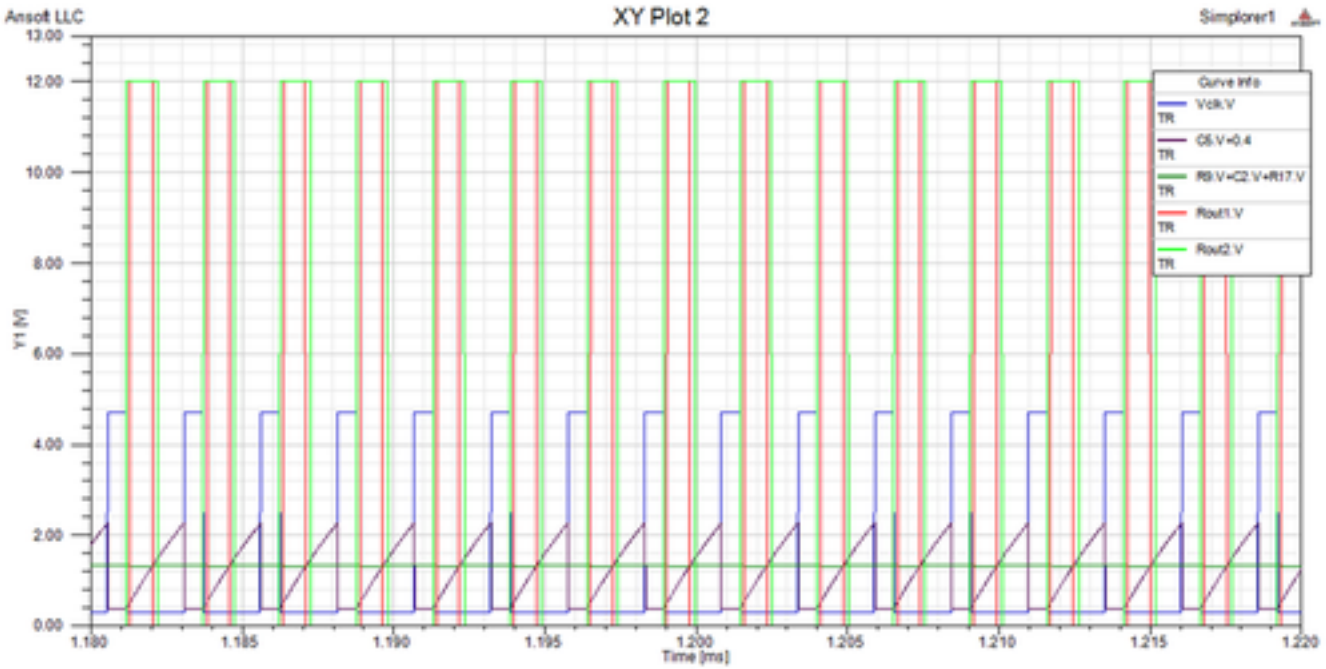


Figure 3. Simulation results(a)

In the diagram above, output voltage is shown. Note that after a transitory time of roughly 0.5ms, output matches the 3.3V regulated value.



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Red: output 1 voltage

Green: output 2 voltage

Blue: clock output

Purple: ramp voltage

Dark green: output of the error amplifier

Figure 4. Simulation results(b)

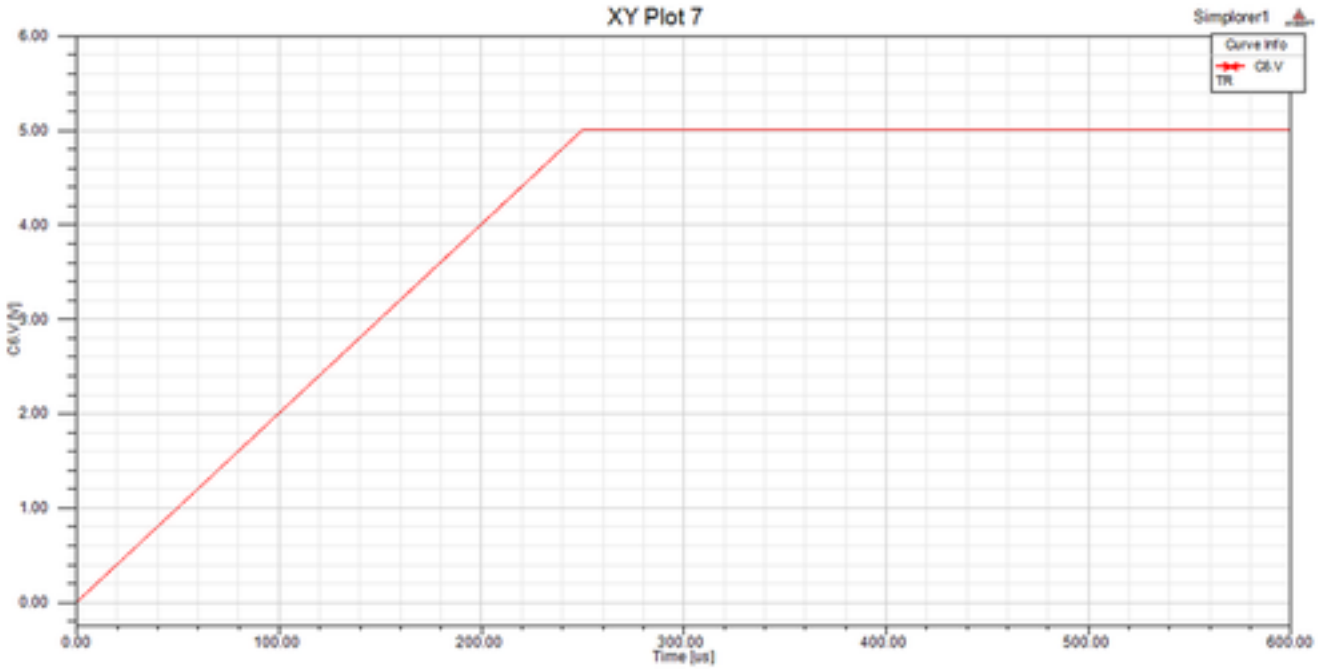

Figure 5. Simulation results(c)

In the figure above we can see the voltage on the soft-start capacitor. The aim of this function is to limit the voltage on the output of the error amplifier during the first moments after starting the device.

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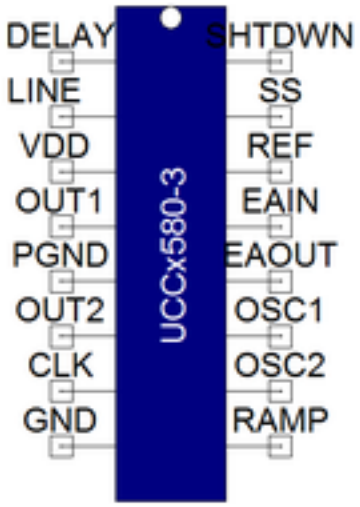
UCCx5803: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCCx580* family of PWM controllers is designed to implement a variety of active clamp/reset and synchronous rectifier switching converter topologies. While containing all the necessary functions for fixed frequency, high performance pulse width modulation, the additional feature of this design is the inclusion of an auxiliary switch driver which complements the main power switch, and with a programmable deadtime or delay between each transition. The active clamp/reset technique allows operation of single ended converters beyond 50% duty cycle while reducing voltage stresses on the switches, and allows a greater flux swing for the power trans-

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former. This approach also allows a reduction in switching losses by recovering energy stored in parasitic elements such as leakage inductance and switch capacitance.

The oscillator is programmed with two resistors and a capacitor to set switching frequency and maximum duty cycle. A separate synchronized ramp provides a voltage feedforward pulse width modulation and a programmed maximum volt-second limit. The generated clock from the oscillator contains both frequency and maximum duty cycle information.

The main gate drive output (OUT1) is controlled by the pulse width modulator. The second output (OUT2) is intended to activate an auxiliary switch during the off time of the main switch, except that between each transition there is deadtime where both switches are off, programmed by a single external resistor. This design offers two options for OUT2, normal and inverted. In the -1 and -2 versions, OUT2 is normal and can be used to drive PMOS FETs. In the -3 and -4 versions, OUT2 is inverted and can be used to drive NMOS FETs. In all versions, both the main and auxiliary switches are held off prior to startup and when the PWM command goes to zero duty cycle. During fault conditions, OUT1 is held off while OUT2 operates at maximum duty cycle with a guaranteed off time equal to the sum of the two deadtimes.

Undervoltage lockout monitors supply voltage (VDD), the precision reference (REF), input line voltage (LINE), and the shutdown comparator (SHTDWN). If after any of these four have sensed a fault condition, recovery to full operation is initiated with a soft start. VDD thresholds, on and off, are 15V and 8.5V for the -2 and -4 versions, 9V and 8.5V for the -1 and -3 versions.

In this model we can differentiate two main parts: the electrical circuit and the logic which manages it.

The circuit consists of (from top left and counterclockwise):
- Oscillator circuitry
- Ramp circuitry
- Error amplifier
- Soft-start circuit
- Shutdown and line inputs
- Ground and power input
- Reference voltage source
- Output circuitry
- Delay setting circuit
- Output clock signal

The logic consists of six state machines. The main state machine, the one located at the bottom right, controls the main operation of the model. It opens and closes the outputs as a function of the ramp voltage, the output of the error amplifier and the programmed delays.

The other state machines control the oscillator, the undervoltage lockout feature, the line pin and the shutdown function.

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Conservative Pins

Table 1

Symbol	Description
DELAY	Delay programming pin.
LINE	Hysteretic comparator pin.
VDD	Chip power supply pin.
OUT1	Gate drive output for the main switch.
PGND	Ground connection for the gate drivers.
OUT2	Gate drive output for the auxiliary switch.
CLK	Oscillator clock output.
GND	Signal ground.
SHTDWN	Comparator input to stop the chip.
SS	Soft-start programming pin.
REF	Precision 5.0V reference pin.
EAIN	Inverting input to the error amplifier.
EAOUT	Output of the error amplifier.
OSC1	Oscillator programming pin (charge).
OSC2	Oscillator programming pin (discharge).
RAMP	Line feedforwardsawtooth signal.

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Parameters

Comparison between model and real component.

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Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx5803			MODEL	UNITS
		MIN	TYP	MAX		
Oscillator Section						
Frequency		370	400	430	395	kHz
CLK Pulse Width		650	750	850	650	ns
CLK V_{OH}	I_{CLK} = 3 mA	4.3	4.7		4.7	V
CLK V_{OL}	I_{CLK}Â = 3 mA		0.3	0.5	0.3	V
Ramp GeneratorSection						
Ramp V_{OL}	I_{RAMP} = 100 µA		50	100	0	mV
Flux Comparator Vth		3.16	3.33	3.50	3.33	V
Pulse WidthModulatorSection						
Minimum DutyCycle	OUT1, EAOUT = VOL			0	0	%
Maximum DutyCycle	OUT1, EAIN = 0 V	63	66	69	69	%
PWM Comparator Offset		0.1	0.4	0.9	0.4	V
Error AmplifierSection						
EAIN	EAOUT = EAIN	2.44	2.5	2.56	2.5	V
I_{EAIN}	EAOUT = EAIN		150	400	0	nA
EAOUT, VOL	EAIN = 2.6 V, I_{EAOUT} = 100 µA		0.3	0.5	0	V
EAOUT, VOH	EAIN = 2.4 V, I_{EAOUT} = 100 µA	4	5	55	5	V
AVOL		70	80		80	dB
Gain Bandwidth Product	f = 100 kHz (Note 1)	2	6		X	MHz

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Softstart/ShutdownSection						
Start DutyCycle	EAIN = 2.4 V		0		0	%
SS V_{OL}	I_{SS} = 100 µA		100	350	0	mV
SS Restart Threshold			400	550	300	mV
I_{SS}			-20	-35	-20	µA
SHTDWN V_{TH}		0.4	0.5	0.6	0.5	V
I_{SHTDWN}			50	150	0	nA
Undervoltage Lockout Section						
VDD On		8	9	10	9	V
VDD Off		7.5	8.5	9.5	8.5	V
LINE On		4.7	5	5.3	5	V
LINE Off		4.2	4.5	4.8	4.5	V
I_{LINE}	LINE = 6 V		50	150	0	nA
Supply Section						
VDD Clamp	I_{VDD} = 10 mA	14	15	16	15	V
I_{VDD} Start	VDD < VDD On		160	250	0	µA
I_{VDD} Operating	No Load		2.5	3.5	0	mA
Output Drivers Section						
OUT1 V_{SAT} High	I_{OUT1} = 50 mA		0.4	1.0	X	V
OUT1 V_{SAT} Low	I_{OUT1} =100 mA		0.4	1.0	X	V
OUT2 V_{SAT} High	I_{OUT2} = 30 mA		0.4	1.0	X	V
OUT2 V_{SAT} Low	$I_{OUT2Â}$ = 30 mA		0.4	1.0	X	V
OUT1 Fall Time	C_{OUT1} = 1nF, R_S = 3		20	50	0	ns
OUT1 Rise Time	$C_{OUT1Â}$ = 1nF, R_S = 3		40	80	0	ns
OUT2 Fall Time	C_{OUT2} = 300pF, R_S = 10		20	50	0	ns
OUT2 Rise	C_{OUT2} =		20	40	0	ns

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Time	300pF, R_S = 10					
Delay 1 OUT2 to OUT1	R3 = 100 k , COUT1 = COUT2 = 15 pF	90	120	160	115	ns
	TA = TJ = 25°C	100	120	140	115	ns
Delay 2 OUT1 to OUT2	R3 = 100 k , COUT1 = COUT2 = 15 pF	110	170	250	167	ns
	TA = TJ = 25°C	140	170	200	167	ns
Reference Section						
REF	I_{REF} = 0	4.87	5	5.12	5	V
Load Regulation	I_{REF} = 0 mAto 1 mA		1	20	0	mV
Line Regulation	VDD = 10 V to 14 V		1	20	0	mV

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Example circuit :

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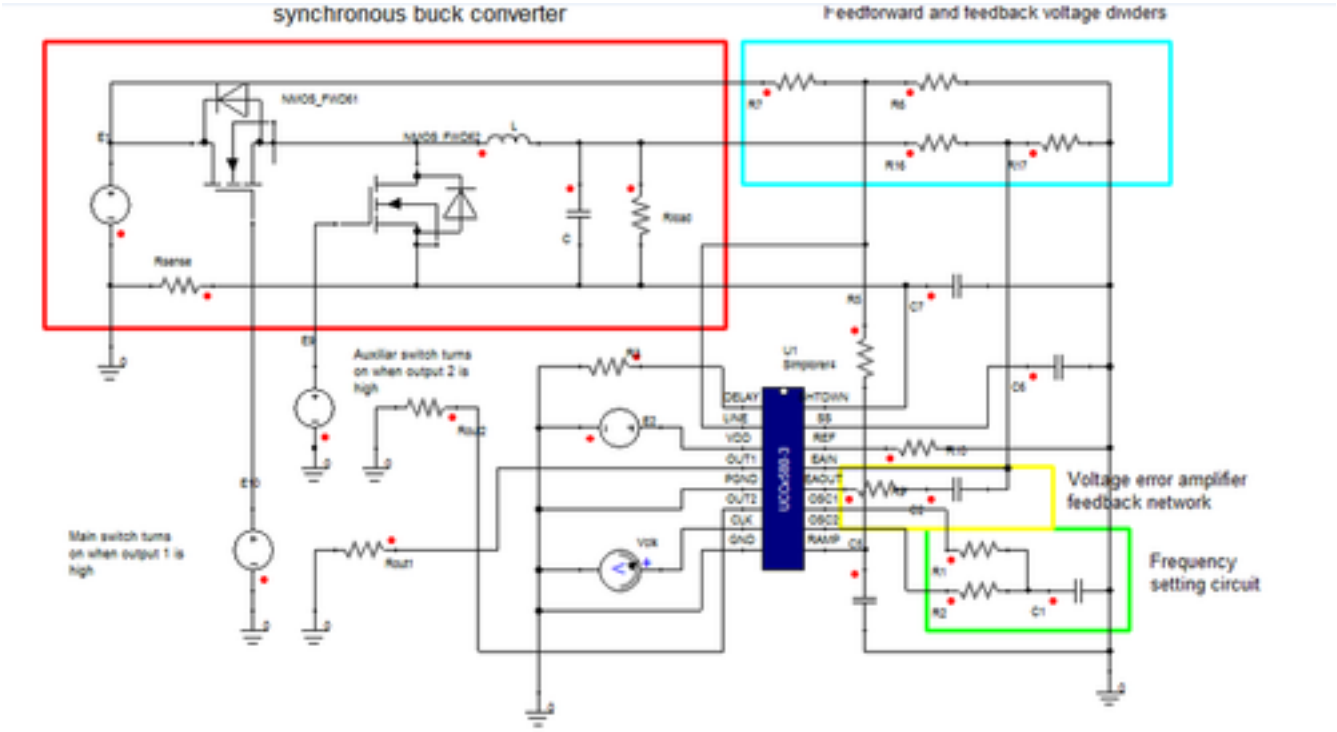

Figure 2. Example Circuit

In this example, the *UCCx580-3* is used to control a synchronous buck converter. In order to focus on the operation of the IC, MOSFETS are driven by dependant voltage sources, this way avoiding the use of a more complex circuitry. When output 1 is high, high side MOSFET is turned on and, as this IC is intended to drive a N-channel transistor with the second channel, when output 2 is high, low side MOSFET is turned on.

Simulation results :

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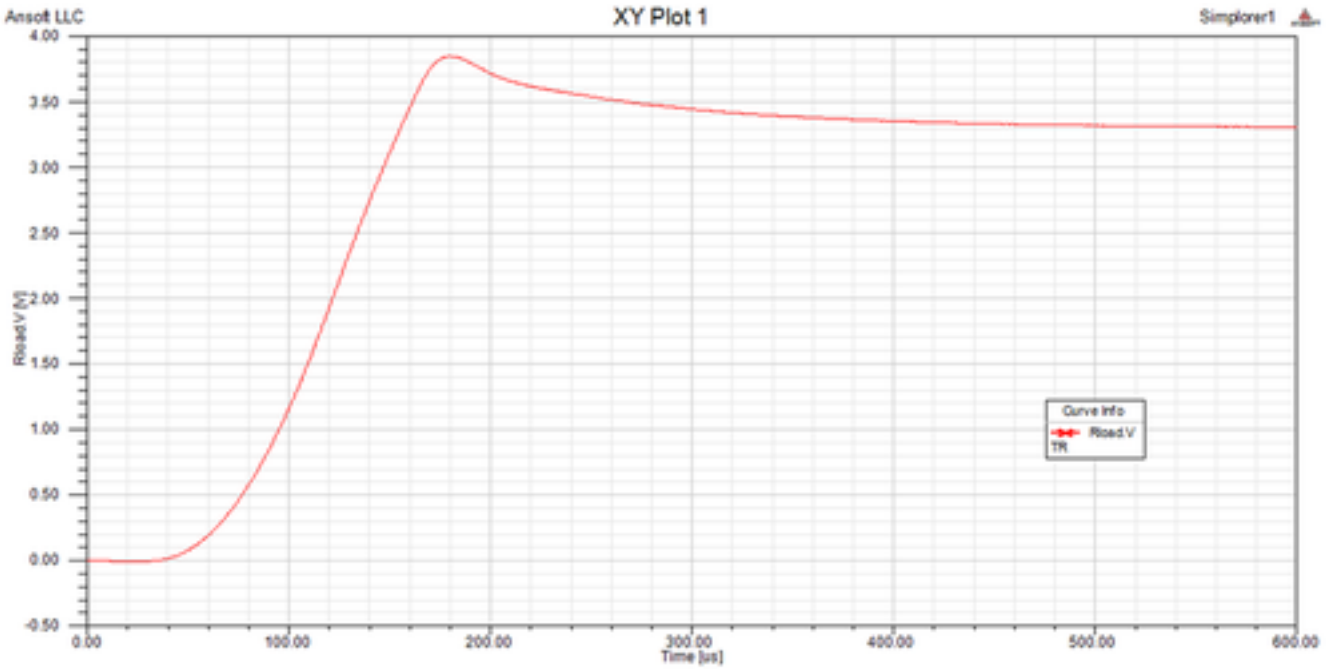
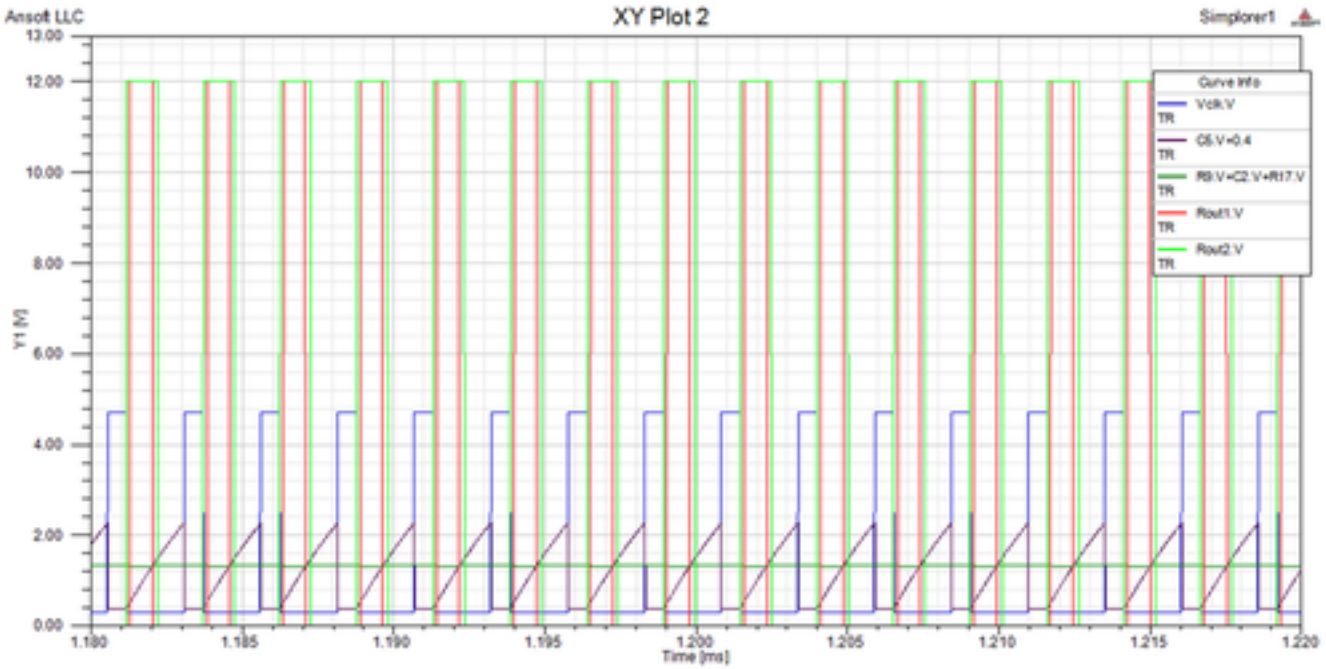


Figure 3. Simulation results(a)

In the diagram above, output voltage is shown. Note that after a transitory time of roughly 0.5ms, output matches the 3.3V regulated value.



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Red: output 1 voltage

Green: output 2 voltage

Blue: clock output

Purple: ramp voltage

Dark green: output of the error amplifier

Figure 4. Simulation results(b)

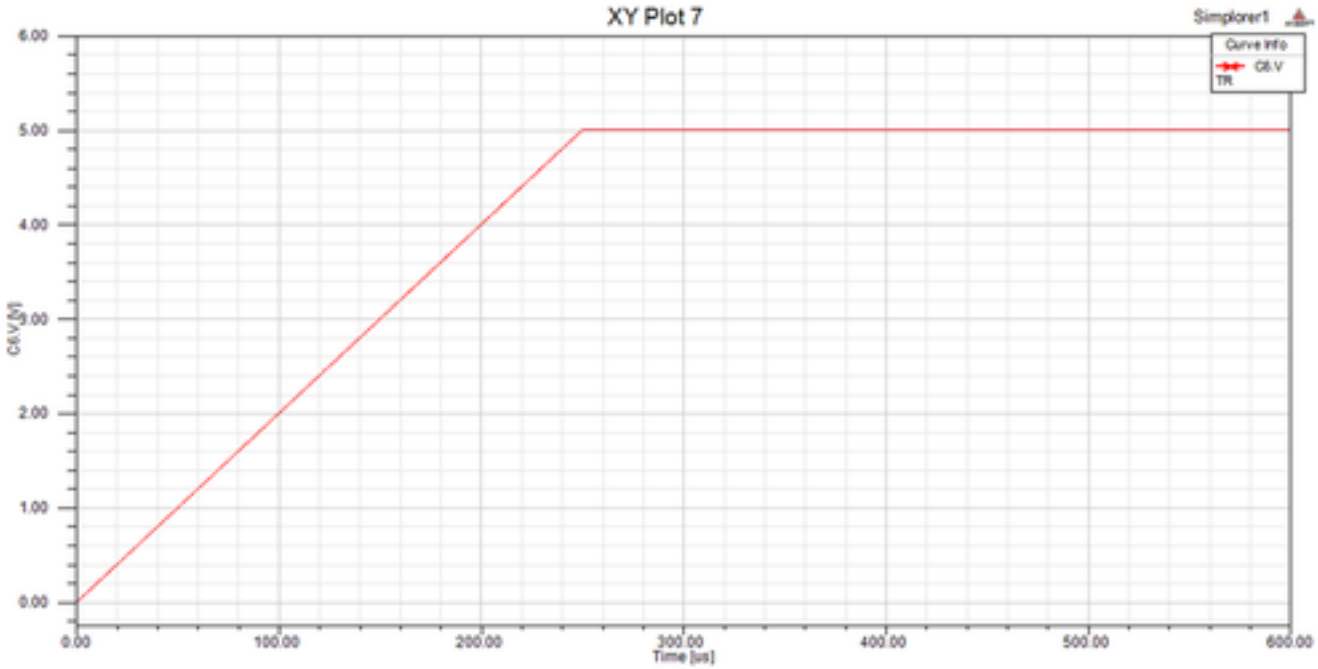

Figure 5. Simulation results(c)

In the figure above we can see the voltage on the soft-start capacitor. The aim of this function is to limit the voltage on the output of the error amplifier during the first moments after starting the device.

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UCCx5804: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

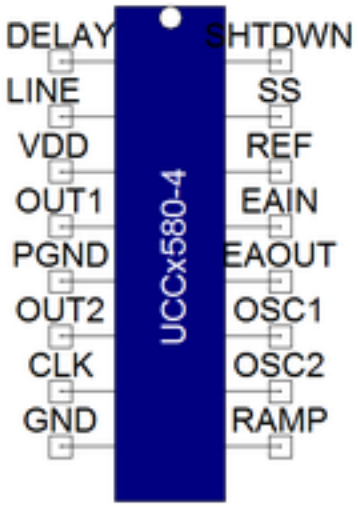

Figure 1. Component symbol

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Description

The *UCCx580* family of PWM controllers is designed to implement a variety of active clamp/reset and synchronous rectifier switching converter topologies. While containing all the necessary functions for fixed frequency, high performance pulse width modulation, the additional feature of this design is the inclusion of an auxiliary switch driver which complements the main power switch, and with a programmable deadtime or delay between each transition. The active clamp/reset technique allows operation of single ended converters beyond 50% duty cycle while reducing voltage stresses on the switches, and allows a greater flux swing for the power trans-

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former. This approach also allows a reduction in switching losses by recovering energy stored in parasitic elements such as leakage inductance and switch capacitance.

The oscillator is programmed with two resistors and a capacitor to set switching frequency and maximum duty cycle. A separate synchronized ramp provides a voltage feedforward pulse width modulation and a programmed maximum volt-second limit. The generated clock from the oscillator contains both frequency and maximum duty cycle information.

The main gate drive output (OUT1) is controlled by the pulse width modulator. The second output (OUT2) is intended to activate an auxiliary switch during the off time of the main switch, except that between each transition there is deadtime where both switches are off, programmed by a single external resistor. This design offers two options for OUT2, normal and inverted. In the -1 and -2 versions, OUT2 is normal and can be used to drive PMOS FETs. In the -3 and -4 versions, OUT2 is inverted and can be used to drive NMOS FETs. In all versions, both the main and auxiliary switches are held off prior to startup and when the PWM command goes to zero duty cycle. During fault conditions, OUT1 is held off while OUT2 operates at maximum duty cycle with a guaranteed off time equal to the sum of the two deadtimes.

Undervoltage lockout monitors supply voltage (VDD), the precision reference (REF), input line voltage (LINE), and the shutdown comparator (SHTDWN). If after any of these four have sensed a fault condition, recovery to full operation is initiated with a soft start. VDD thresholds, on and off, are 15V and 8.5V for the -2 and -4 versions, 9V and 8.5V for the -1 and -3 versions.

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The circuit consists of (from top left and counterclockwise):
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- Ramp circuitry
- Error amplifier
- Soft-start circuit
- Shutdown and line inputs
- Ground and power input
- Reference voltage source
- Output circuitry
- Delay setting circuit
- Output clock signal

The logic consists of six state machines. The main state machine, the one located at the bottom right, controls the main operation of the model. It opens and closes the outputs as a function of the ramp voltage, the output of the error amplifier and the programmed delays.

The other state machines control the oscillator, the undervoltage lockout feature, the line pin and the shutdown function.

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Conservative Pins

Table 1

Symbol	Description
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VDD	Chip power supply pin.
OUT1	Gate drive output for the main switch.
PGND	Ground connection for the gate drivers.
OUT2	Gate drive output for the auxiliary switch.
CLK	Oscillator clock output.
GND	Signal ground.
SHTDWN	Comparator input to stop the chip.
SS	Soft-start programming pin.
REF	Precision 5.0V reference pin.
EAIN	Inverting input to the error amplifier.
EAOUT	Output of the error amplifier.
OSC1	Oscillator programming pin (charge).
OSC2	Oscillator programming pin (discharge).
RAMP	Line feedforwardsawtooth signal.

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Comparison between model and real component.

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Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx5804			MODEL	UNITS
		MIN	TYP	MAX		
Oscillator Section						
Frequency		370	400	430	395	kHz
CLK Pulse Width		650	750	850	650	ns
CLK V_{OH}	I_{CLK} = 3 mA	4.3	4.7		4.7	V
CLK V_{OL}	I_{CLK}Â = 3 mA		0.3	0.5	0.3	V
Ramp GeneratorSection						
Ramp V_{OL}	I_{RAMP} = 100 µA		50	100	0	mV
Flux Comparator Vth		3.16	3.33	3.50	3.33	V
Pulse WidthModulatorSection						
Minimum DutyCycle	OUT1, EAOUT = VOL			0	0	%
Maximum DutyCycle	OUT1, EAIN = 0 V	63	66	69	69	%
PWM Comparator Offset		0.1	0.4	0.9	0.4	V
Error AmplifierSection						
EAIN	EAOUT = EAIN	2.44	2.5	2.56	2.5	V
I_{EAIN}	EAOUT = EAIN		150	400	0	nA
EAOUT, VOL	EAIN = 2.6 V, I_{EAOUT} = 100 µA		0.3	0.5	0	V
EAOUT, VOH	EAIN = 2.4 V, I_{EAOUT} = 100 µA	4	5	55	5	V
AVOL		70	80		80	dB
Gain Bandwidth Product	f = 100 kHz (Note 1)	2	6		X	MHz

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Softstart/ShutdownSection						
Start DutyCycle	EAIN = 2.4 V		0		0	%
SS V_{OL}	I_{SS} = 100 µA		100	350	0	mV
SS Restart Threshold			400	550	300	mV
I_{SS}			-20	-35	-20	µA
SHTDWN V_{TH}		0.4	0.5	0.6	0.5	V
I_{SHTDWN}			50	150	0	nA
Undervoltage Lockout Section						
VDD On		14	15	16	15	V
VDD Off		7.5	8.5	9.5	8.5	V
LINE On		4.7	5	5.3	5	V
LINE Off		4.2	4.5	4.8	4.5	V
I_{LINE}	LINE = 6 V		50	150	0	nA
Supply Section						
VDD Clamp	I_{VDD} = 10 mA	14	15	16	15	V
I_{VDD} Start	VDD < VDD On		160	250	0	µA
I_{VDD} Operating	No Load		2.5	3.5	0	mA
Output Drivers Section						
OUT1 V_{SAT} High	I_{OUT1} = 50 mA		0.4	1.0	X	V
OUT1 V_{SAT} Low	I_{OUT1} =100 mA		0.4	1.0	X	V
OUT2 V_{SAT} High	I_{OUT2} = 30 mA		0.4	1.0	X	V
OUT2 V_{SAT} Low	$I_{OUT2Â}$ = 30 mA		0.4	1.0	X	V
OUT1 Fall Time	C_{OUT1} = 1nF, R_S = 3		20	50	0	ns
OUT1 Rise Time	$C_{OUT1Â}$ = 1nF, R_S = 3		40	80	0	ns
OUT2 Fall Time	C_{OUT2} = 300pF, R_S = 10		20	50	0	ns

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OUT2 Rise Time	C_{OUT2} = 300pF, R_S = 10		20	40	0	ns
Delay 1 OUT2 to OUT1	R3 = 100 k , COUT1 = COUT2 = 15 pF	90	120	160	115	ns
	TA = TJ = 25°C	100	120	140	115	ns
Delay 2 OUT1 to OUT2	R3 = 100 k , COUT1 = COUT2 = 15 pF	110	170	250	167	ns
	TA = TJ = 25°C	140	170	200	167	ns
Reference Section						
REF	I_{REF} = 0	4.87	5	5.12	5	V
Load Regu-lation	I_{REF} = 0 mAto 1 mA		1	20	0	mV
Line Regu-lation	VDD = 10 V to 14 V		1	20	0	mV

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Example circuit :

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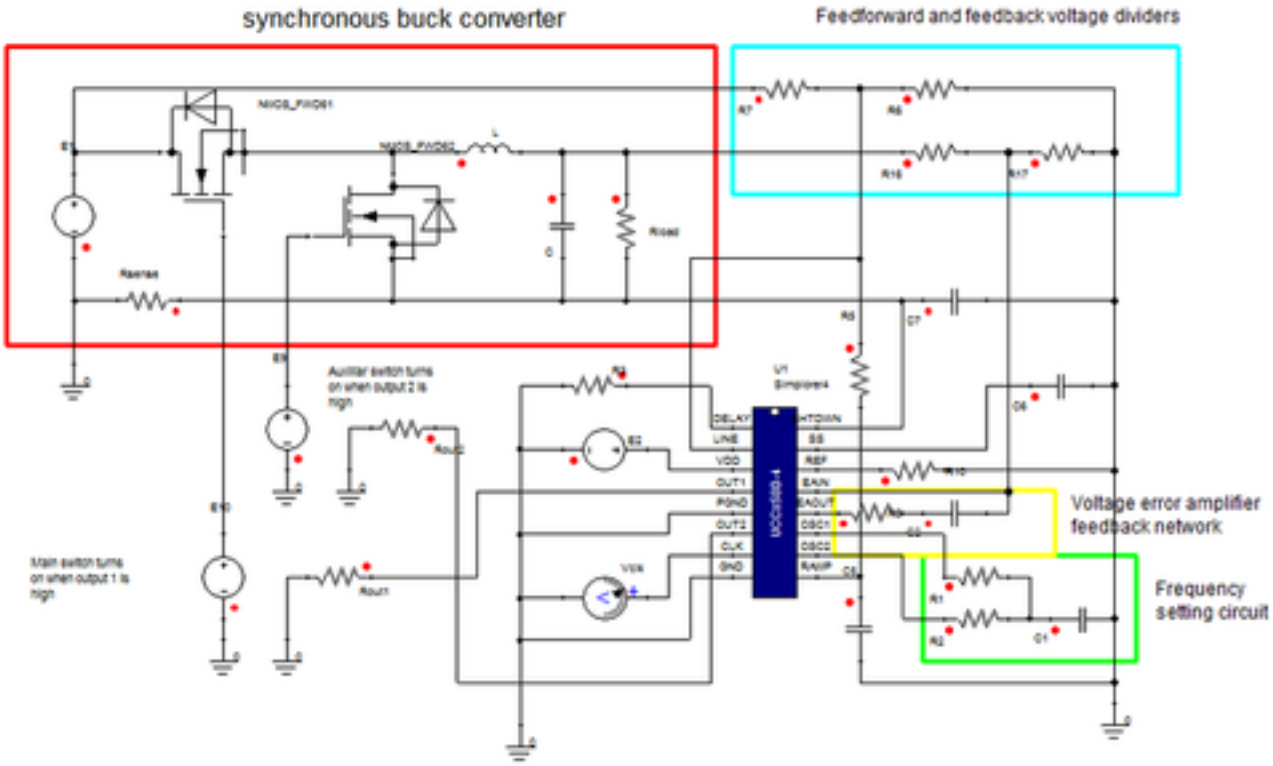

Figure 2. Example Circuit

In this example, the *UCCx580-4* is used to control a synchronous buck converter. In order to focus on the operation of the IC, MOSFETS are driven by dependant voltage sources, this way avoiding the use of a more complex circuitry. When output 1 is high, high side MOSFET is turned on and, as this IC is intended to drive a N-channel transistor with the second channel, when output 2 is high, low side MOSFET is turned on.

Simulation results :

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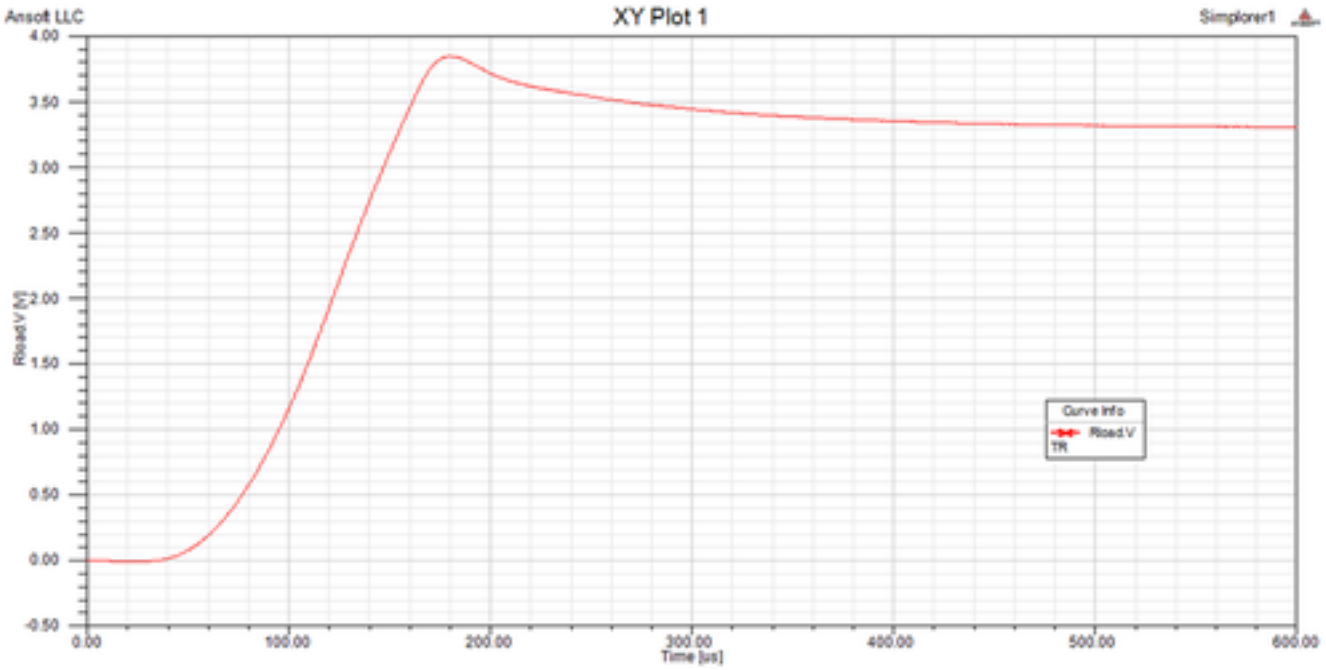
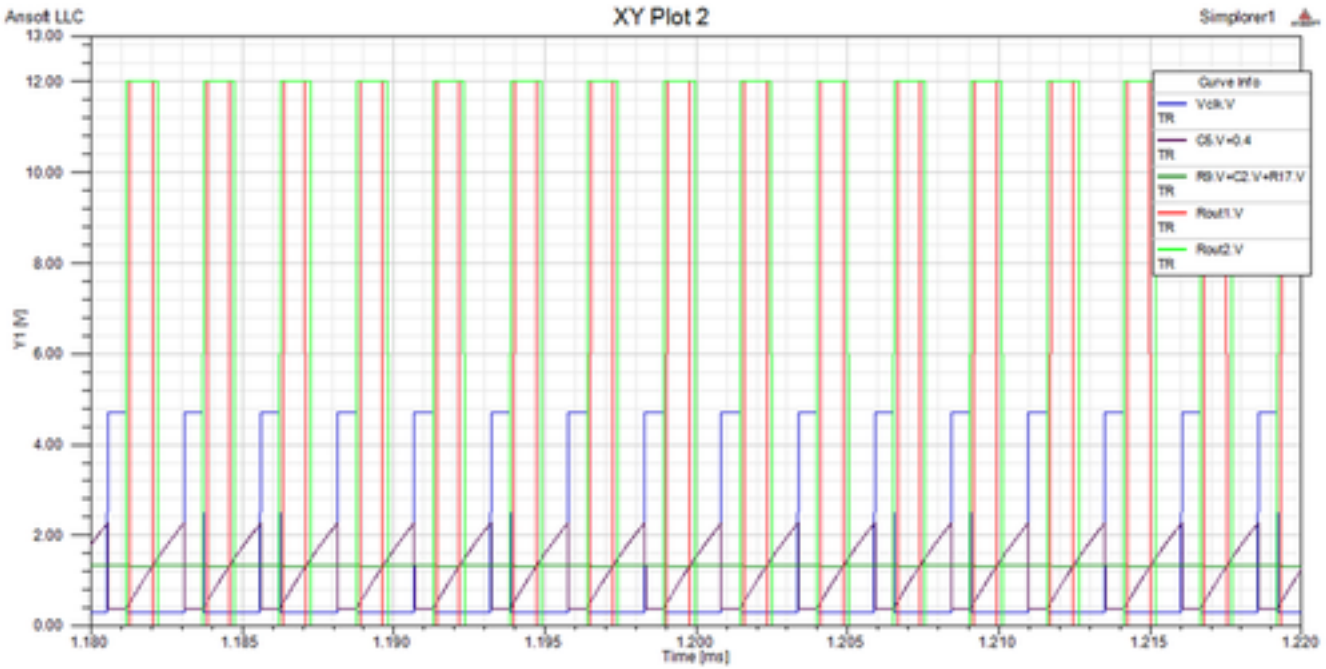


Figure 3. Simulation results(a)

In the diagram above, output voltage is shown. Note that after a transitory time of roughly 0.5ms, output matches the 3.3V regulated value.



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Red: output 1 voltage

Green: output 2 voltage

Blue: clock output

Purple: ramp voltage

Dark green: output of the error amplifier

Figure 4. Simulation results(b)

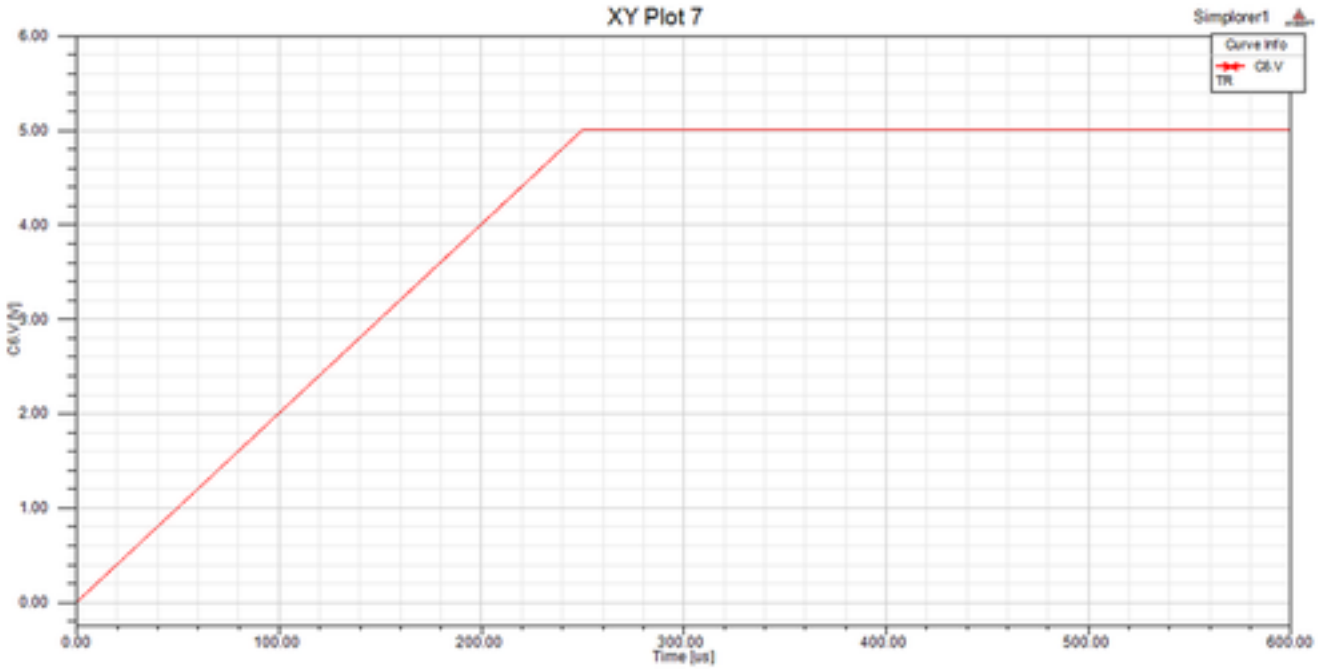

Figure 5. Simulation results(c)

In the figure above we can see the voltage on the soft-start capacitor. The aim of this function is to limit the voltage on the output of the error amplifier during the first moments after starting the device.

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UCCx800: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

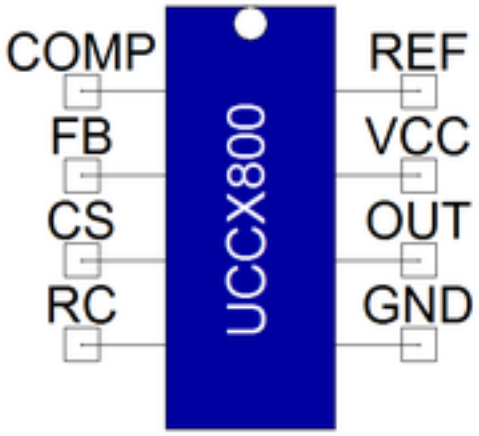

Figure 1. Component symbol

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Description

The *UCCX800/1/2/3/4/5* provides a Pulse Width Modulated (PWM) signal (*UCCX803/5* with a maximum duty cycle of 50%) and current-mode control.

The switching frequency is set by a resistor and a capacitor connected to the RC pin, which forms a RC oscillator circuit with a "saw-tooth" output waveform.

The output voltage rises up at every oscillator peak and when the CS pin voltage reaches the output comparator voltage the output falls.

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The *UCCX801/2/3/4/5* has a soft start circuit that limits the output duty cycle when it initializes. It also has an over current sensor that triggers a soft start cycle when an over current is detected.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output, FB pin is connected to the inverting input and NI to the non-inverting one.
• Current sense: a voltmeter measures the CS pin voltage.
• Oscillator: Its period depends on the resistance and the capacitor connected to RC pin.
• Soft-start: this circuit limits the maximum voltage that the error amplifier can supply during the first cycles after a restart.
• Reference voltage: provides a 5V voltage reference with variable output impedance.
• Output: controlled by a state machine. Its output impedance is variable.

The state machines control the under-voltage protection (when the input voltage falls below 6.9V, the protection activates and the outputs fall to zero), the oscillator, the output voltage and the shutdown function.

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Table 1

Name	Description
1. COMP	Output of the error amplifier
2. FB	Inversing input of the error amplifier
3. CS	Current sense
4. RC	Oscillator
5. GND	Power and reference ground
6. OUT	PWM Output
7. VCC	Power input
8. REF	Reference Voltage

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -55°C ≤TA ≤+125°C for UCC180x; -40°C ≤TA ≤+85°C for UCC280x; 0°C ≤TA ≤+70°C for *UCC380x*; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1 F capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

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Table 2

PARAMETER	TEST CONDITIONS	UCCX80X	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
	T_J=+25°C, I=0.2mA, UCCx803/5	4.00	4.00	
Load Regulation	0.2mA<I<5mA	10-30	25	
Line Regulation	T_J=+25°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	1.9	2.0	mV/V
	T_J=-55°C to +125°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	2.5	2.0	mV/V
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
	UCCx803/5 (Note 7)	4.00	4.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz, T_J=+25°C (Note 9)	130	X	V
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	X	mV
Output Short Circuit		-5 / -35	-35	mA
Oscillator Section				
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	46	46	kHz
	UCCx803/5 (Note 4)	31	33	kHz
Temperature Stability	(Note 9)	2.5	X	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.45	V
Error Amplifier Section				

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Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.5	2.5	V
	COMP=2.0V; UCCx803/5	2.0	2.0	V
Input Bias Current		0	X	V
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle	UCCx800/2/3	99	100	%
	UCCx801/4/5	49	50	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0.1	V
	I=200mA, allparts	0.35	0.1	V
	I=50mA, VCC-C=5V, UCCx803/5	0.15	0.1	V
	I=20mA, VCC-C=0V, all parts	0.7	0.7	V

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OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0.1	V
	I=-200mA, allparts	1.0	1.0	V
	I=-50mA,VCC-C=5V, UCCx803/5	0.4	0.6	V
Rise Time	CL=1nF	41	41	ns
Fall Time	CL=1nF	44	41	ns
Undervoltage Lockout Section				
Start Threshold (Note 8)	UCCx800	7.2	7.2	V
	UCCx801	9.4	9.4	V
	UCCx802/4	12.5	12.5	V
	UCCx803/5	4.1	4.1	V
Stop Threshold (Note 8)	UCCx800	6.9	6.9	V
	UCCx801	7.4	7.4	V
	UCCx802/4	8.3	8.3	V
	UCCx803/5	3.6	3.6	V
Start to Stop Hysteresis	UCCx800	0.3	0.3	V
	UCCx801	2	2	V
	UCCx802/4	4.2	4.2	V
	UCCx803/5	0.5	0.5	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0.5	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start	CS=0V	1.0	1.0	V

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Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency. Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.
Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤Vcs ≤0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.
Note 10: The device is fully operating in clamp mode as the forcing current is higher than the normal operating supply current.

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Example circuit :

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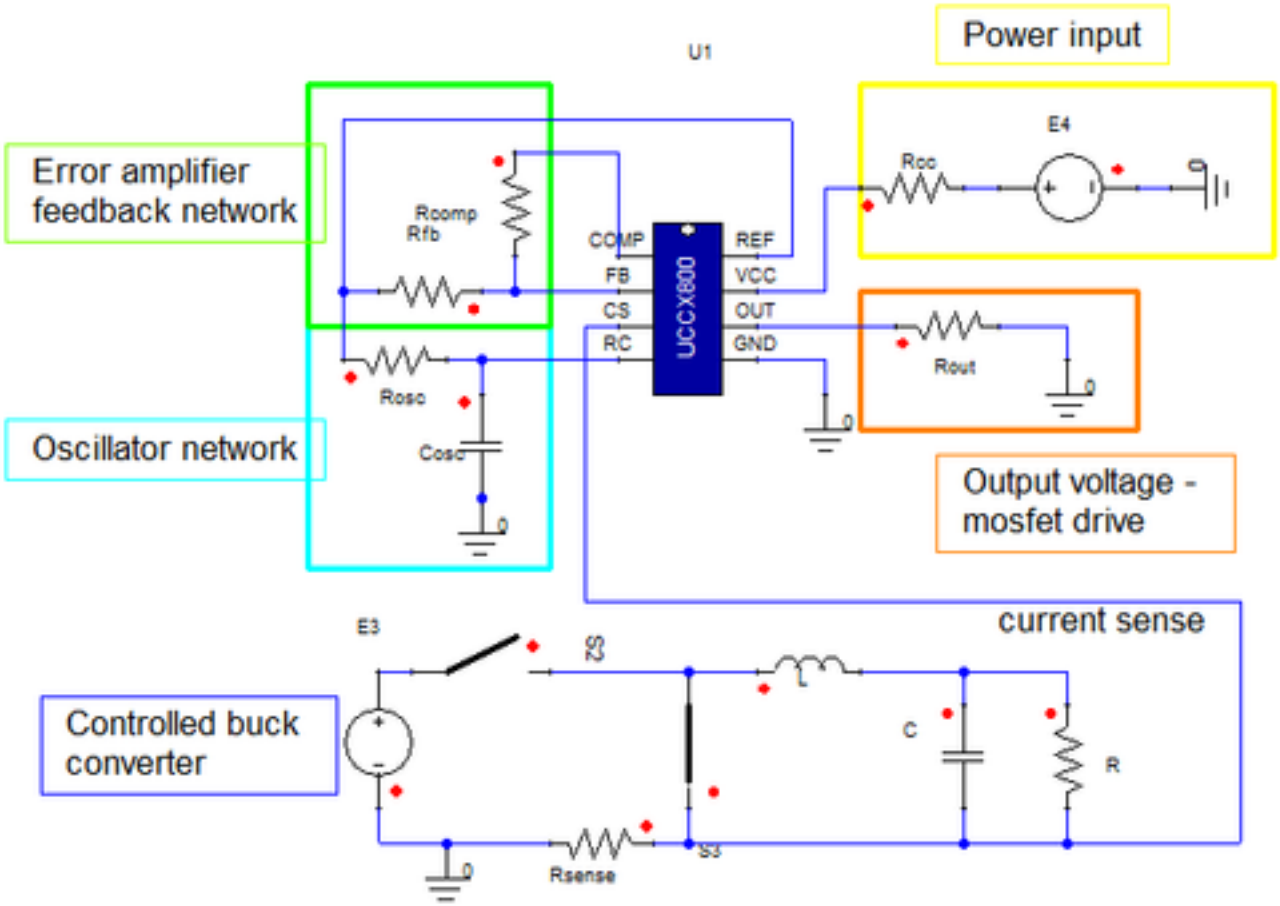

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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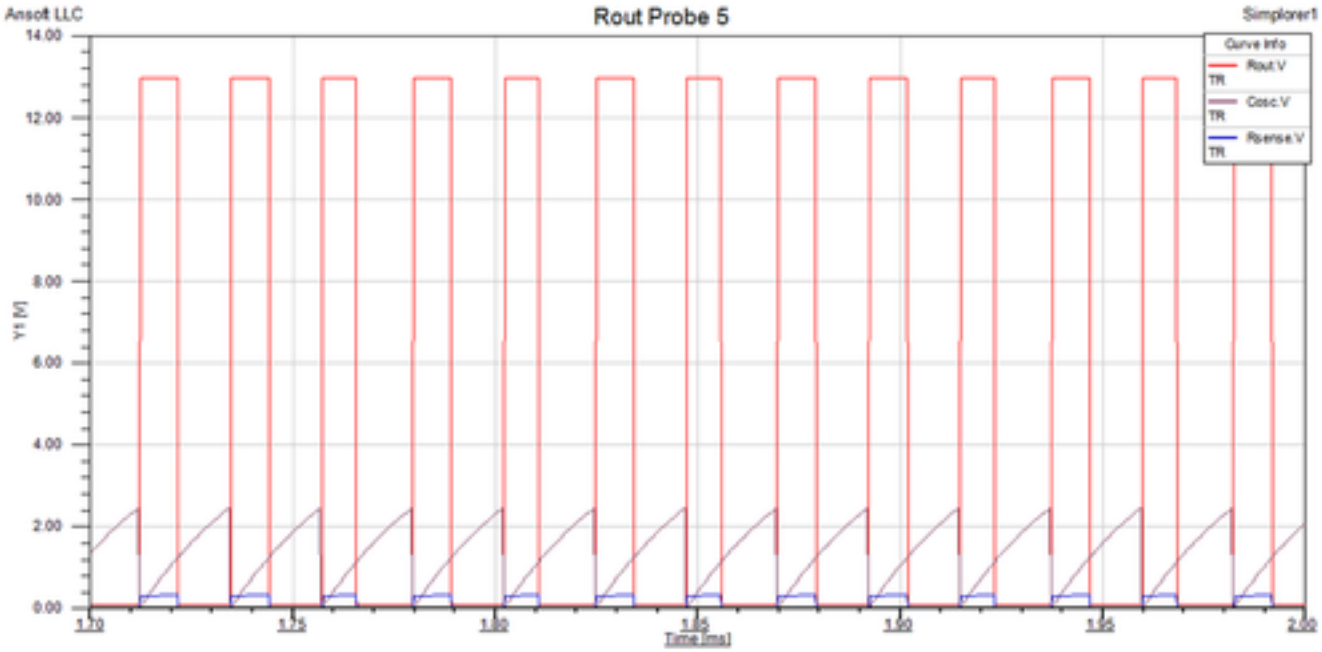
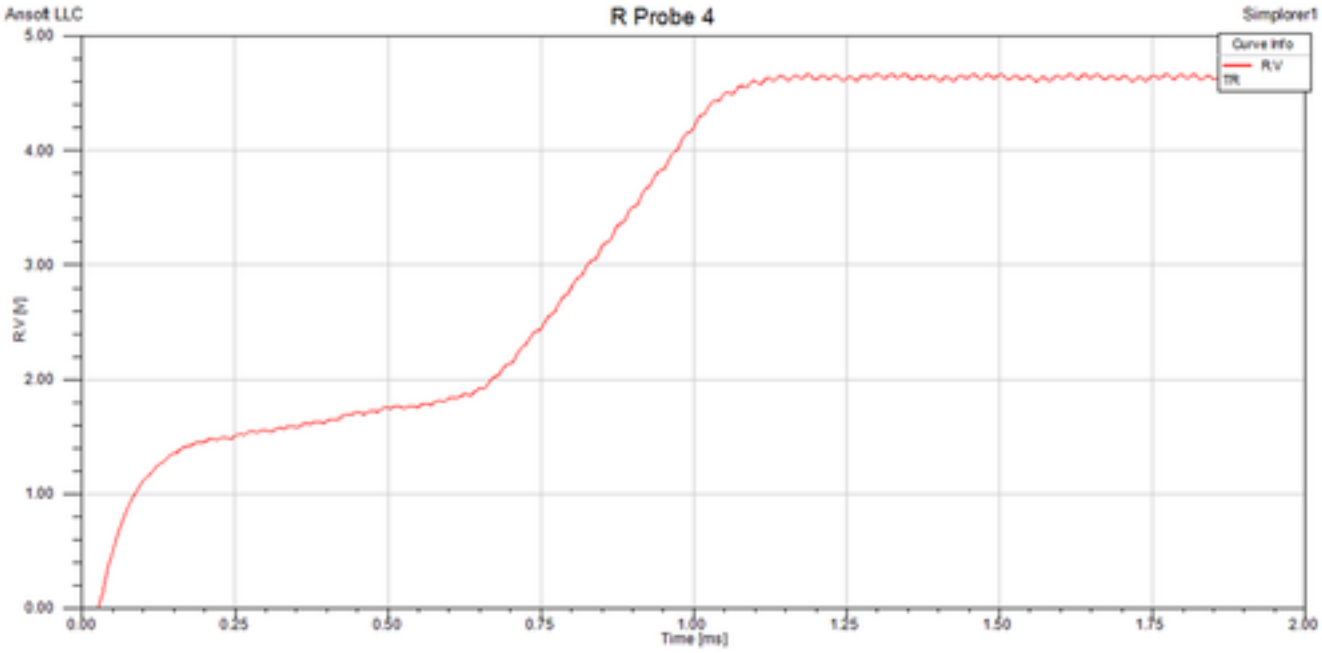


Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)



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Red: converter output voltage.

Figure 4. Simulation results(b)

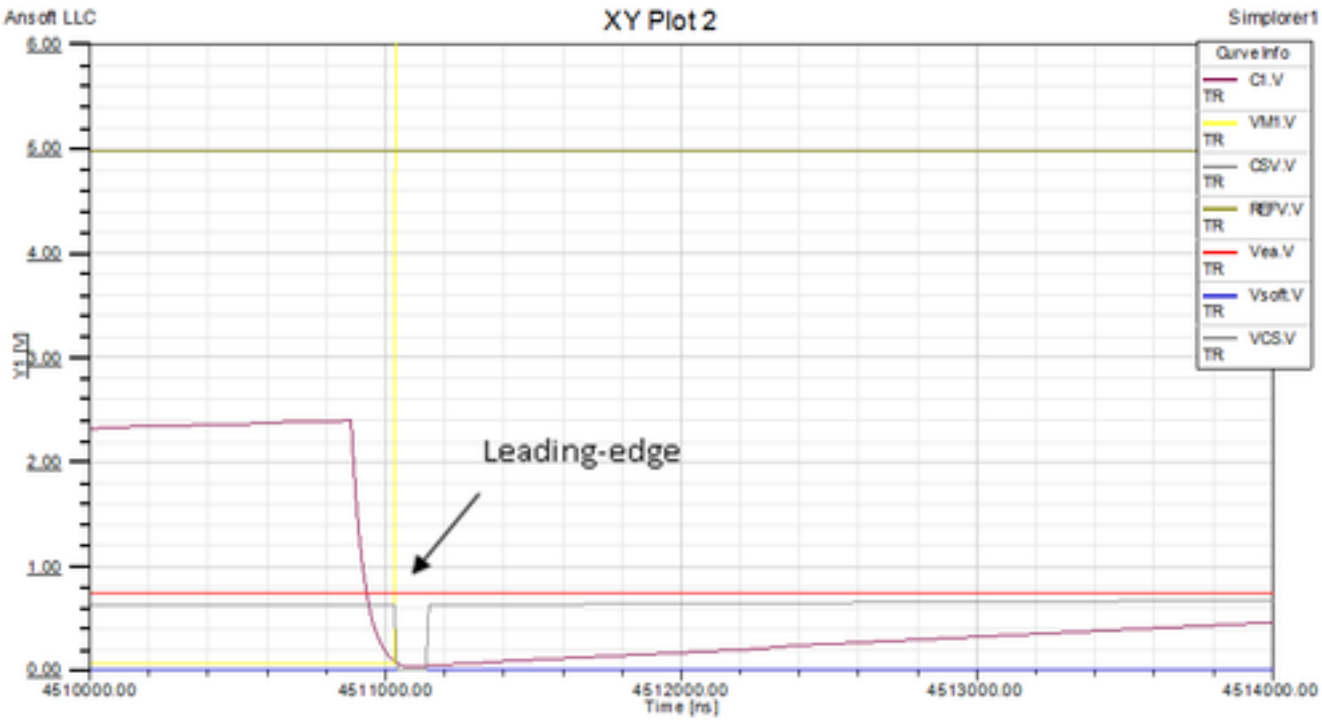

Figure 5. Simulation results(c)

The leading-edge blanking circuit acts like a filter, disconnecting the CS pin from the current sensor during the 100ns following a rising edge of the output voltage.

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UCCx801: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

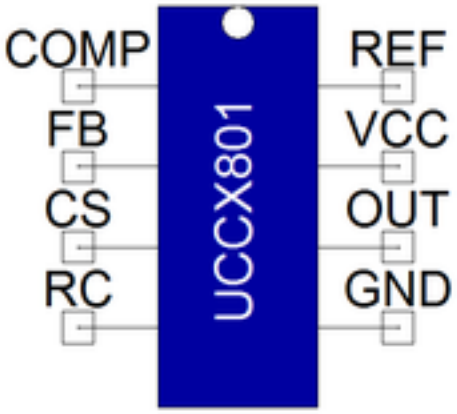

Figure 1. Component symbol

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Description

The *UCCX800/1/2/3/4/5* provides a Pulse Width Modulated (PWM) signal (*UCCX803/5* with a maximum duty cycle of 50%) and current-mode control.

The switching frequency is set by a resistor and a capacitor connected to the RC pin, which forms a RC oscillator circuit with a "saw-tooth" output waveform.

The output voltage rises up at every oscillator peak and when the CS pin voltage reaches the output comparator voltage the output falls.

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The *UCCX801/2/3/4/5* has a soft start circuit that limits the output duty cycle when it initializes. It also has an over current sensor that triggers a soft start cycle when an over current is detected.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output, FB pin is connected to the inverting input and NI to the non-inverting one.
• Current sense: a voltmeter measures the CS pin voltage.
• Oscillator: Its period depends on the resistance and the capacitor connected to RC pin.
• Soft-start: this circuit limits the maximum voltage that the error amplifier can supply during the first cycles after a restart.
• Reference voltage: provides a 5V voltage reference with variable output impedance.
• Output: controlled by a state machine. Its output impedance is variable.

The state machines control the under-voltage protection (when the input voltage falls below 7.4V, the protection activates and the outputs fall to zero), the oscillator, the output voltage and the shutdown function.

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Table 1

Name	Description
1. COMP	Output of the error amplifier
2. FB	Inversing input of the error amplifier
3. CS	Current sense
4. RC	Oscillator
5. GND	Power and reference ground
6. OUT	PWM Output
7. VCC	Power input
8. REF	Reference Voltage

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -55°C ≤TA ≤+125°C for UCC180x; -40°C ≤TA ≤+85°C for UCC280x; 0°C ≤TA ≤+70°C for *UCC380x*; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1 F capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

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Table 2

PARAMETER	TEST CONDITIONS	UCCX80X	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
	T_J=+25°C, I=0.2mA, UCCx803/5	4.00	4.00	
Load Regulation	0.2mA<I<5mA	10-30	25	
Line Regulation	T_J=+25°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	1.9	2.0	mV/V
	T_J=-55°C to +125°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	2.5	2.0	mV/V
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
	UCCx803/5 (Note 7)	4.00	4.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz, T_J=+25°C (Note 9)	130	X	V
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	X	mV
Output Short Circuit		-5 / -35	-35	mA
Oscillator Section				
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	46	46	kHz
	UCCx803/5 (Note 4)	31	33	kHz
Temperature Stability	(Note 9)	2.5	X	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.45	V
Error Amplifier Section				

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Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.5	2.5	V
	COMP=2.0V; UCCx803/5	2.0	2.0	V
Input Bias Current		0	X	V
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle	UCCx800/2/3	99	100	%
	UCCx801/4/5	49	50	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0.1	V
	I=200mA, allparts	0.35	0.1	V
	I=50mA, VCC-C=5V, UCCx803/5	0.15	0.1	V
	I=20mA, VCC-C=0V, all parts	0.7	0.7	V

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OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0.1	V
	I=-200mA, allparts	1.0	1.0	V
	I=-50mA,VCC-C=5V, UCCx803/5	0.4	0.6	V
Rise Time	CL=1nF	41	41	ns
Fall Time	CL=1nF	44	41	ns
Undervoltage Lockout Section				
Start Threshold (Note 8)	UCCx800	7.2	7.2	V
	UCCx801	9.4	9.4	V
	UCCx802/4	12.5	12.5	V
	UCCx803/5	4.1	4.1	V
Stop Threshold (Note 8)	UCCx800	6.9	6.9	V
	UCCx801	7.4	7.4	V
	UCCx802/4	8.3	8.3	V
	UCCx803/5	3.6	3.6	V
Start to Stop Hysteresis	UCCx800	0.3	0.3	V
	UCCx801	2	2	V
	UCCx802/4	4.2	4.2	V
	UCCx803/5	0.5	0.5	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0.5	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start	CS=0V	1.0	1.0	V

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Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency. Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.
Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤Vcs ≤0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.
Note 10: The device is fully operating in clamp mode as the forcing current is higher than the normal operating supply current.

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Example circuit :

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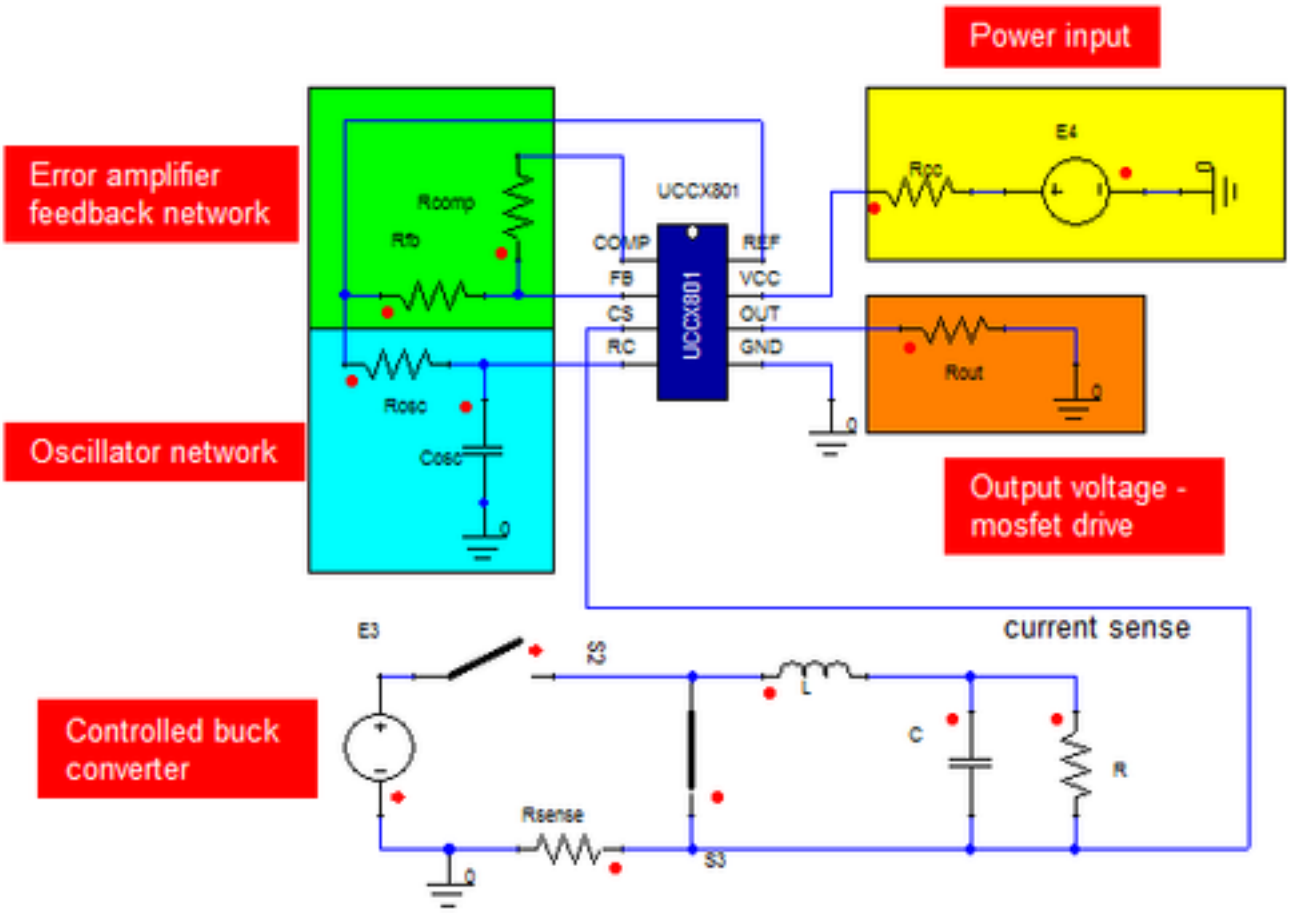

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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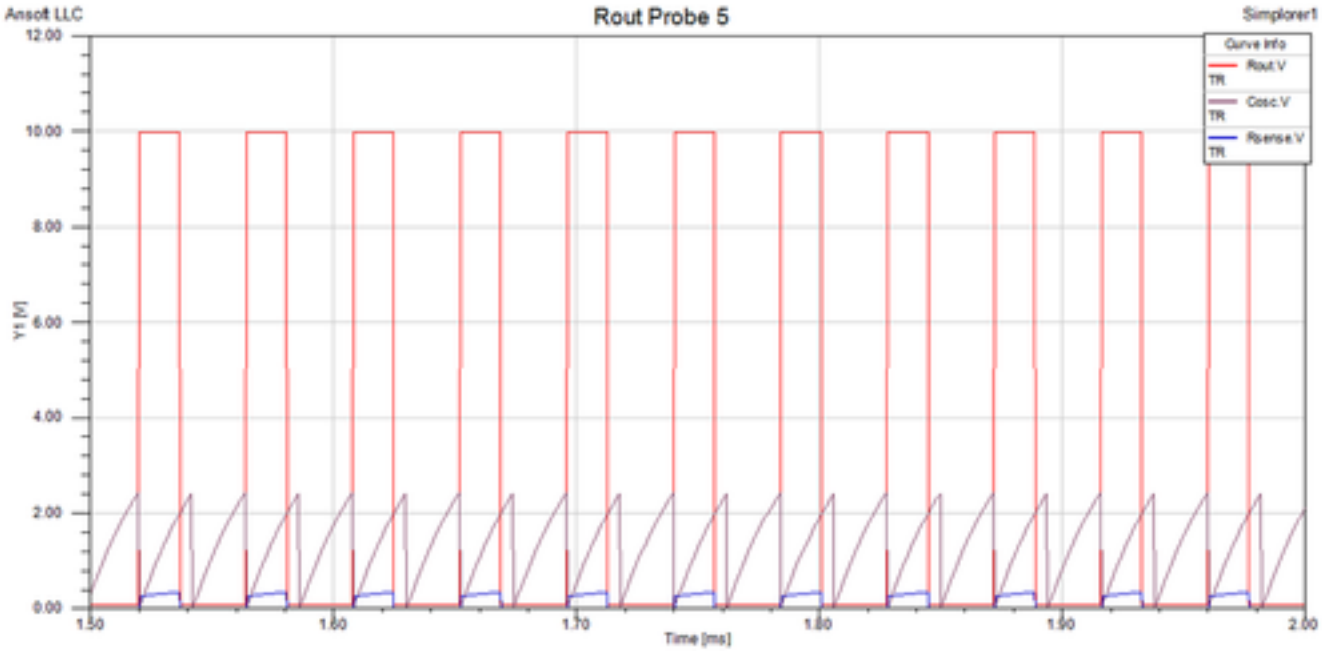
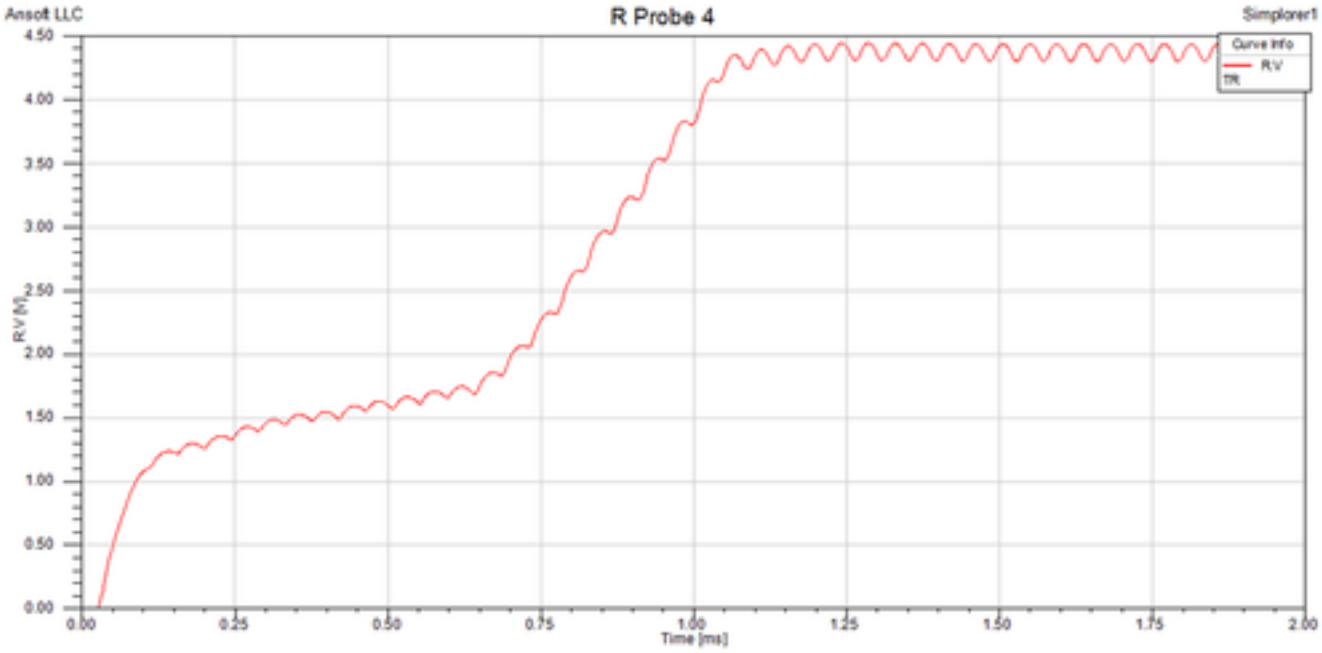


Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)



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Red: converter output voltage.

Figure 4. Simulation results(b)

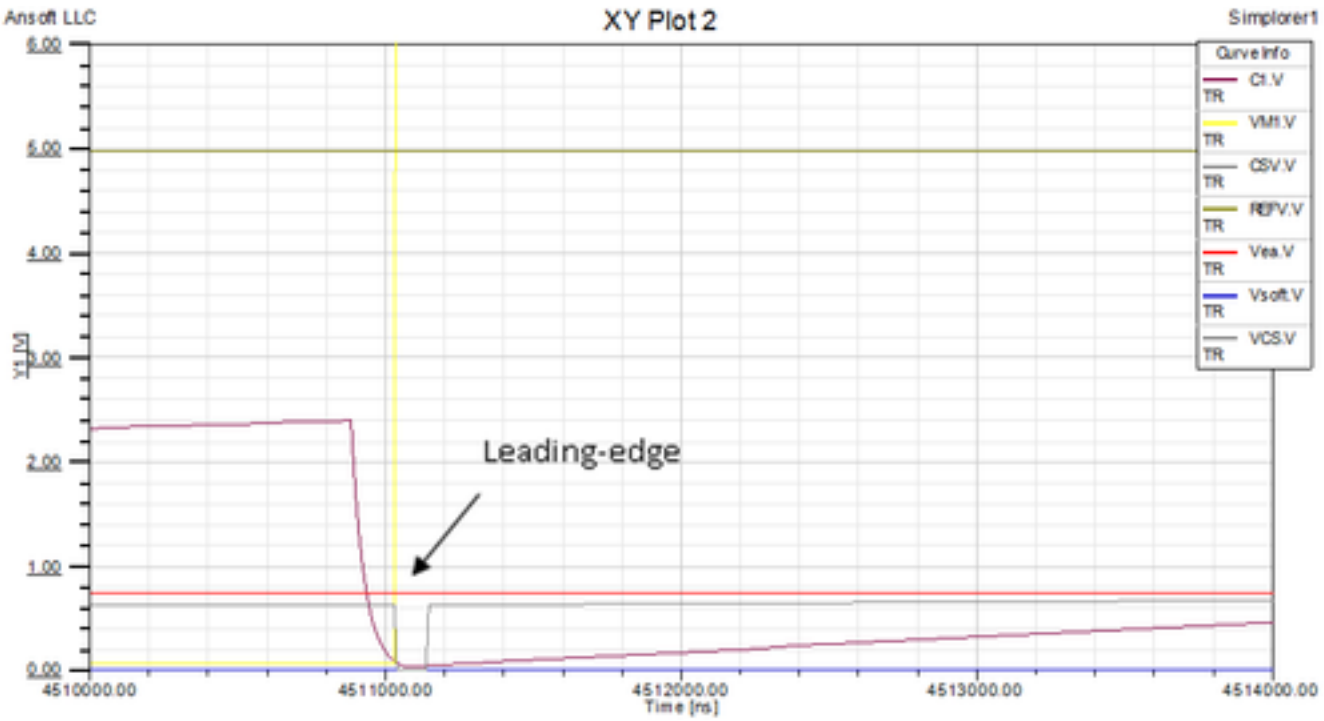

Figure 5. Simulation results(c)

The leading-edge blanking circuit acts like a filter, disconnecting the CS pin from the current sensor during the 100ns following a rising edge of the output voltage.

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UCCx802: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

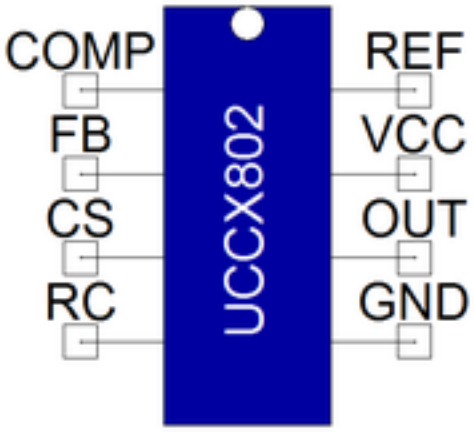

Figure 1. Component symbol

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Description

The *UCCx800/1/2/3/4/5* provides a Pulse Width Modulated (PWM) signal (*UCCX803/5* with a maximum duty cycle of 50%) and current-mode control.

The switching frequency is set by a resistor and a capacitor connected to the RC pin, which forms a RC oscillator circuit with a "saw-tooth" output waveform.

The output voltage rises up at every oscillator peak and when the CS pin voltage reaches the output comparator voltage the output falls.

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The *UCCX801/2/3/4/5* has a soft start circuit that limits the output duty cycle when it initializes. It also has an over current sensor that triggers a soft start cycle when an over current is detected.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output, FB pin is connected to the inverting input and NI to the non-inverting one.
• Current sense: a voltmeter measures the CS pin voltage.
• Oscillator: Its period depends on the resistance and the capacitor connected to RC pin.
• Soft-start: this circuit limits the maximum voltage that the error amplifier can supply during the first cycles after a restart.
• Reference voltage: provides a 5V voltage reference with variable output impedance.
• Output: controlled by a state machine. Its output impedance is variable.

The state machines control the under-voltage protection (when the input voltage falls below 8.3V, the protection activates and the outputs fall to zero), the oscillator, the output voltage and the shutdown function.

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Table 1

Name	Description
1. COMP	Output of the error amplifier
2. FB	Inversing input of the error amplifier
3. CS	Current sense
4. RC	Oscillator
5. GND	Power and reference ground
6. OUT	PWM Output
7. VCC	Power input
8. REF	Reference Voltage

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -55°C ≤TA ≤+125°C for UCC180x; -40°C ≤TA ≤+85°C for UCC280x; 0°C ≤TA ≤+70°C for *UCC380x*; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1 F capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

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Table 2

PARAMETER	TEST CONDITIONS	UCCX80X	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
	T_J=+25°C, I=0.2mA, UCCx803/5	4.00	4.00	
Load Regulation	0.2mA<I<5mA	10-30	25	
Line Regulation	T_J=+25°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	1.9	2.0	mV/V
	T_J=-55°C to +125°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	2.5	2.0	mV/V
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
	UCCx803/5 (Note 7)	4.00	4.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz, T_J=+25°C (Note 9)	130	X	V
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	X	mV
Output Short Circuit		-5 / -35	-35	mA
Oscillator Section				
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	46	46	kHz
	UCCx803/5 (Note 4)	31	33	kHz
Temperature Stability	(Note 9)	2.5	X	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.45	V
Error Amplifier Section				

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Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.5	2.5	V
	COMP=2.0V; UCCx803/5	2.0	2.0	V
Input Bias Current		0	X	V
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle	UCCx800/2/3	99	100	%
	UCCx801/4/5	49	50	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0.1	V
	I=200mA, allparts	0.35	0.1	V
	I=50mA, VCC-C=5V, UCCx803/5	0.15	0.1	V
	I=20mA, VCC-C=0V, all parts	0.7	0.7	V

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OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0.1	V
	I=-200mA, allparts	1.0	1.0	V
	I=-50mA,VCC-C=5V, UCCx803/5	0.4	0.6	V
Rise Time	CL=1nF	41	41	ns
Fall Time	CL=1nF	44	41	ns
Undervoltage Lockout Section				
Start Threshold (Note 8)	UCCx800	7.2	7.2	V
	UCCx801	9.4	9.4	V
	UCCx802/4	12.5	12.5	V
	UCCx803/5	4.1	4.1	V
Stop Threshold (Note 8)	UCCx800	6.9	6.9	V
	UCCx801	7.4	7.4	V
	UCCx802/4	8.3	8.3	V
	UCCx803/5	3.6	3.6	V
Start to Stop Hysteresis	UCCx800	0.3	0.3	V
	UCCx801	2	2	V
	UCCx802/4	4.2	4.2	V
	UCCx803/5	0.5	0.5	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0.5	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start	CS=0V	1.0	1.0	V

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Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency. Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.
Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤Vcs ≤0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.
Note 10: The device is fully operating in clamp mode as the forcing current is higher than the normal operating supply current.

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Example circuit :

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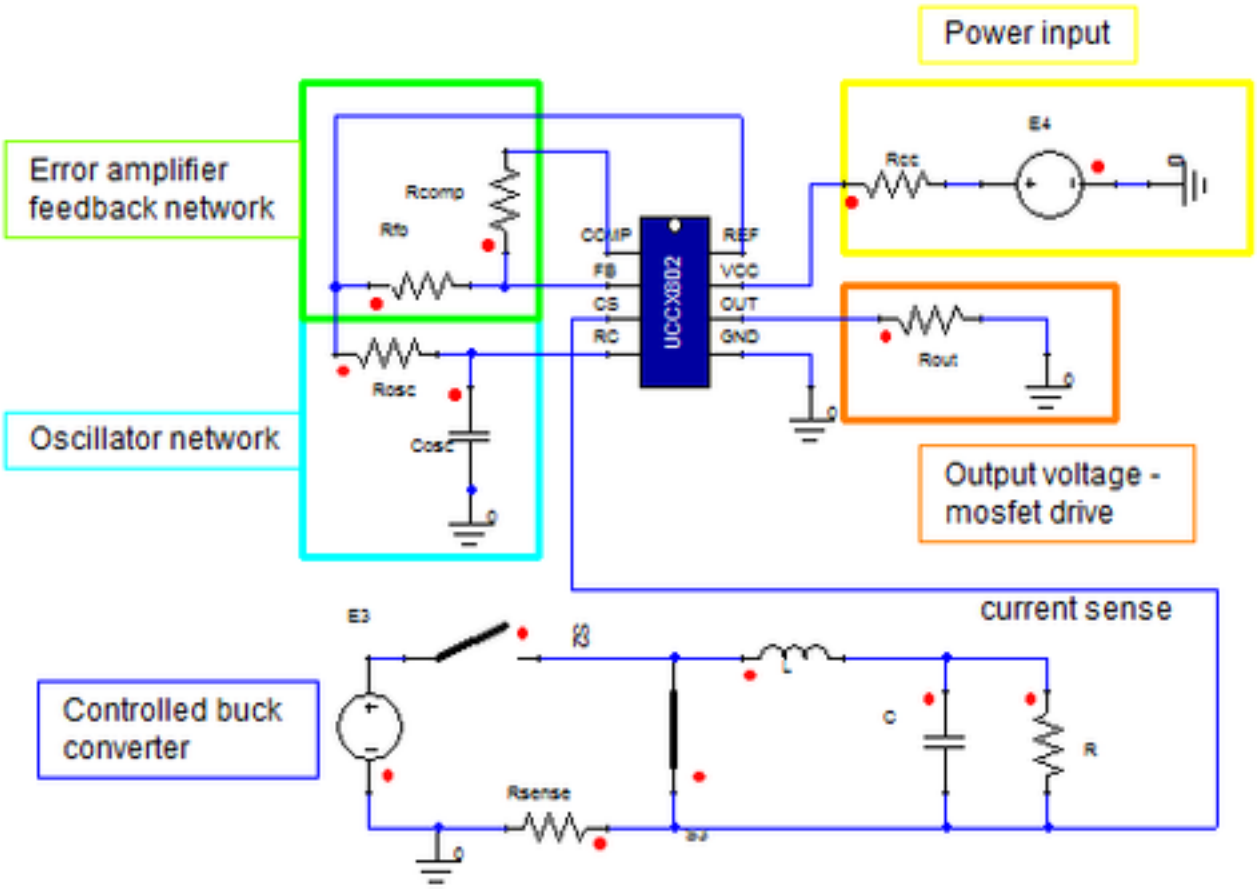

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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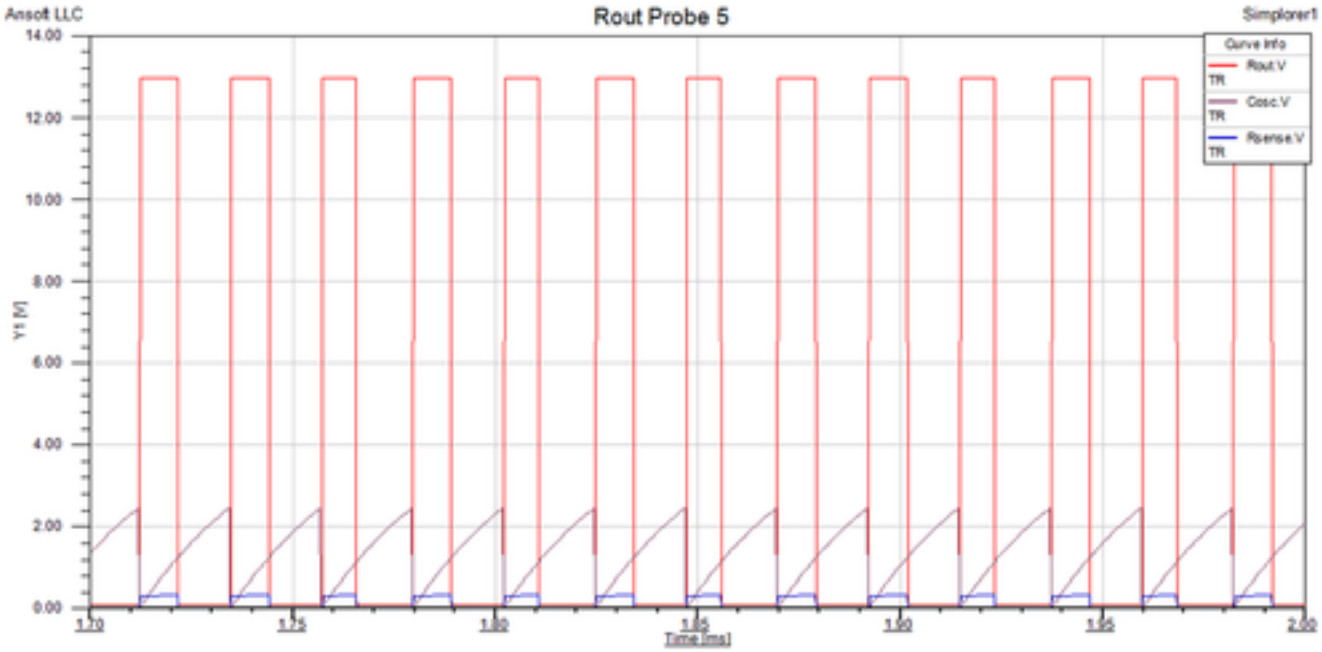
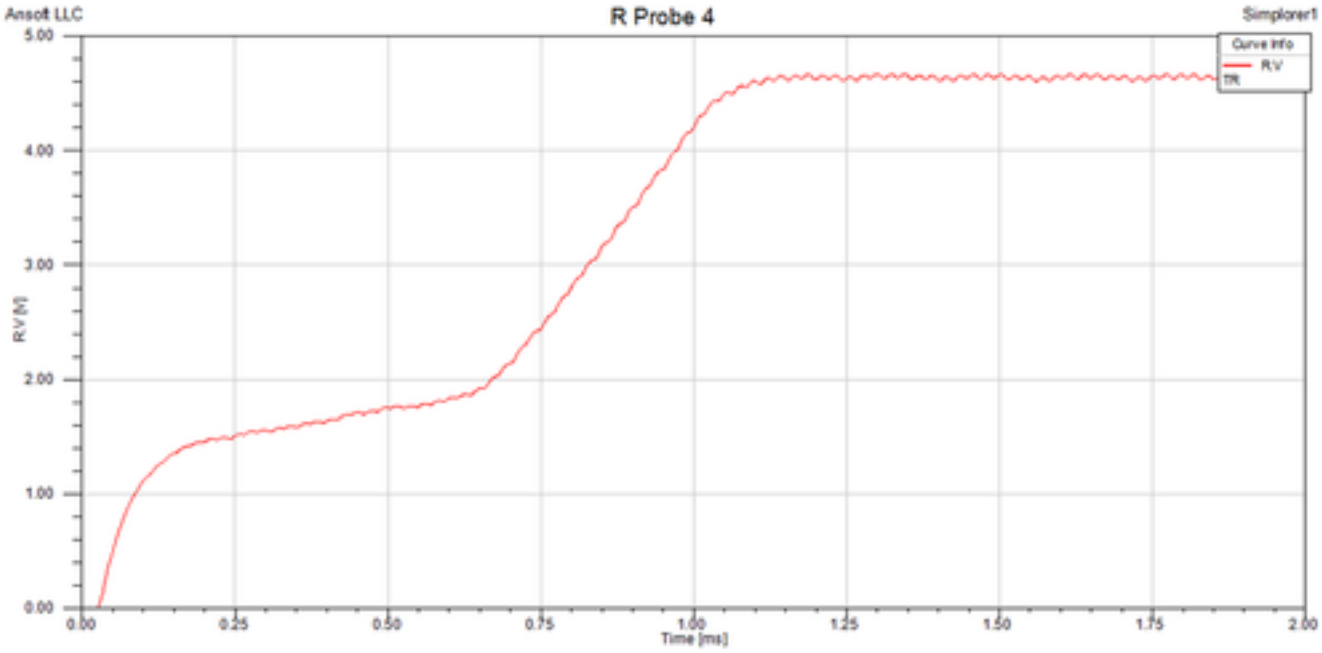


Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)



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Red: converter output voltage.

Figure 4. Simulation results(b)

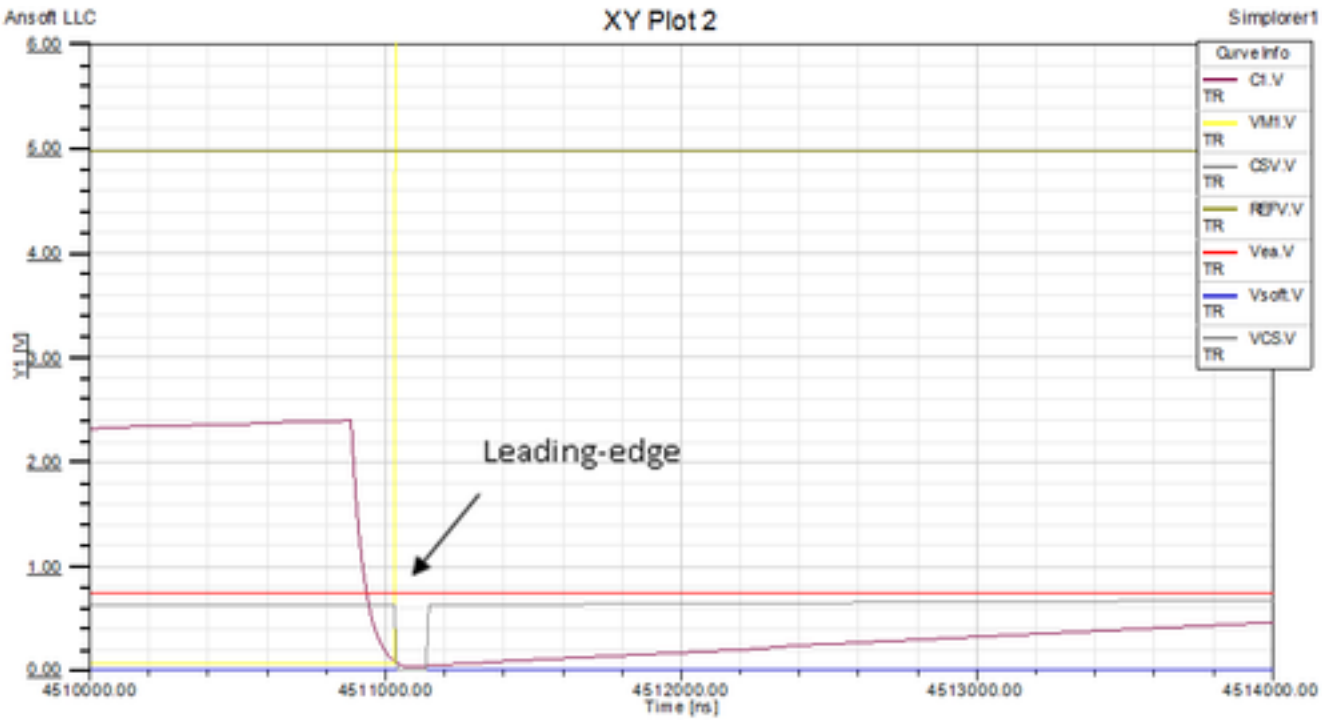

Figure 5. Simulation results(c)

The leading-edge blanking circuit acts like a filter, disconnecting the CS pin from the current sensor during the 100ns following a rising edge of the output voltage.

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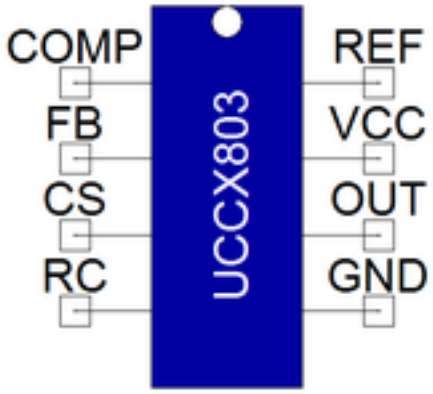
UCCx803: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCCx800/1/2/3/4/5* provides a Pulse Width Modulated (PWM) signal (*UCCX803/5* with a maximum duty cycle of 50%) and current-mode control.

The switching frequency is set by a resistor and a capacitor connected to the RC pin, which forms a RC oscillator circuit with a "saw-tooth" output waveform.

The output voltage rises up at every oscillator peak and when the CS pin voltage reaches the output comparator voltage the output falls.

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The *UCCX801/2/3/4/5* has a soft start circuit that limits the output duty cycle when it initializes. It also has an over current sensor that triggers a soft start cycle when an over current is detected.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output, FB pin is connected to the inverting input and NI to the non-inverting one.
• Current sense: a voltmeter measures the CS pin voltage.
• Oscillator: Its period depends on the resistance and the capacitor connected to RC pin.
• Soft-start: this circuit limits the maximum voltage that the error amplifier can supply during the first cycles after a restart.
• Reference voltage: provides a 5V voltage reference with variable output impedance.
• Output: controlled by a state machine. Its output impedance is variable.

The state machines control the under-voltage protection (when the input voltage falls below 3.6V, the protection activates and the outputs fall to zero), the oscillator, the output voltage and the shutdown function.

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Table 1

Name	Description
1. COMP	Output of the error amplifier
2. FB	Inversing input of the error amplifier
3. CS	Current sense
4. RC	Oscillator
5. GND	Power and reference ground
6. OUT	PWM Output
7. VCC	Power input
8. REF	Reference Voltage

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -55°C ≤TA ≤+125°C for UCC180x; -40°C ≤TA ≤+85°C for UCC280x; 0°C ≤TA ≤+70°C for *UCC380x*; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1 F capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

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Table 2

PARAMETER	TEST CONDITIONS	UCCX80X	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
	T_J=+25°C, I=0.2mA, UCCx803/5	4.00	4.00	
Load Regulation	0.2mA<I<5mA	10-30	25	
Line Regulation	T_J=+25°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	1.9	2.0	mV/V
	T_J=-55°C to +125°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	2.5	2.0	mV/V
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
	UCCx803/5 (Note 7)	4.00	4.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz, T_J=+25°C (Note 9)	130	X	V
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	X	mV
Output Short Circuit		-5 / -35	-35	mA
Oscillator Section				
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	46	46	kHz
	UCCx803/5 (Note 4)	31	33	kHz
Temperature Stability	(Note 9)	2.5	X	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.45	V
Error Amplifier Section				

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Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.5	2.5	V
	COMP=2.0V; UCCx803/5	2.0	2.0	V
Input Bias Current		0	X	V
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle	UCCx800/2/3	99	100	%
	UCCx801/4/5	49	50	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0.1	V
	I=200mA, allparts	0.35	0.1	V
	I=50mA, VCC-C=5V, UCCx803/5	0.15	0.1	V
	I=20mA, VCC-C=0V, all parts	0.7	0.7	V

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OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0.1	V
	I=-200mA, allparts	1.0	1.0	V
	I=-50mA,VCC-C=5V, UCCx803/5	0.4	0.6	V
Rise Time	CL=1nF	41	41	ns
Fall Time	CL=1nF	44	41	ns
Undervoltage Lockout Section				
Start Threshold (Note 8)	UCCx800	7.2	7.2	V
	UCCx801	9.4	9.4	V
	UCCx802/4	12.5	12.5	V
	UCCx803/5	4.1	4.1	V
Stop Threshold (Note 8)	UCCx800	6.9	6.9	V
	UCCx801	7.4	7.4	V
	UCCx802/4	8.3	8.3	V
	UCCx803/5	3.6	3.6	V
Start to Stop Hysteresis	UCCx800	0.3	0.3	V
	UCCx801	2	2	V
	UCCx802/4	4.2	4.2	V
	UCCx803/5	0.5	0.5	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0.5	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start	CS=0V	1.0	1.0	V

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Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency. Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.
Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤Vcs ≤0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
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Examples

Example circuit :

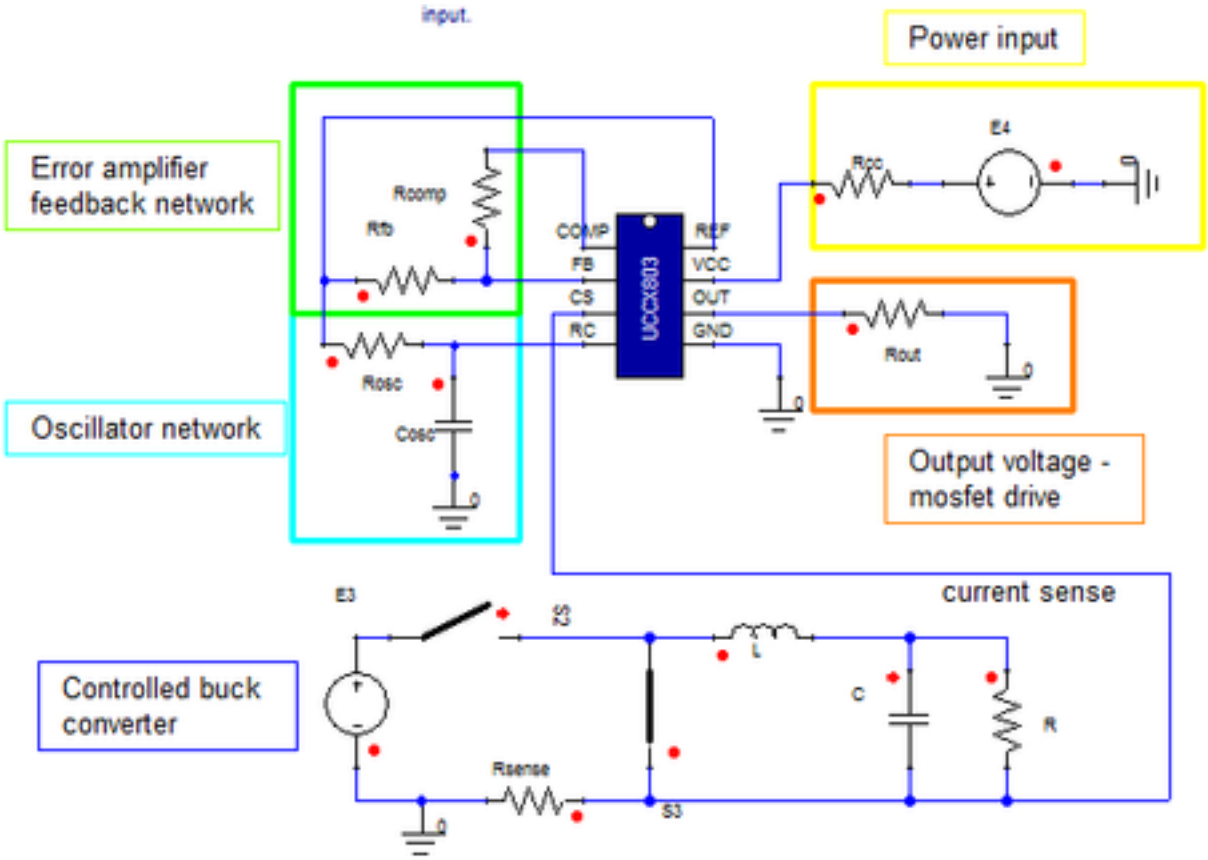

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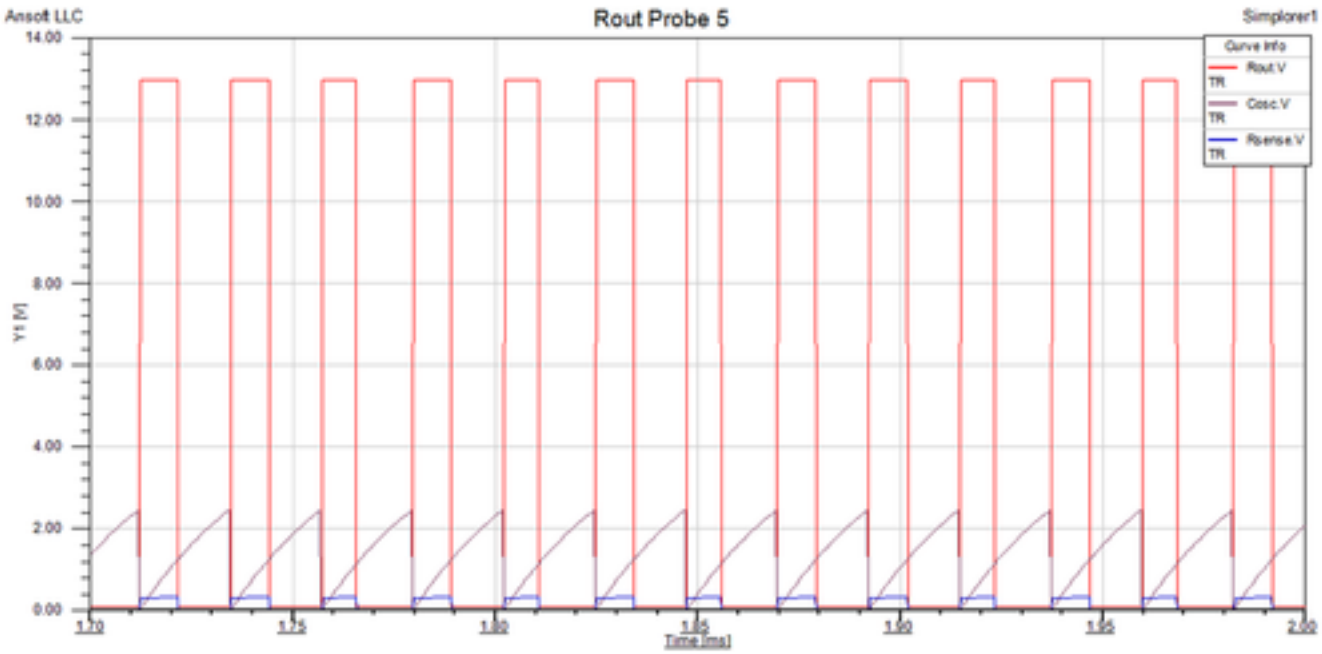
Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :



Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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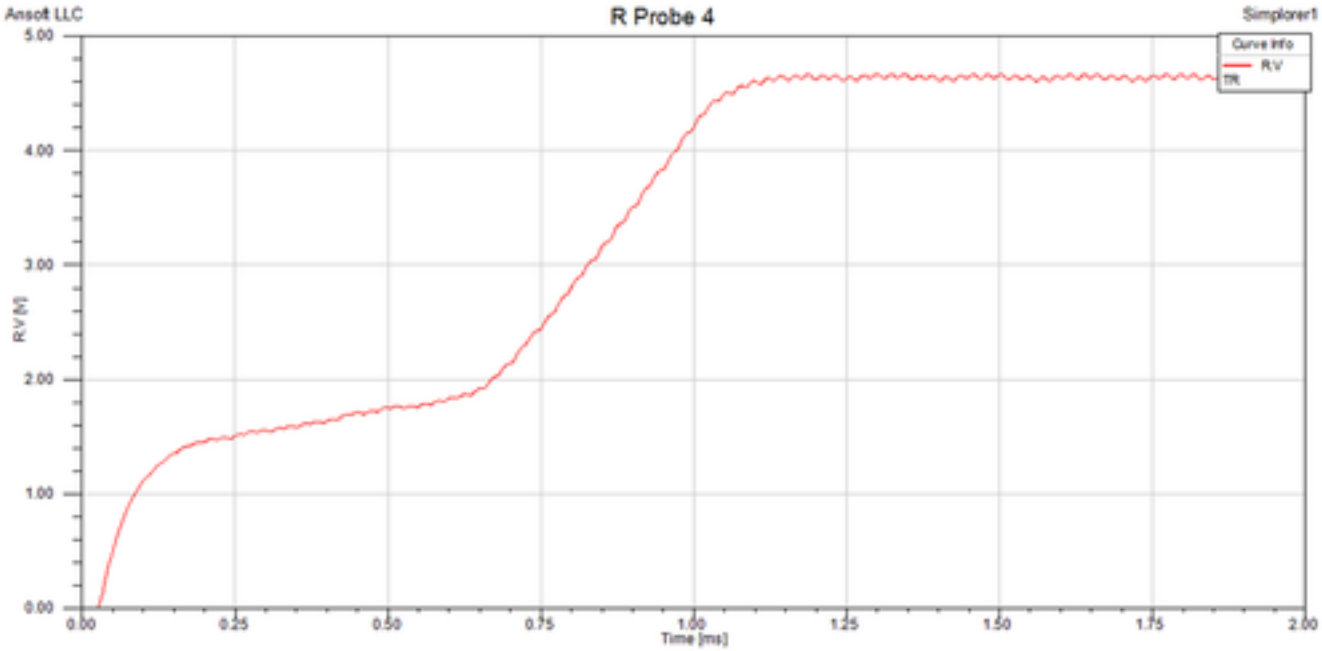

Red: converter output voltage.

Figure 4. Simulation results(b)

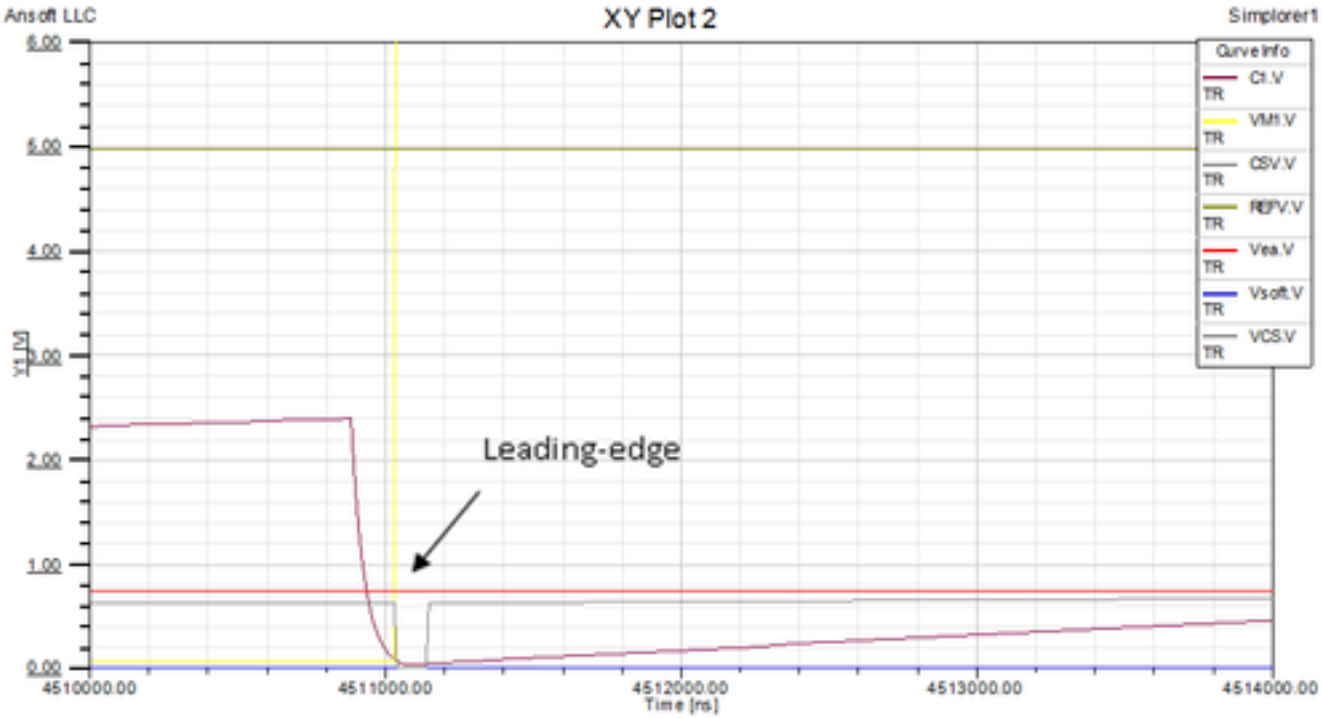

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Figure 5. Simulation results(c)

The leading-edge blanking circuit acts like a filter, disconnecting the CS pin from the current sensor during the 100ns following a rising edge of the output voltage.

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UCCx804: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

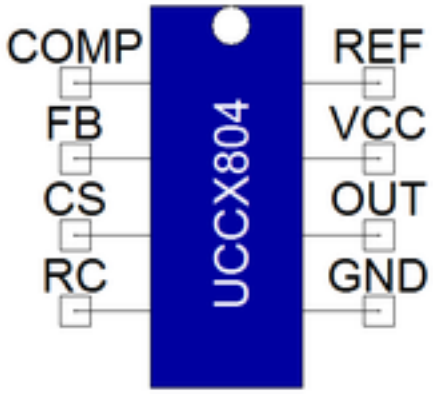

Figure 1. Component symbol

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Description

The *UCCx800/1/2/3/4/5* provides a Pulse Width Modulated (PWM) signal (*UCCX803/5* with a maximum duty cycle of 50%) and current-mode control.

The switching frequency is set by a resistor and a capacitor connected to the RC pin, which forms a RC oscillator circuit with a "saw-tooth" output waveform.

The output voltage rises up at every oscillator peak and when the CS pin voltage reaches the output comparator voltage the output falls.

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The *UCCX801/2/3/4/5* has a soft start circuit that limits the output duty cycle when it initializes. It also has an over current sensor that triggers a soft start cycle when an over current is detected.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output, FB pin is connected to the inverting input and NI to the non-inverting one.
• Current sense: a voltmeter measures the CS pin voltage.
• Oscillator: Its period depends on the resistance and the capacitor connected to RC pin.
• Soft-start: this circuit limits the maximum voltage that the error amplifier can supply during the first cycles after a restart.
• Reference voltage: provides a 5V voltage reference with variable output impedance.
• Output: controlled by a state machine. Its output impedance is variable.

The state machines control the under-voltage protection (when the input voltage falls below 8.3V, the protection activates and the outputs fall to zero), the oscillator, the output voltage and the shutdown function.

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Table 1

Name	Description
1. COMP	Output of the error amplifier
2. FB	Inversing input of the error amplifier
3. CS	Current sense
4. RC	Oscillator
5. GND	Power and reference ground
6. OUT	PWM Output
7. VCC	Power input
8. REF	Reference Voltage

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -55°C ≤TA ≤+125°C for UCC180x; -40°C ≤TA ≤+85°C for UCC280x; 0°C ≤TA ≤+70°C for *UCC380x*; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1 F capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

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Table 2

PARAMETER	TEST CONDITIONS	UCCX80X	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
	T_J=+25°C, I=0.2mA, UCCx803/5	4.00	4.00	
Load Regulation	0.2mA<I<5mA	10-30	25	
Line Regulation	T_J=+25°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	1.9	2.0	mV/V
	T_J=-55°C to +125°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	2.5	2.0	mV/V
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
	UCCx803/5 (Note 7)	4.00	4.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz, T_J=+25°C (Note 9)	130	X	V
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	X	mV
Output Short Circuit		-5 / -35	-35	mA
Oscillator Section				
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	46	46	kHz
	UCCx803/5 (Note 4)	31	33	kHz
Temperature Stability	(Note 9)	2.5	X	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.45	V
Error Amplifier Section				

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Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.5	2.5	V
	COMP=2.0V; UCCx803/5	2.0	2.0	V
Input Bias Current		0	X	V
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle	UCCx800/2/3	99	100	%
	UCCx801/4/5	49	50	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0.1	V
	I=200mA, allparts	0.35	0.1	V
	I=50mA, VCC-C=5V, UCCx803/5	0.15	0.1	V
	I=20mA, VCC-C=0V, all parts	0.7	0.7	V

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OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0.1	V
	I=-200mA, allparts	1.0	1.0	V
	I=-50mA,VCC-C=5V, UCCx803/5	0.4	0.6	V
Rise Time	CL=1nF	41	41	ns
Fall Time	CL=1nF	44	41	ns
Undervoltage Lockout Section				
Start Threshold (Note 8)	UCCx800	7.2	7.2	V
	UCCx801	9.4	9.4	V
	UCCx802/4	12.5	12.5	V
	UCCx803/5	4.1	4.1	V
Stop Threshold (Note 8)	UCCx800	6.9	6.9	V
	UCCx801	7.4	7.4	V
	UCCx802/4	8.3	8.3	V
	UCCx803/5	3.6	3.6	V
Start to Stop Hysteresis	UCCx800	0.3	0.3	V
	UCCx801	2	2	V
	UCCx802/4	4.2	4.2	V
	UCCx803/5	0.5	0.5	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0.5	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start	CS=0V	1.0	1.0	V

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Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency. Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.
Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤Vcs ≤0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.
Note 10: The device is fully operating in clamp mode as the forcing current is higher than the normal operating supply current.

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Example circuit :

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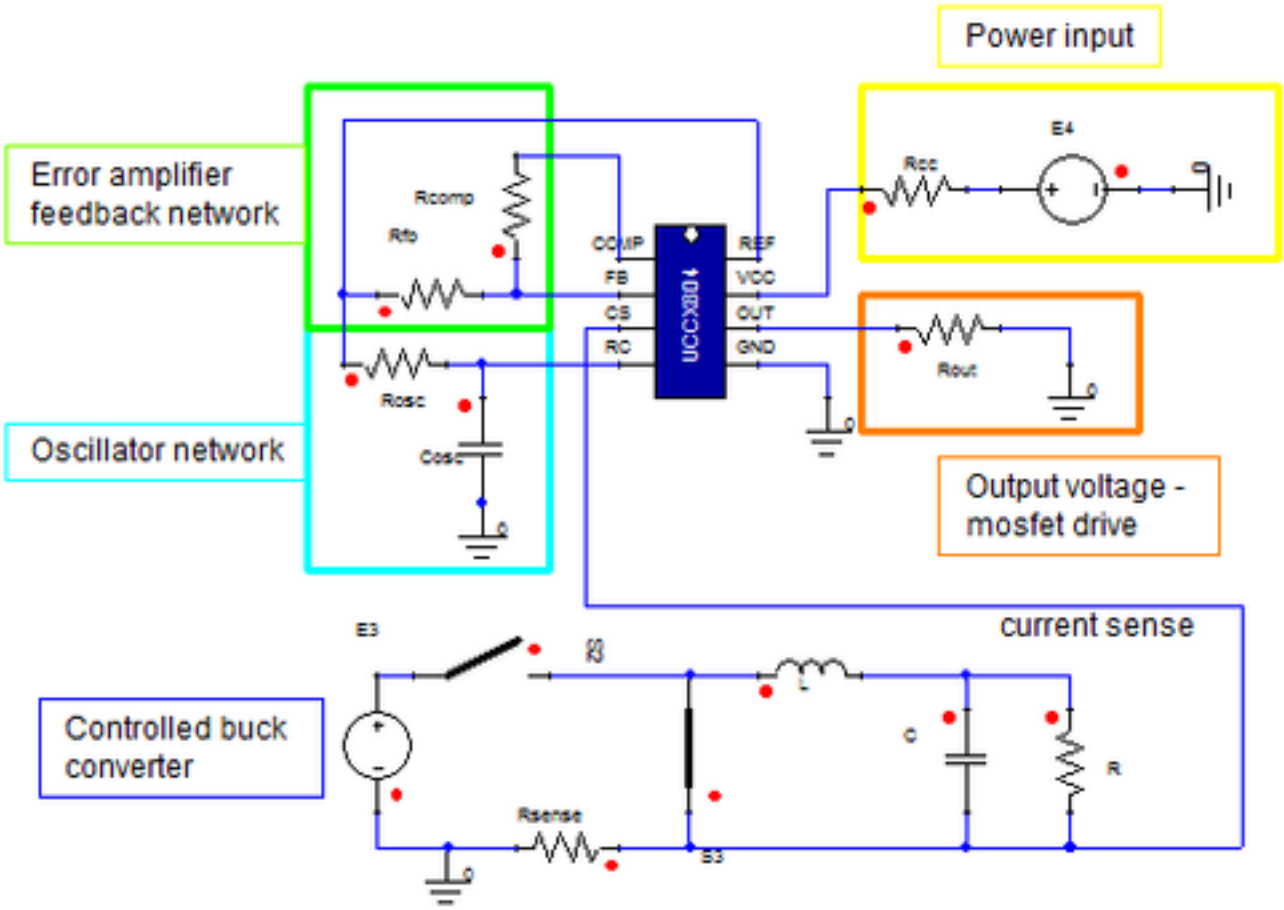

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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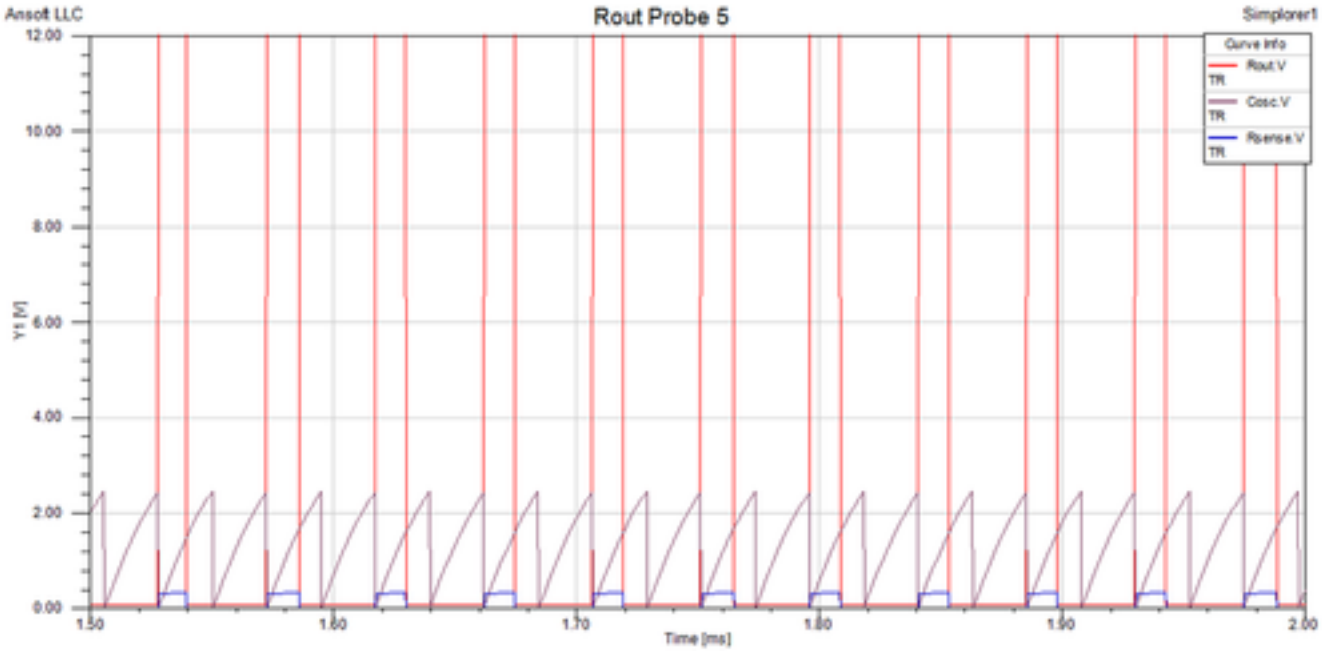
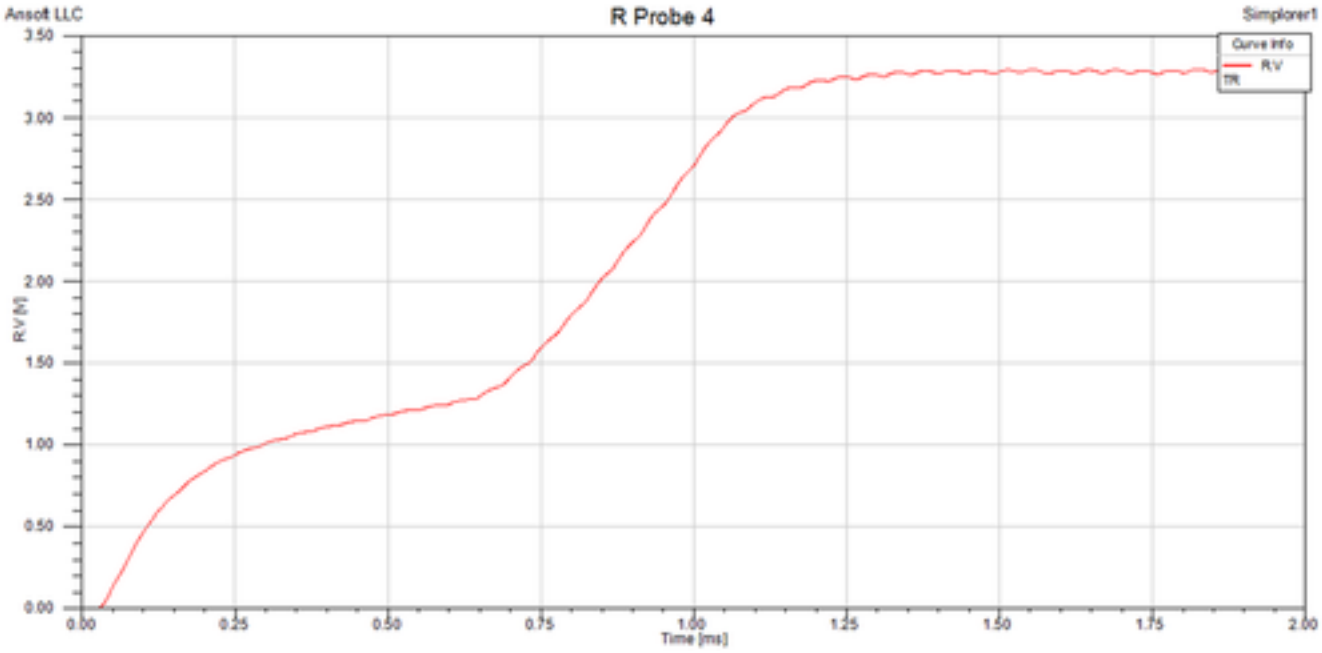


Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)



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Red: converter output voltage.

Figure 4. Simulation results(b)

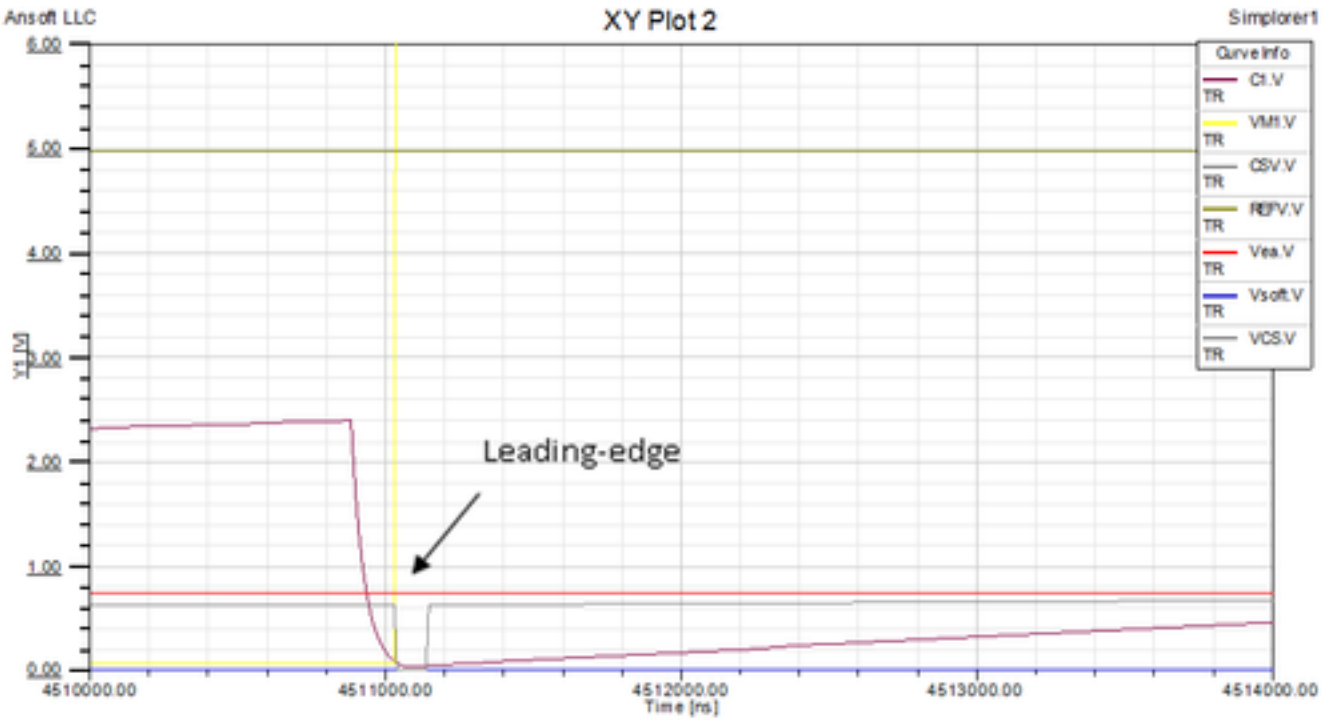

Figure 5. Simulation results(c)

The leading-edge blanking circuit acts like a filter, disconnecting the CS pin from the current sensor during the 100ns following a rising edge of the output voltage.

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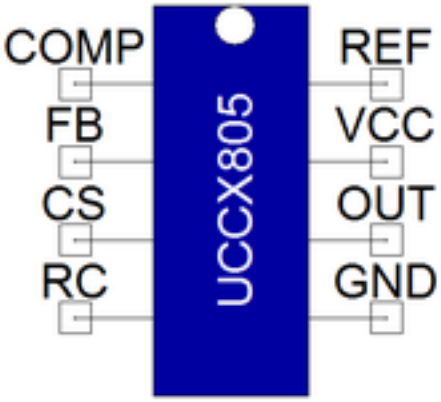
UCCx805: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output, FB pin is connected to the inverting input and NI to the non-inverting one.
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• Reference voltage: provides a 5V voltage reference with variable output impedance.
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Table 1

Name	Description
1. COMP	Output of the error amplifier
2. FB	Inversing input of the error amplifier
3. CS	Current sense
4. RC	Oscillator
5. GND	Power and reference ground
6. OUT	PWM Output
7. VCC	Power input
8. REF	Reference Voltage

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Comparison between model and real component.

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Table 2

PARAMETER	TEST CONDITIONS	UCCX80X	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
	T_J=+25°C, I=0.2mA, UCCx803/5	4.00	4.00	
Load Regulation	0.2mA<I<5mA	10-30	25	
Line Regulation	T_J=+25°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	1.9	2.0	mV/V
	T_J=-55°C to +125°C, V_{CC}=10V to Clamp (I_{VCC}=25mA)	2.5	2.0	mV/V
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
	UCCx803/5 (Note 7)	4.00	4.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz, T_J=+25°C (Note 9)	130	X	V
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	X	mV
Output Short Circuit		-5 / -35	-35	mA
Oscillator Section				
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	46	46	kHz
	UCCx803/5 (Note 4)	31	33	kHz
Temperature Stability	(Note 9)	2.5	X	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.45	V
Error Amplifier Section				

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Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.5	2.5	V
	COMP=2.0V; UCCx803/5	2.0	2.0	V
Input Bias Current		0	X	V
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle	UCCx800/2/3	99	100	%
	UCCx801/4/5	49	50	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0.1	V
	I=200mA, allparts	0.35	0.1	V
	I=50mA, VCC-C=5V, UCCx803/5	0.15	0.1	V
	I=20mA, VCC-C=0V, all parts	0.7	0.7	V

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OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0.1	V
	I=-200mA, allparts	1.0	1.0	V
	I=-50mA,VCC-C=5V, UCCx803/5	0.4	0.6	V
Rise Time	CL=1nF	41	41	ns
Fall Time	CL=1nF	44	41	ns
Undervoltage Lockout Section				
Start Threshold (Note 8)	UCCx800	7.2	7.2	V
	UCCx801	9.4	9.4	V
	UCCx802/4	12.5	12.5	V
	UCCx803/5	4.1	4.1	V
Stop Threshold (Note 8)	UCCx800	6.9	6.9	V
	UCCx801	7.4	7.4	V
	UCCx802/4	8.3	8.3	V
	UCCx803/5	3.6	3.6	V
Start to Stop Hysteresis	UCCx800	0.3	0.3	V
	UCCx801	2	2	V
	UCCx802/4	4.2	4.2	V
	UCCx803/5	0.5	0.5	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0.5	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start	CS=0V	1.0	1.0	V

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Note 3: Adjust VCC above the start threshold before setting at 10V.
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Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤Vcs ≤0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.
Note 10: The device is fully operating in clamp mode as the forcing current is higher than the normal operating supply current.

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Examples

Example circuit :

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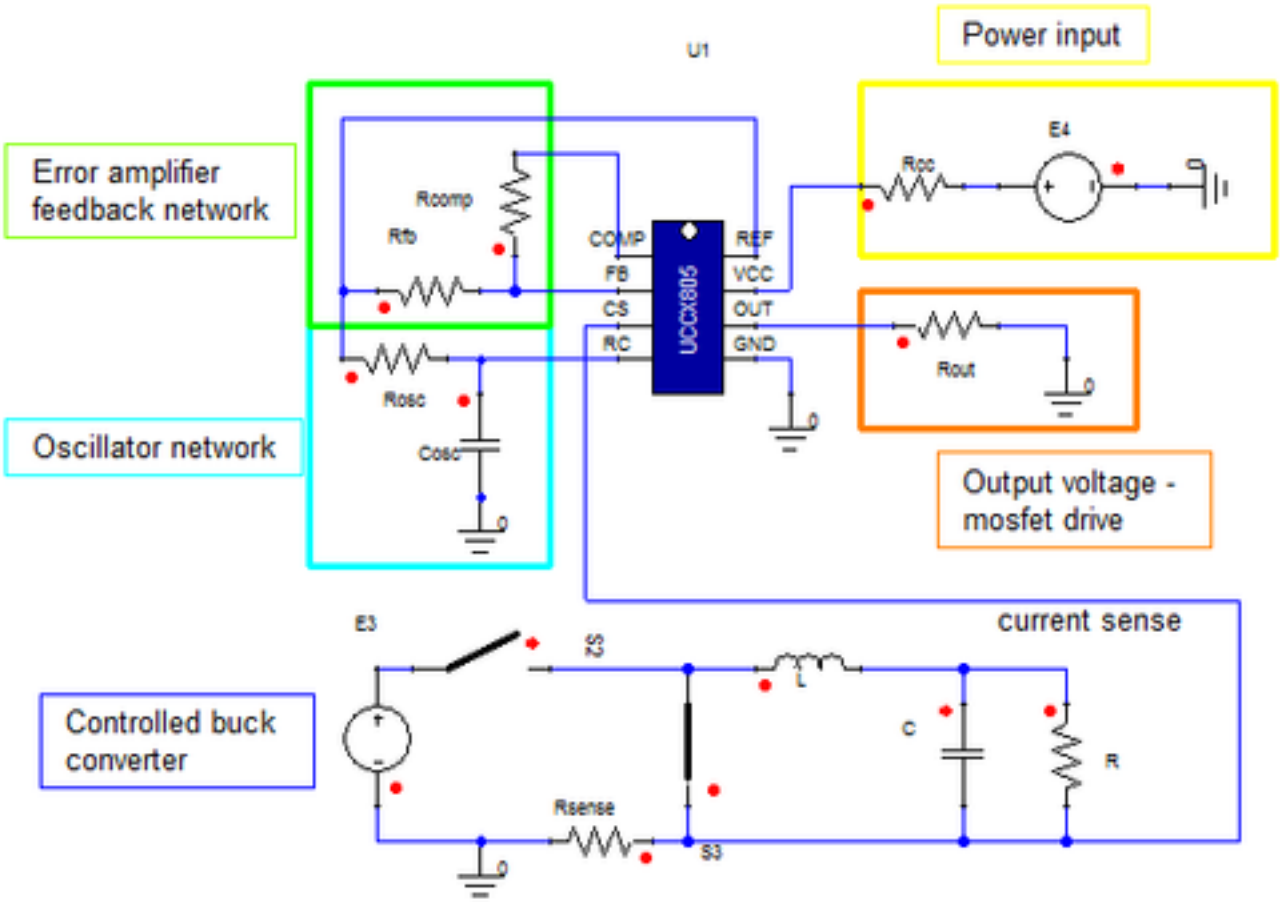

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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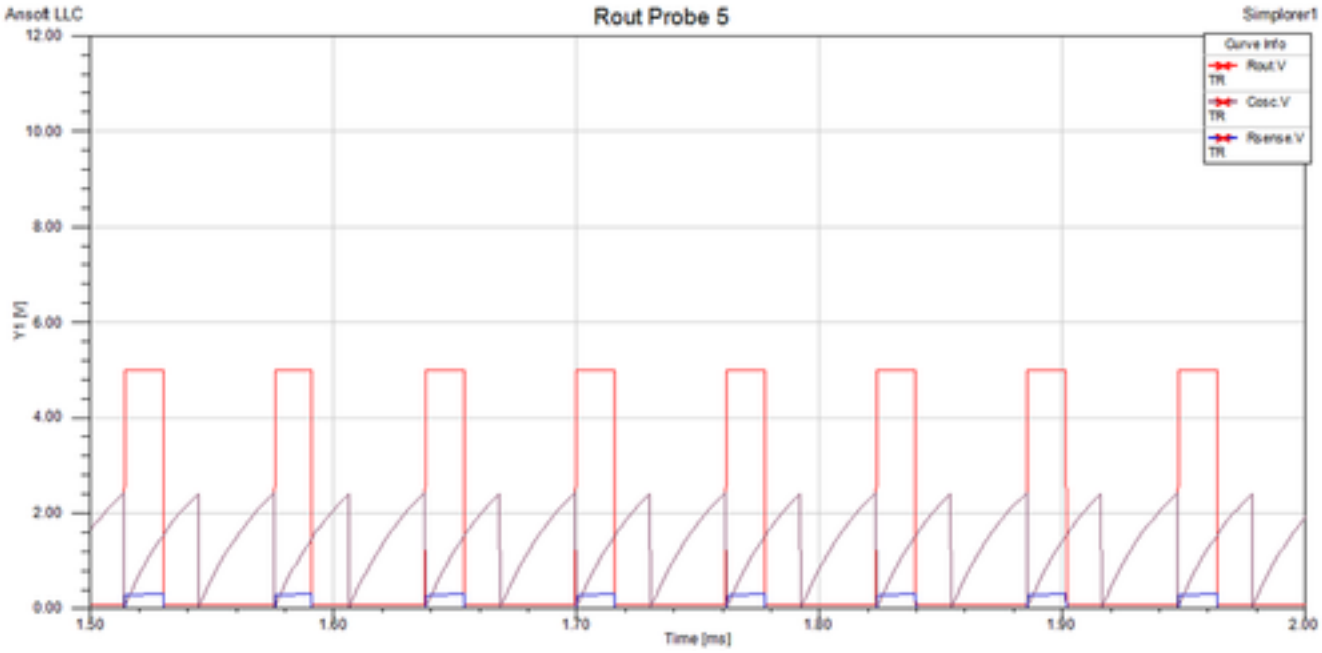
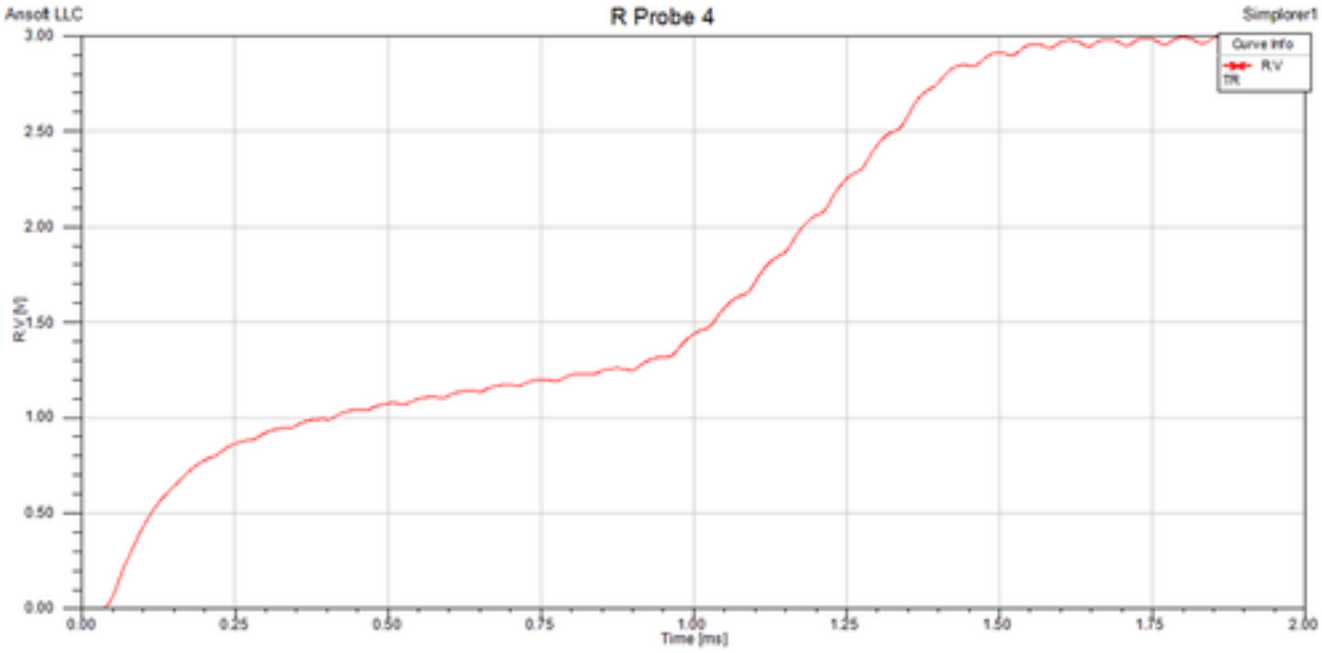


Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)



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Red: converter output voltage.

Figure 4. Simulation results(b)

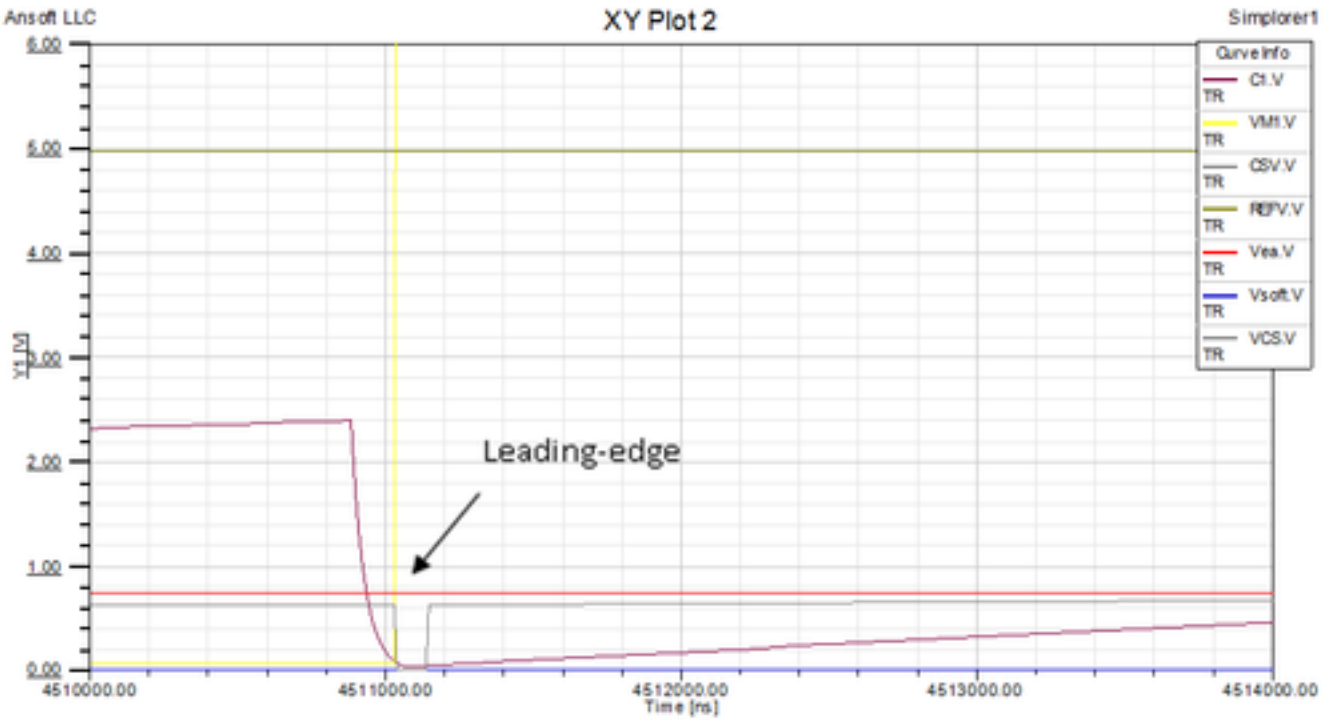

Figure 5. Simulation results(c)

The leading-edge blanking circuit acts like a filter, disconnecting the CS pin from the current sensor during the 100ns following a rising edge of the output voltage.

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UCCx806: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

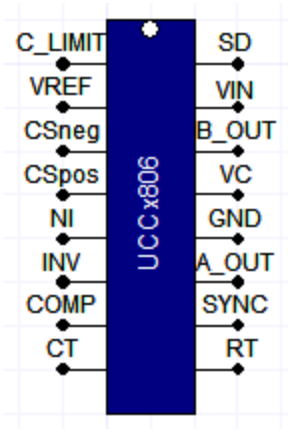

Figure 1. Component symbol

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Description

The *UCC1806* family of BiCMOS PWM controllers offers exceptionally improved performance with a familiar architecture. With the same block diagram and pinout of the popular *UC1846* series, the *UCC1806* line features increased switching frequency capability while greatly reducing the bias current used within the device. With a typical startup current of 50µA and a well defined voltage threshold for turn-on, these devices are favored for applications ranging from off-line power supplies to battery operated portable equipment. Dual high current, FET driving outputs and a fast current sense loop further enhance device versatility.

All the benefits of current mode control including simpler loop closing, voltage feed-forward, parallel ability with current sharing, pulse-by-pulse current limiting, and push-pull symmetry correction are readily achievable with the *UCC1806* series.

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This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output, INV pin is connected to the inverting input and NI to the non-inverting one.
• Differential current sense: a voltmeter measures the voltage between CS+ and CS- pins.
• Oscillator: Its period depends on the resistance connected to Rt pin and the capacitor to Ct. Sync pin allows synchronizing two UCx806 devices.
• Current limit and soft-start: voltmeters measure the voltage on these pins to set the current peak.
• Reference voltage: provides an ideal 5.1V voltage reference with zero output impedance.
• Outputs A & B: controlled by a state machine. Their output impedance is zero.
• Shutdown: a voltmeter measures the SD pin voltage. When its value falls below 0.350V, the IC shuts down.

The state machines control the under-voltage protection (when the input voltage falls below 7.5V, the protection activates and the outputs fall to zero), the oscillator, the output voltage and the shutdown function.

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Table 1

PIN	DESCRIPTION
C_LIMIT	Current limit / Soft-start
VREF	Reference voltage
C/S-	Differential current sense, negative pin
C/S+	Differential current sense, positive pin
NI	Non-inverting error amplifier input
INV	Inverting error amplifier input
Comp	Error amplifier output
CT	Oscillator capacitor pin

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RT	Oscillator resistor pin
Sync	Clock and synchronization pin
A Out	A output
Gnd	Ground
VC	Power supply voltaje
B Out	B output
VIN	Supply voltaje
Shutdown	Shutdown input

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications hold for TA = -55°C to +125°C for the UCC1806, -40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; VIN = 12V, RT = 33k, CT = 330pF, CBYPASS on VREF = 0.01µF, TA= TJ.

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Table 2

PARAMETER	TEST CONDITION	UCCx806			MODEL	UNITS
		MIN	TYP	MAX		
Reference Section						
Output Voltage	TJ = 25°C, IO = 0.2mA	5.02	5.10	5.17	5.10	V
Load Regulation	0.2mA < IO<5mA		3	25	0	mV
Total Output Variation	Line, Load, Temperature (Note 7)	-150		150	0	mV
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, TJ = 25°C (Note 5)		70		0	µV
Long Term Stability	TA = 125°C, 1000 Hours (Note 5)		5	25	0	mV
Output Short Circuit		-10		-30	X	mA
Oscillator Section						
Initial Accuracy	TJ = 25°C	42	47	52	47	kHz
Temperature Stability	TMIN < TA < TMAX (Note 5)		2		0	%
Amplitude			2.35		2.35	V
SYNC Delay to Outputs	Pin 8 = 0V, Pin 9 = VREF, VSYNC = 0.8V to 2.0V		50	125	50	ns
Discharge Current	TJ = 25°C, VPIN 8 = 2.0V		2		2	mA
SYNC, VOL	IOUT = +1mA			0.4	0.4	V
SYNC, VOH	IOUT = -4mA	2.4			2.4	V
SYNC, VIL	Pin 8 = 0V, Pin 9 = VREF			0.8	0.8	V
SYNC, VIH	Pin 8 = 0V, Pin 9 = VREF	2.0			2.0	V
SYNC Input Current		−1		+1	0	µA

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Error Amplifier Section						
Input Offset Voltage				5	0	mV
Input BiasCur-rent				–1	0	µA
Input Offset Current				500	0	nA
Common Mode Range		0		VIN-2	X	V
Open Loop Gain	VO = 1.0 to 4.0	80	100		100	dB
Unity Gain Bandwith		1			X	MHz
Output Sink Current	VID < -20mV, VPIN 7 = 1.0V	1			0	mA
Output SourceCur-rent	VID < 20mV, VPIN 7 = 3.0V	–80	–120		0	µA
Output High Level	VID = -50mV	4.5			4.6	V
Output Low Level	VID = -50mV			0.5	0	V
Current Sense Amplifier Section						
Amplifier Gain	VPIN 3 = 0V, VPIN 1 = VREF (Notes 3,4)	2.75	3	3.35	3	V/V
Maximum Differential Input Signal (VPIN 4 - VPIN 3)	VPIN 1 = VREF, VPIN 5 = VREF, VPIN 6 = 0V	1.1			X	V
Input Offset Voltage	VPIN 1 = 0.5V, VPIN 7 = OPEN		10	30	0	mV
CMRR	VCM = 0 to VIN - 3.5	60			X	dB
PSRR		56			X	dB
Input Bias Current	VPIN 1 = 0.5V, PIN 7 OPEN (Note 3)			-1	0	µA
Input Offset Current	VPIN 1 = 0.5V, PIN 7 OPEN (Note 3)			1	0	µA
Delay to	VPIN 5 =		125	175	125	ns

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Outputs	VREF, PIN 6 = 0, PIN 1 = 2.75V, PIN 4 - PIN 3 = 0 to 1.5V step (Note 6)					
Current Limit Adjust Section						
Current Limit Offset	VPIN 3 = 0, VPIN 4 = 0, PIN 7 = open	0.40	0.50	0.60	0.5	V
Input Bias Current				1	0	µA
Minimum Latching Current		300	200		0	µA
Maximum Non-Latch-ing Current			200	80	0	µA
Shutdown Terminal Section						
Threshold Voltage		0.94	1.00	1.06	1.00	V
Input Voltage Range		0		VIN	X	V
Delay to Outputs	VPIN 16 = 0 to 1.3V		75	150	75	ns
Output Section						
Output Sup-ply Voltage		2.5		15	0-∞	V
Output Low Level	ISINK = 20mA		100	300	0	mV
	ISINK = 100mA		0.40	1.1	0	V
Output High Level	ISOURCE = -20mA	11.6	11.9		12	V
	ISOURCE = -100mA	11	11.6		12	V
Rise Time	TJ = 25°C, CLOAD = 1000pF		35	65	0	ns
Fall Time	TJ = 25°C, CLOAD = 1000pF		35	65	0	ns
Under Voltage Lockout Section						
Startup Cur-rent	VIN < Start Threshold		50	100	0	µA
Operating Supply Cur-			1	1.4	0	mA

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rent						
VIN Shunt Voltage	IVIN = 10mA	15		17.5	15	V
Startup Threshold		6.5	7.5	8	7.5	V
Threshold Hysteresis			0.75		0.75	V

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Example circuit :

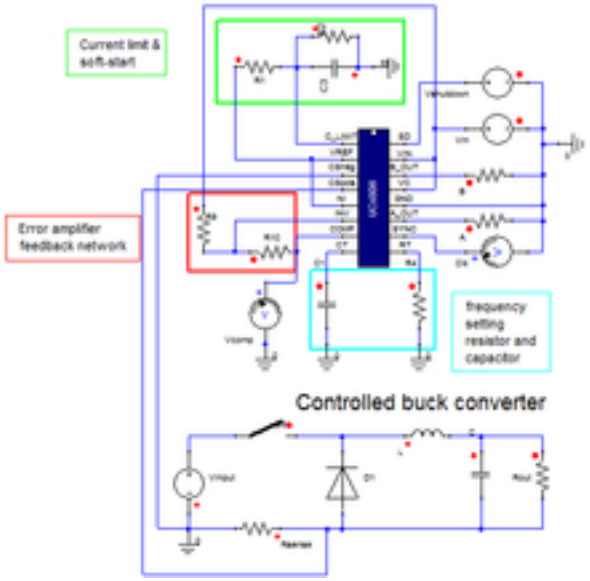

Figure 2. Example Circuit

Simulation results :

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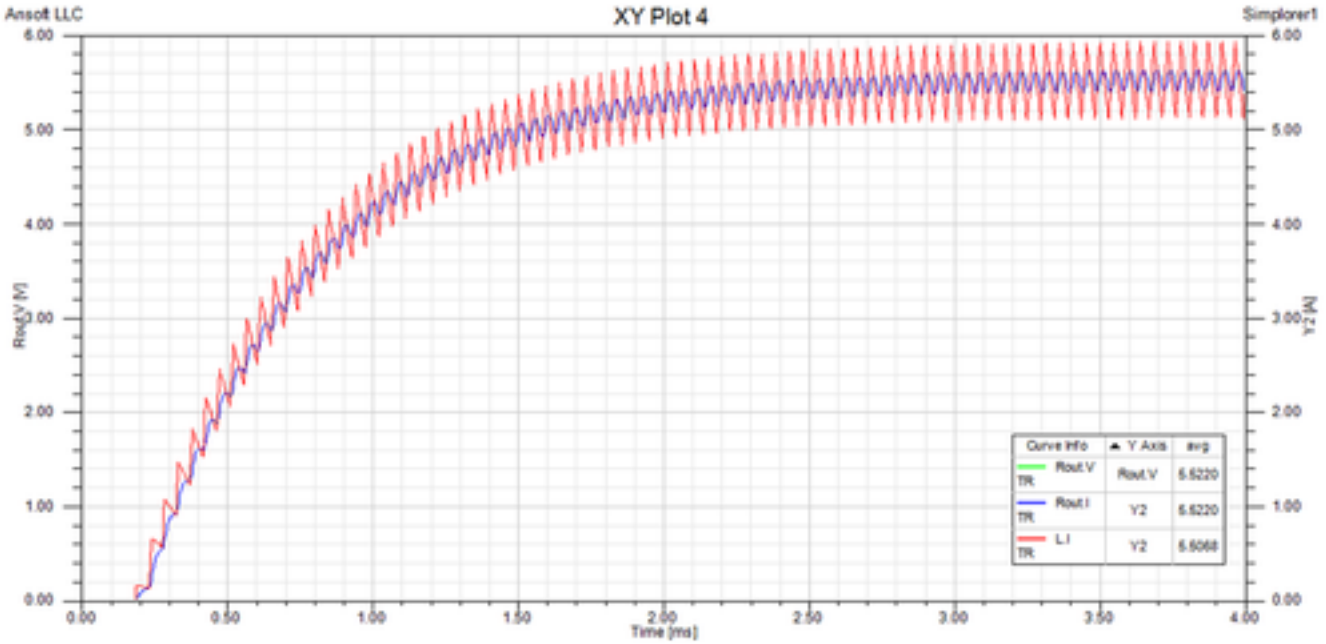
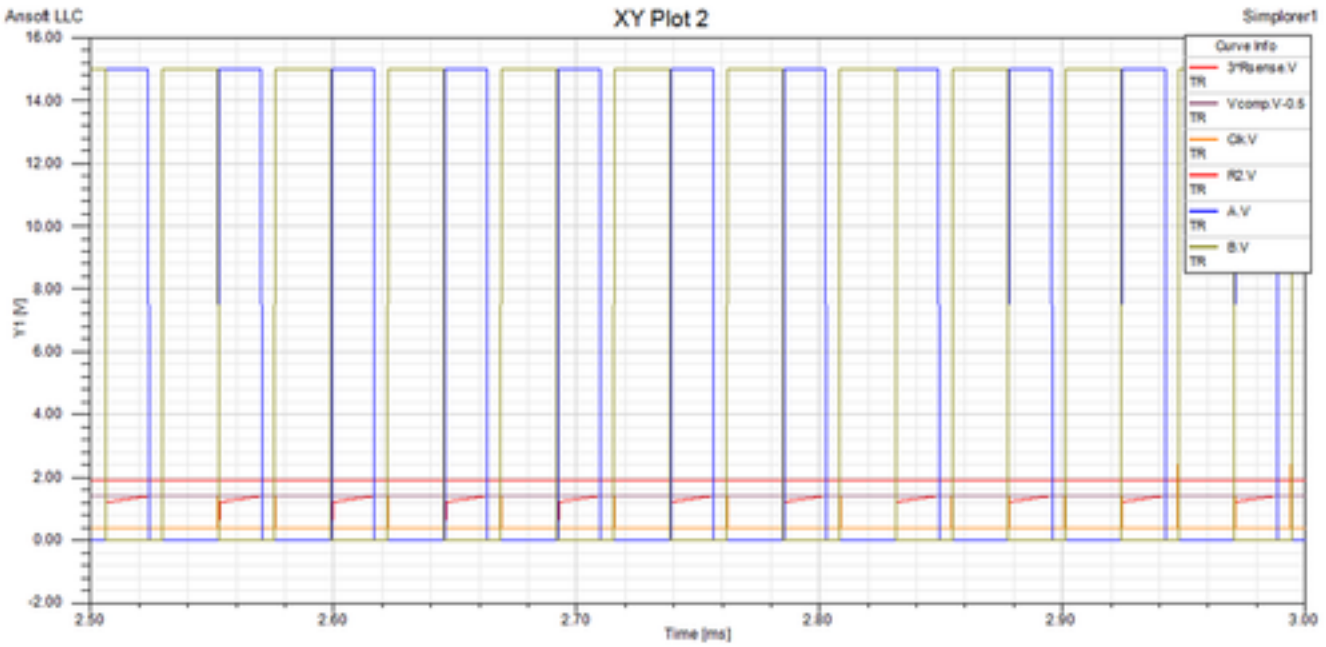


Red: inductor current

Blue: load current (right scale, in Amps), load voltage (left scale, in Volts)

Figure 3. Simulation results(a)



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Red: current sense resistor voltage * 3

Blue: A output voltage

Green: B output voltage

Orange: clock

Purple: error amplifier output voltage - 0.5V

Figure 4. Simulation results(b)

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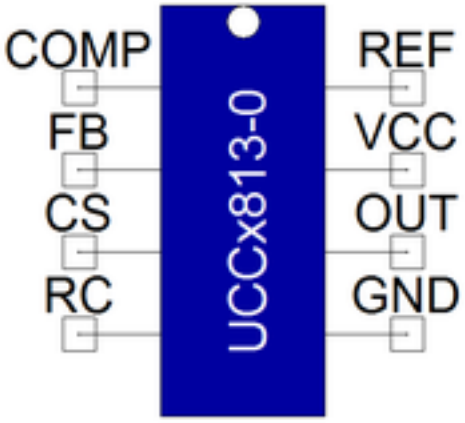
UCCx813_0: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCC3813-0/-1/-2/-3/-4/-5* family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the *UC3842/3/4/5* family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

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The *UCC3813-0/-1/-2/-3/-4/-5* family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the *UCC3813-3* and *UCC3813-5* fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the *UCC3813-2* and *UCC3813-4* make these ideal choices for use in off-line power supplies.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite. An ideal switch controlled by the main state machine models the leading-edge filtering disconnecting the voltmeter of the pin during the 100ns after a switching occurs.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It gets connected to ground through a 5k resistor if the power input falls below the under-voltage value.
• Power input: limited to 13.5V using a zener diode.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 6.9V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Conservative Pins

Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin

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Vref	Voltage reference
Vcc	Power input
OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -40°C ≤ TA ≤ +85°C for UCC2813-x; 0°C ≤ TA ≤ +70°C for UCC3813-x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx813-0	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
Load Regulation	0.2mA<I<5mA	10-30	0	mV
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz,T_J=+25°C (N. 9)	130	0	µV
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	0	mV
Output Short Circuit		-5 / -35	X	mA
Oscillator Section				
Oscillator Frequency	(Note 4)	46	46	kHz
Temperature Stability	(Note 9)	2.5	0	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.5	V
Error Amplifier Section				
Input Voltage	COMP=2.5V;	2.5	2.5	V
Input Bias Current		-2/2	0	µA
Open Loop Voltage Gain		80	80	dB

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COMP Sink Current	FB=2.7V, COMP=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle		99	99	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0	V
	I=200mA, allparts	0.35	0	V
	I=20mA, VCC=0V, all parts	0.7	0	V
OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0	V
	I=-200mA, allparts	1.0	0	V
Rise Time	CL=1nF	41	X	ns
Fall Time	CL=1nF	44	X	ns
Undervoltage Lockout Section				
Start Threshold (Note 8)		7.2	7.2	V
Stop Threshold (Note 8)		6.9	6.9	V
Start to Stop Hysteresis		0.3	0.3	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Cur-	FB=0V, CS=0V	0.5	0	mA

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rent				
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	CS=0V	1.0	1.0	V

X: not modeled
Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx813-0, UCCx813-2 and UCCx813-3 is the output frequency. Oscillator frequency for the UCCx813-1, UCCx813-4 and UCCx813-5 is twice the output frequency.
Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤ Vcs ≤ 0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.

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Examples

Example circuit :

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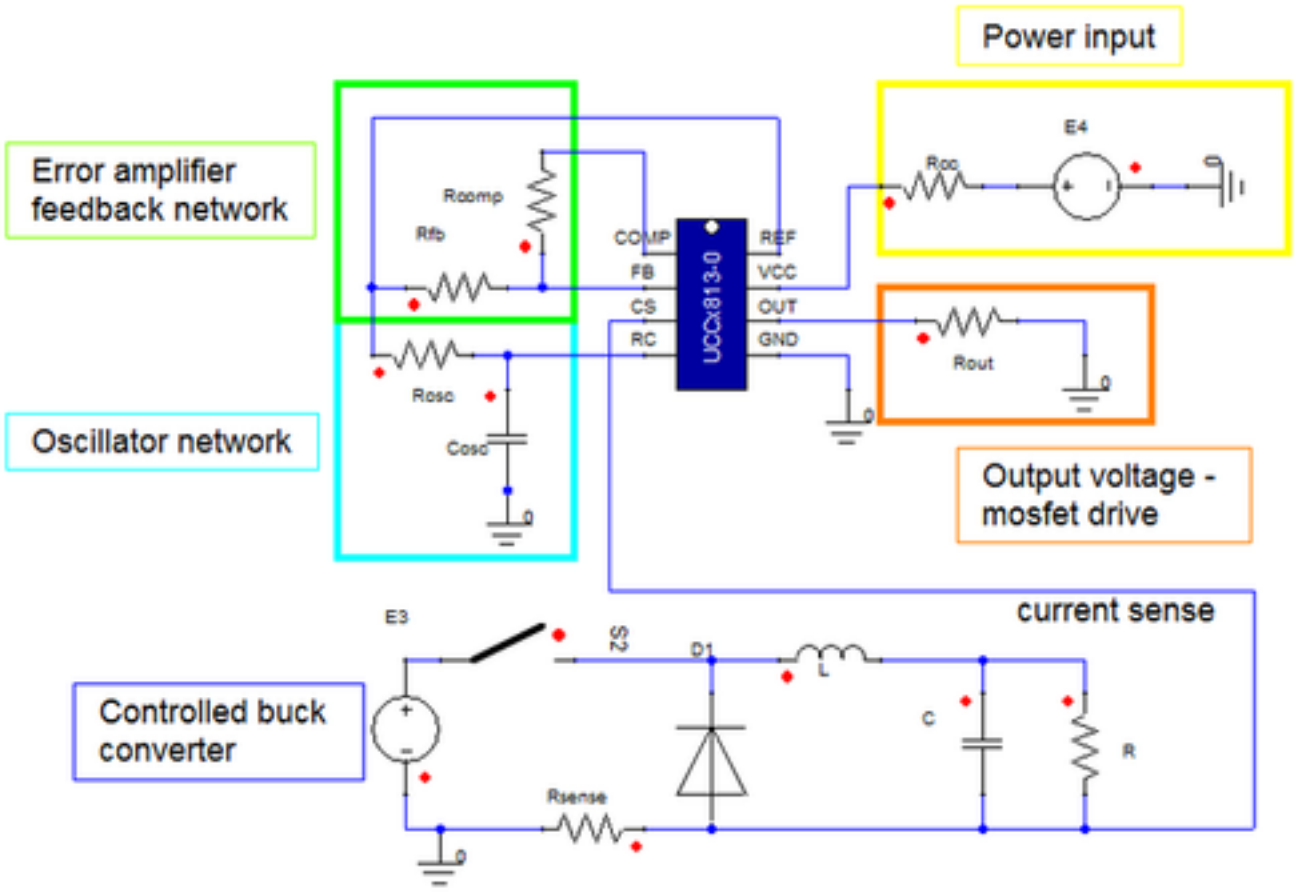

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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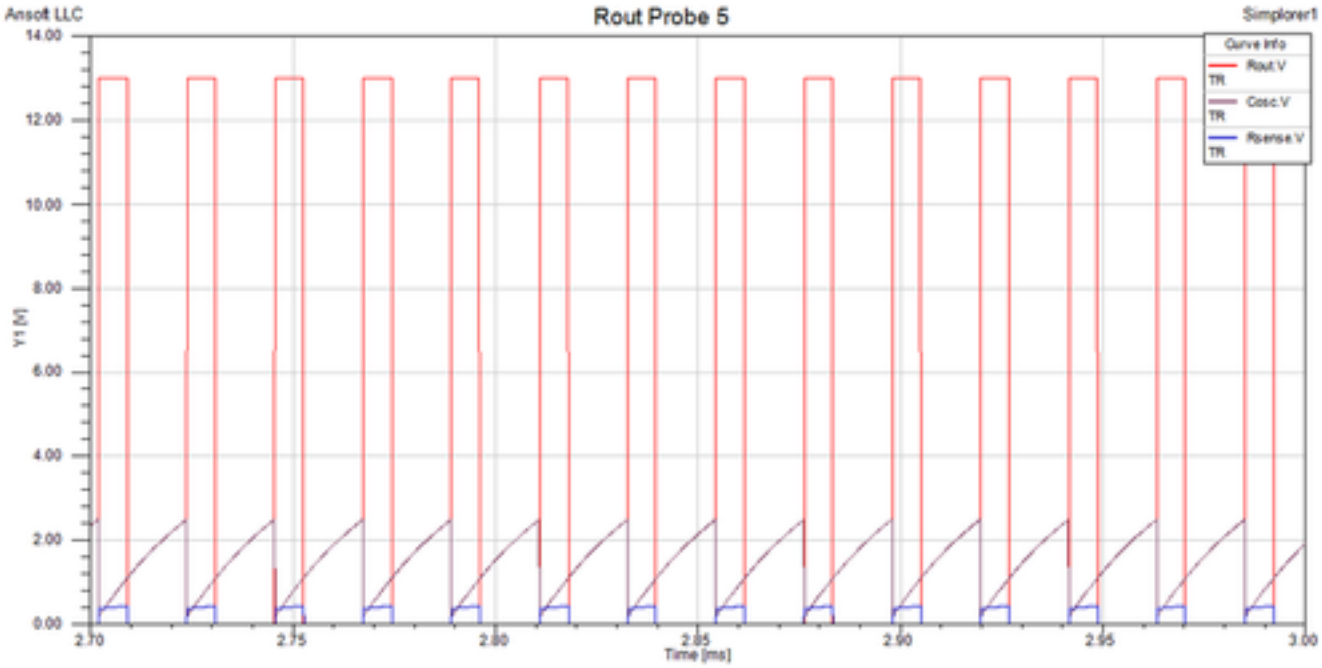

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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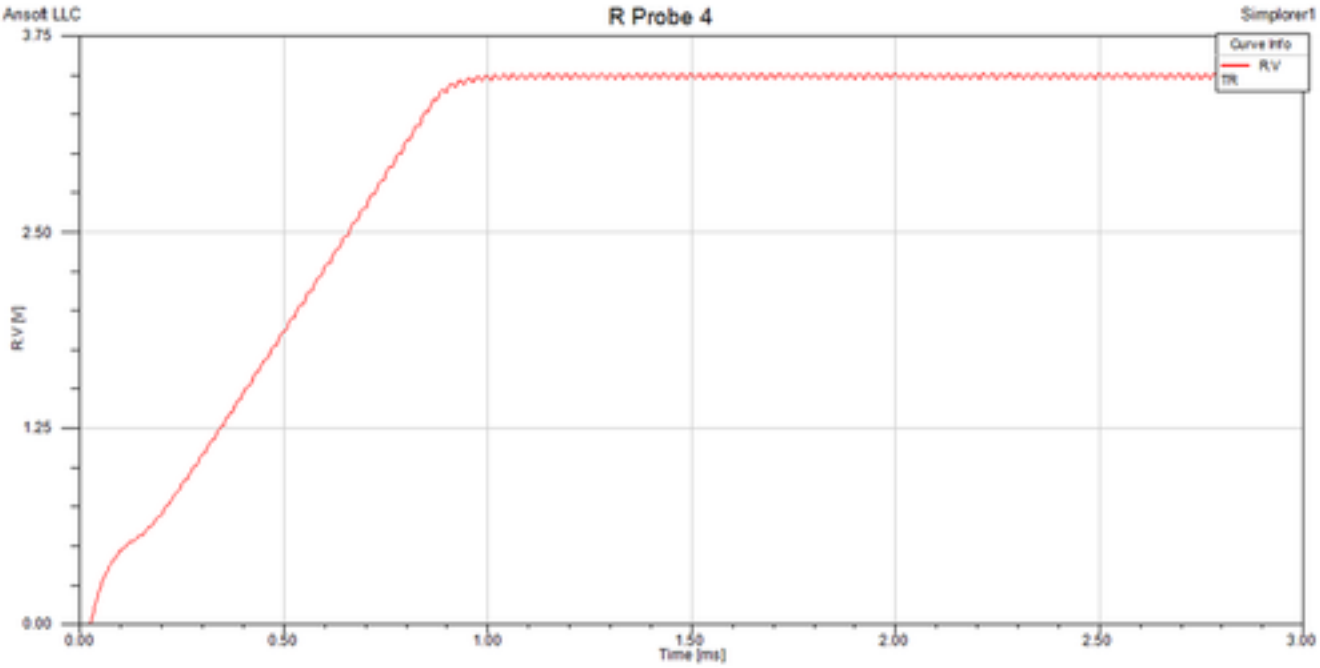

Red: converter output voltage. Note the ramp generated by the soft-start circuitry.

Figure 4. Simulation results(b)

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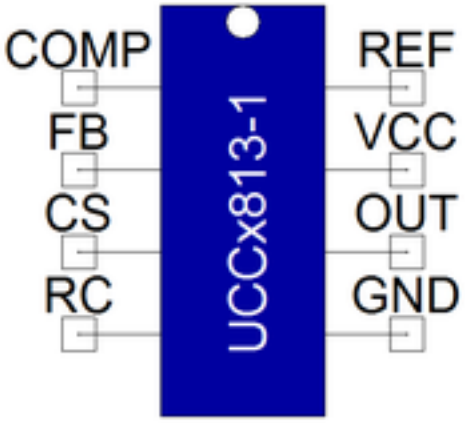
UCCx813_1: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCC3813-0/-1/-2/-3/-4/-5* family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the *UC3842/3/4/5* family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

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The *UCC3813-0/-1/-2/-3/-4/-5* family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the *UCC3813-3* and *UCC3813-5* fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the *UCC3813-2* and *UCC3813-4* make these ideal choices for use in off-line power supplies.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite. An ideal switch controlled by the main state machine models the leading-edge filtering disconnecting the voltmeter of the pin during the 100ns after a switching occurs.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It gets connected to ground through a 5k resistor if the power input falls below the under-voltage value.
• Power input: limited to 13.5V using a zener diode.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 7.4V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin

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Vref	Voltage reference
Vcc	Power input
OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -40°C ≤ TA ≤ +85°C for UCC2813-x; 0°C ≤ TA ≤ +70°C for UCC3813-x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx813-1	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
Load Regulation	0.2mA<I<5mA	10-30	0	mV
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz,T_J =+25°C (N. 9)	130	0	µV
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	0	mV
Output Short Circuit		-5 / -35	X	mA
Oscillator Section				
Oscillator Frequency	(Note 4)	46	46	kHz
Temperature Stability	(Note 9)	2.5	0	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.5	V

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Error Amplifier Section				
Input Voltage	COMP=2.5V;	2.5	2.5	V
Input Bias Current		-2/2	0	µA
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle		49	49	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0	V
	I=200mA, allparts	0.35	0	V
	I=20mA, VCC-C=0V, all parts	0.7	0	V
OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0	V
	I=-200mA, allparts	1.0	0	V
Rise Time	CL=1nF	41	X	ns
Fall Time	CL=1nF	44	X	ns
Undervoltage Lockout Section				

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Start Threshold (Note 8)		9.4	9.4	V
Stop Threshold (Note 8)		7.4	7.4	V
Start to Stop Hysteresis		2.0	2.0	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	CS=0V	1.0	1.0	V

X: not modeled
Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx813-0, UCCx813-2 and UCCx813-3 is the output frequency. Oscillator frequency for the UCCx813-1, UCCx813-4 and UCCx813-5 is twice the output frequency.
Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤ Vcs ≤ 0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.

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Examples

Example circuit :

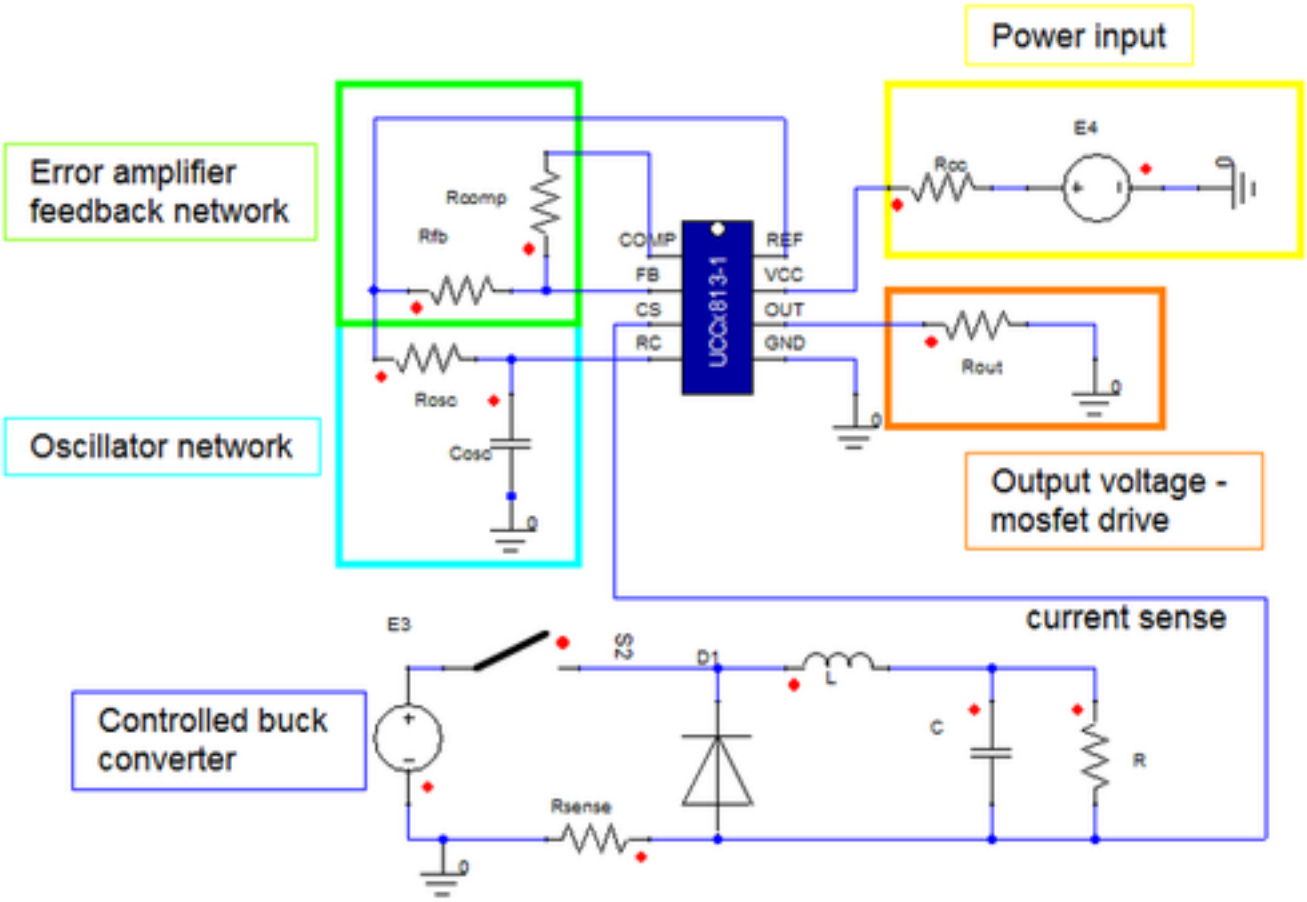

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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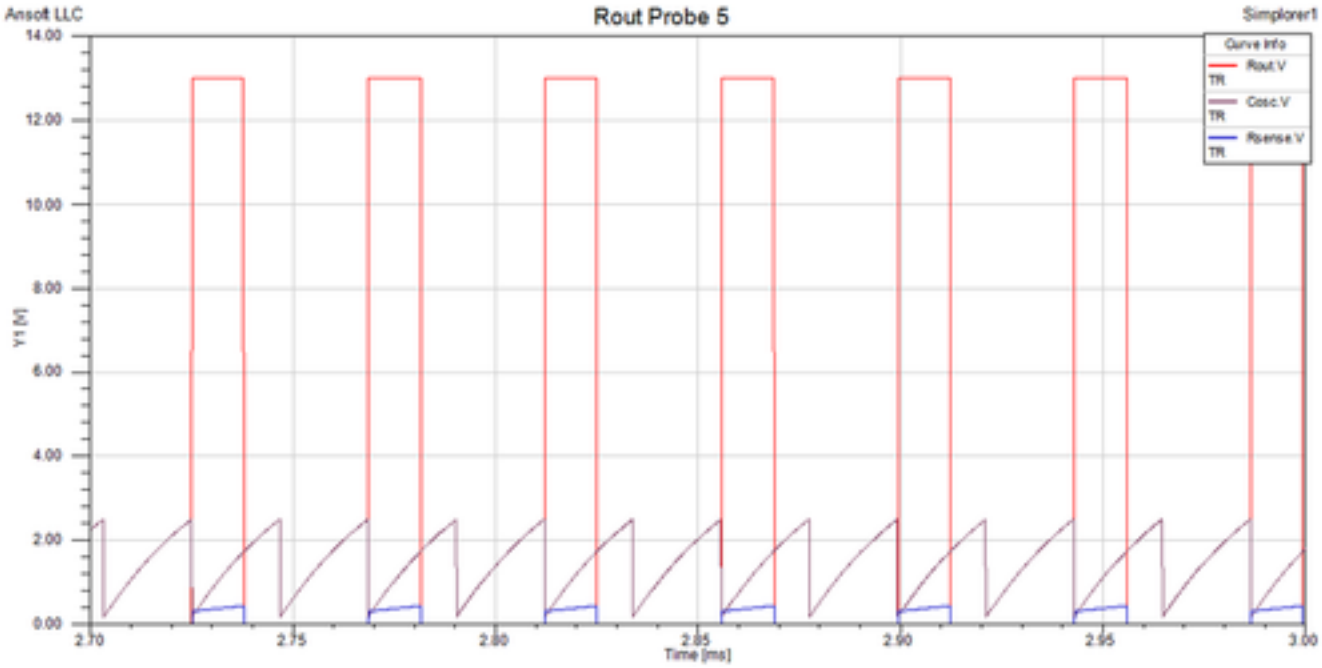

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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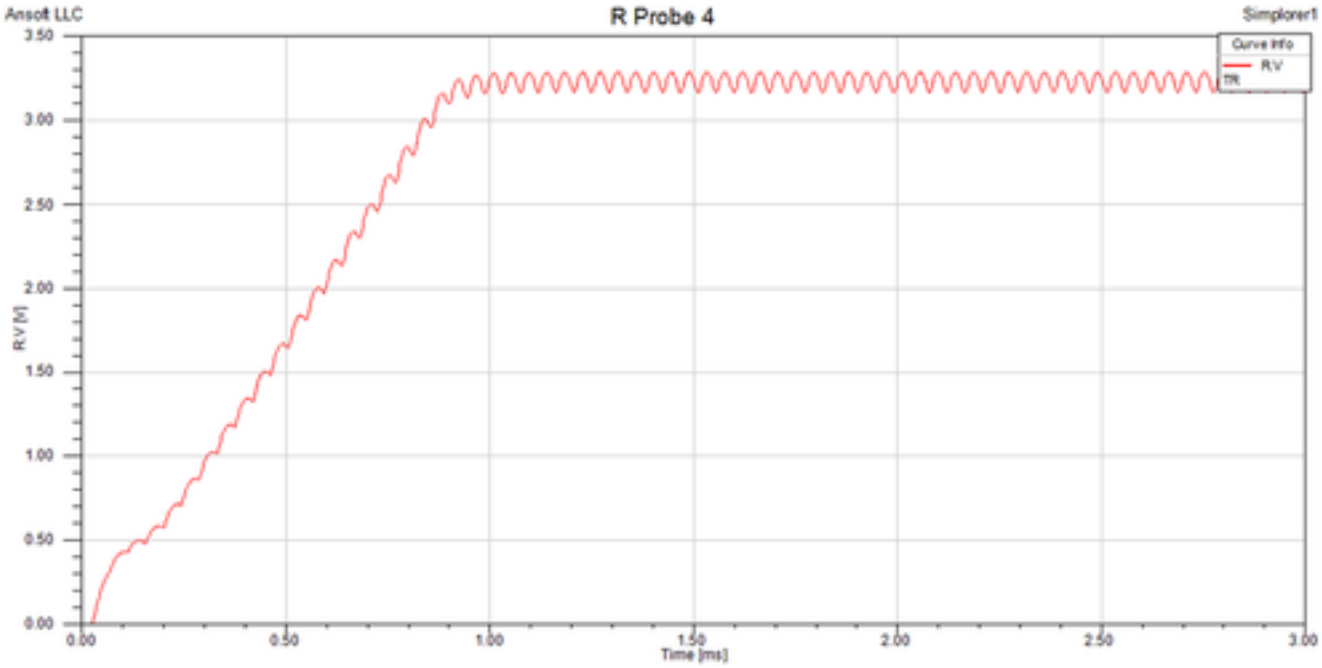

Red: converter output voltage. Note the ramp generated by the soft-start circuitry.

Figure 4. Simulation results(b)

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References

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UCCx813_2: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

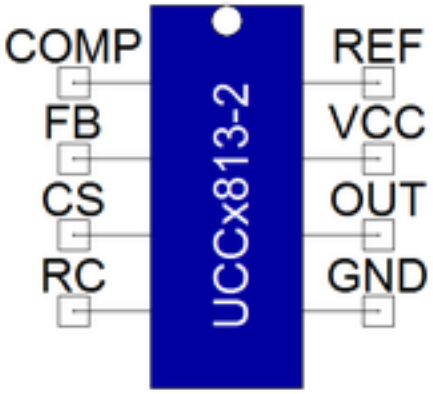

Figure 1. Component symbol

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Description

The *UCC3813-0/-1/-2/-3/-4/-5* family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the *UC3842/3/4/5* family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

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The *UCC3813-0/-1/-2/-3/-4/-5* family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the *UCC3813-3* and *UCC3813-5* fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the *UCC3813-2* and *UCC3813-4* make these ideal choices for use in off-line power supplies.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite. An ideal switch controlled by the main state machine models the leading-edge filtering disconnecting the voltmeter of the pin during the 100ns after a switching occurs.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It gets connected to ground through a 5k resistor if the power input falls below the under-voltage value.
• Power input: limited to 13.5V using a zener diode.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 8.3V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Conservative Pins

Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vcc	Power input
OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -40°C ≤ TA ≤ +85°C for UCC2813-x; 0°C ≤ TA ≤ +70°C for UCC3813-x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx813-2	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
Load Regulation	0.2mA<I<5mA	10-30	0	mV
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz,T_J =+25°C (N. 9)	130	0	µV
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	0	mV

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Output Short Circuit		-5 / -35	X	mA
Oscillator Section				
Oscillator Frequency	(Note 4)	46	46	kHz
Temperature Stability	(Note 9)	2.5	0	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.5	V
Error Amplifier Section				
Input Voltage	COMP=2.5V;	2.5	2.5	V
Input Bias Current		-2/2	0	µA
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle		99	99	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low	I=20mA, allparts	0.1	0	V

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Level				
	I=200mA, allparts	0.35	0	V
	I=20mA, VCC-C=0V, all parts	0.7	0	V
OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0	V
	I=-200mA, allparts	1.0	0	V
Rise Time	CL=1nF	41	X	ns
Fall Time	CL=1nF	44	X	ns
Undervoltage Lockout Section				
Start Threshold (Note 8)		12.5	12.5	V
Stop Threshold (Note 8)		8.3	8.3	V
Start to Stop Hysteresis		4.2	4.2	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	CS=0V	1.0	1.0	V

X: not modeled
Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx813-0, UCCx813-2 and UCCx813-3 is the output

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frequency. Oscillator frequency for the UCCx813-1, UCCx813-4 and UCCx813-5 is twice the output frequency.
Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤ Vcs ≤ 0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.

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Example circuit :

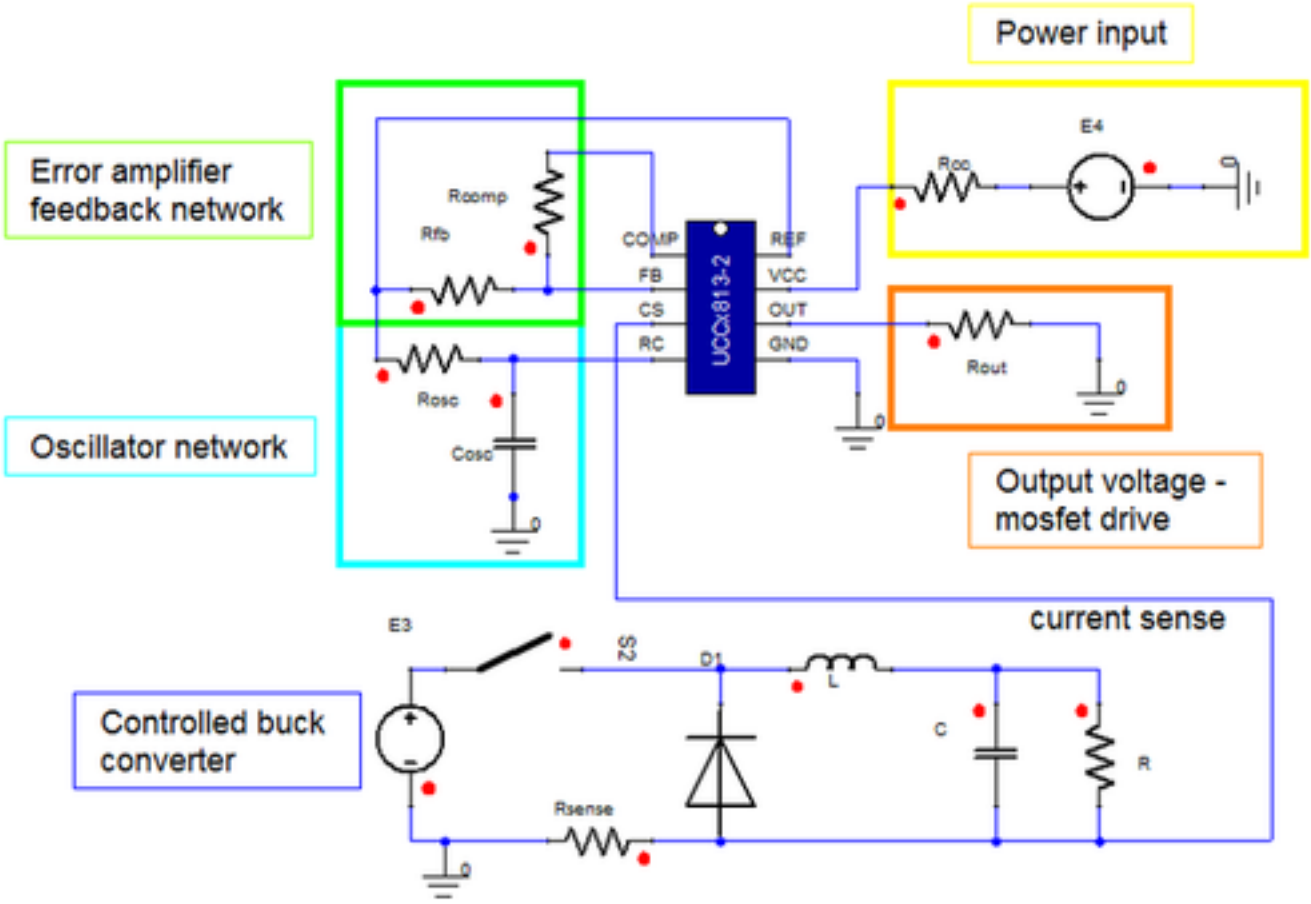

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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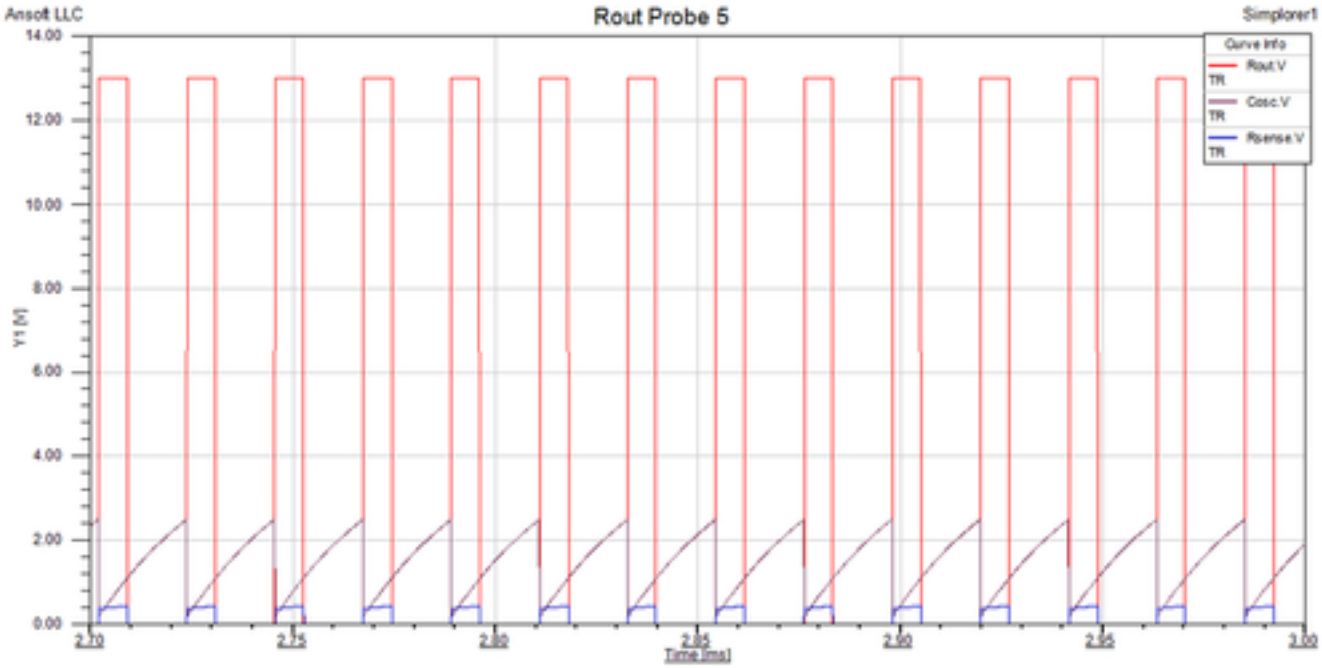

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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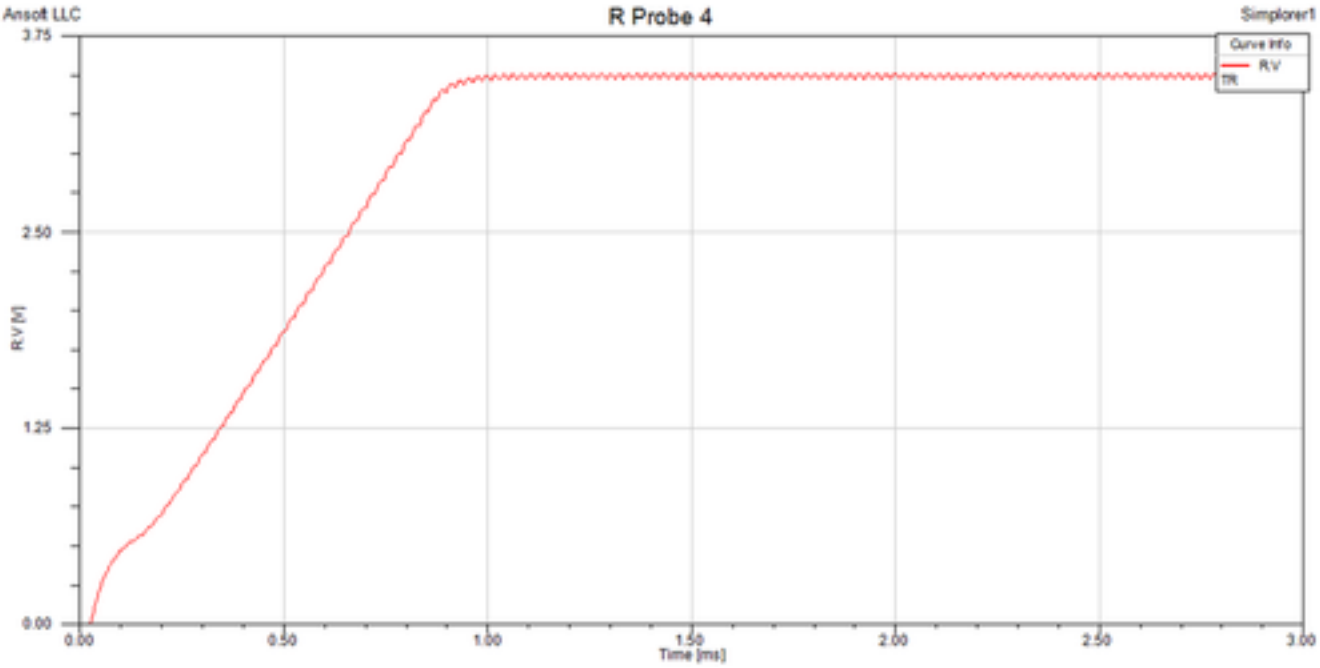

Red: converter output voltage. Note the ramp generated by the soft-start circuitry.

Figure 4. Simulation results(b)

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References

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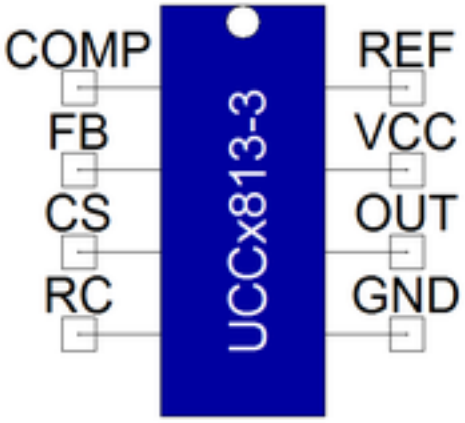
UCCx813_3: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCC3813-0/-1/-2/-3/-4/-5* family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the *UC3842/3/4/5* family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

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The *UCC3813-0/-1/-2/-3/-4/-5* family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the *UCC3813-3* and *UCC3813-5* fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the *UCC3813-2* and *UCC3813-4* make these ideal choices for use in off-line power supplies.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite. An ideal switch controlled by the main state machine models the leading-edge filtering disconnecting the voltmeter of the pin during the 100ns after a switching occurs.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It gets connected to ground through a 5k resistor if the power input falls below the under-voltage value.
• Power input: limited to 13.5V using a zener diode.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 3.6V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Conservative Pins

Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin

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Vref	Voltage reference
Vcc	Power input
OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -40°C ≤ TA ≤ +85°C for UCC2813-x; 0°C ≤ TA ≤ +70°C for UCC3813-x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx813-3	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	4.00	4.00	V
Load Regulation	0.2mA<I<5mA	10-30	0	mV
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz,T_J =+25°C (N. 9)	130	0	µV
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	0	mV
Output Short Circuit		-5 / -35	X	mA
Oscillator Section				
Oscillator Frequency	(Note 4)	31	32	kHz
Temperature Stability	(Note 9)	2.5	0	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.5	V

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Error Amplifier Section				
Input Voltage	COMP=2.5V;	2.0	2.0	V
Input Bias Current		-2/2	0	µA
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle		99	99	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0	V
	I=200mA, allparts	0.35	0	V
	I=20mA, VCC-C=0V, all parts	0.7	0	V
OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0	V
	I=-200mA, allparts	1.0	0	V
Rise Time	CL=1nF	41	X	ns
Fall Time	CL=1nF	44	X	ns
Undervoltage Lockout Section				

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Start Threshold (Note 8)		4.1	4.1	V
Stop Threshold (Note 8)		3.6	3.6	V
Start to Stop Hysteresis		0.5	0.5	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	CS=0V	1.0	1.0	V

X: not modeled
Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx813-0, UCCx813-2 and UCCx813-3 is the output frequency. Oscillator frequency for the UCCx813-1, UCCx813-4 and UCCx813-5 is twice the output frequency.
Note 5: Gain is defined by: $A=\Delta Vcomp/\Delta Vcs$, $0 \le Vcs \le 0.8$
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
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Note 9: Guaranteed by design. Not 100% tested in production.

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Input/Output Quantities

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Examples

Example circuit :

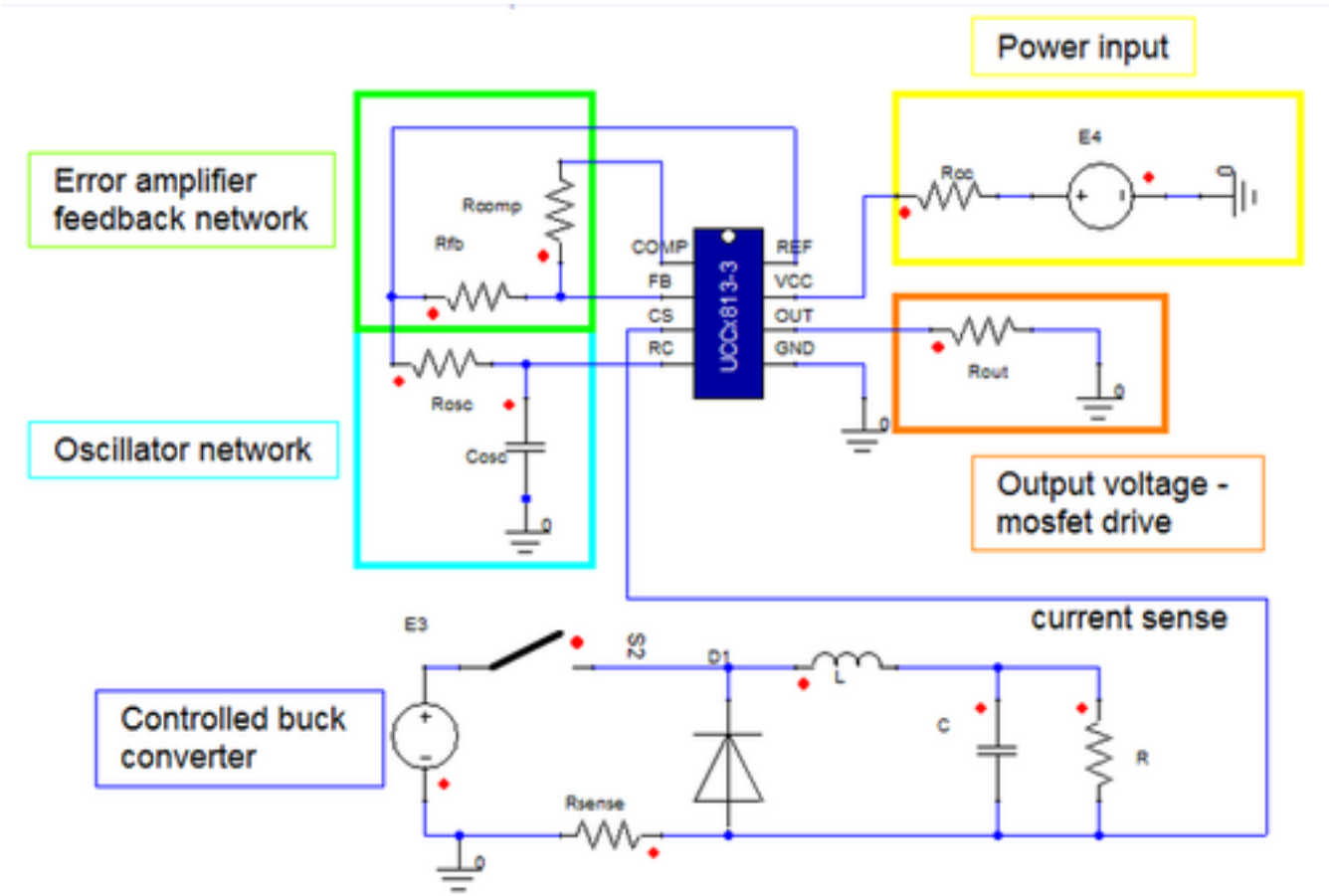

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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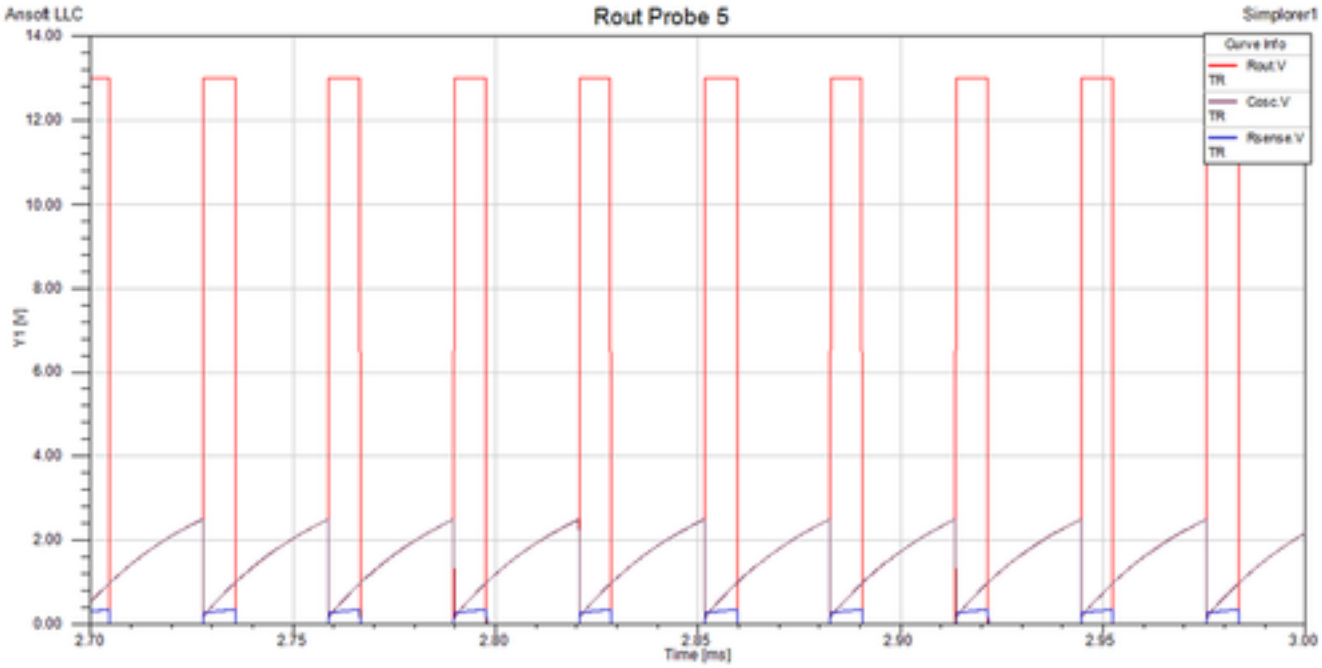

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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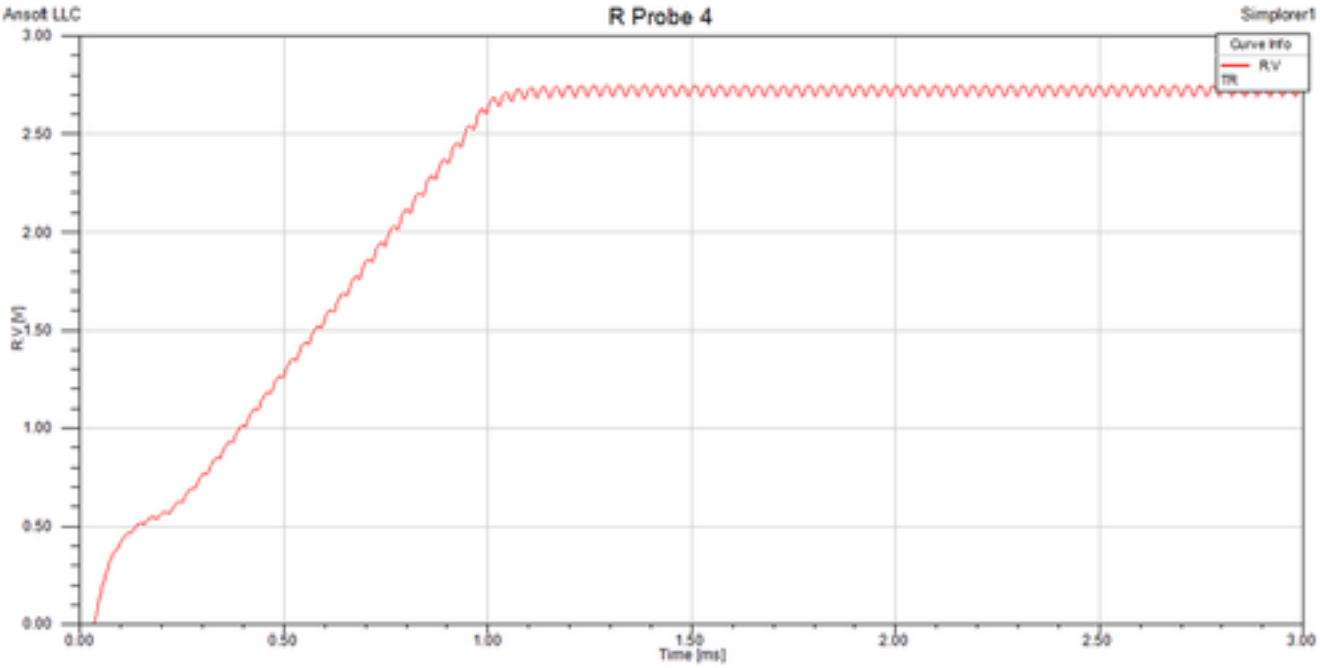

Red: converter output voltage. Note the ramp generated by the soft-start circuitry.

Figure 4. Simulation results(b)

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References

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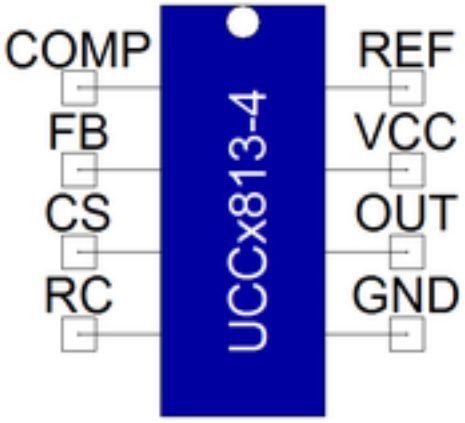
UCCx813_4: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

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The *UCC3813-0/-1/-2/-3/-4/-5* family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the *UCC3813-3* and *UCC3813-5* fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the *UCC3813-2* and *UCC3813-4* make these ideal choices for use in off-line power supplies.

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• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite. An ideal switch controlled by the main state machine models the leading-edge filtering disconnecting the voltmeter of the pin during the 100ns after a switching occurs.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It gets connected to ground through a 5k resistor if the power input falls below the under-voltage value.
• Power input: limited to 13.5V using a zener diode.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 8.3V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Conservative Pins

Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin

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Vref	Voltage reference
Vcc	Power input
OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -40°C ≤ TA ≤ +85°C for UCC2813-x; 0°C ≤ TA ≤ +70°C for UCC3813-x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx813-4	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	5.00	5.00	V
Load Regulation	0.2mA<I<5mA	10-30	0	mV
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz,T_J =+25°C (N. 9)	130	0	µV
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	0	mV
Output Short Circuit		-5 / -35	X	mA
Oscillator Section				
Oscillator Frequency	(Note 4)	46	46	kHz
Temperature Stability	(Note 9)	2.5	0	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.5	V

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Error Amplifier Section				
Input Voltage	COMP=2.5V;	2.5	2.5	V
Input Bias Current		-2/2	0	µA
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle		49	49	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0	V
	I=200mA, allparts	0.35	0	V
	I=20mA, VCC-C=0V, all parts	0.7	0	V
OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0	V
	I=-200mA, allparts	1.0	0	V
Rise Time	CL=1nF	41	X	ns
Fall Time	CL=1nF	44	X	ns
Undervoltage Lockout Section				

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Start Threshold (Note 8)		9.4	9.4	V
Stop Threshold (Note 8)		7.4	7.4	V
Start to Stop Hysteresis		2.0	2.0	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	CS=0V	1.0	1.0	V

X: not modeled
Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx813-0, UCCx813-2 and UCCx813-3 is the output frequency. Oscillator frequency for the UCCx813-1, UCCx813-4 and UCCx813-5 is twice the output frequency.
Note 5: Gain is defined by: A=ΔVcomp/ΔVcs, 0 ≤ Vcs ≤ 0.8
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.

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Examples

Example circuit :

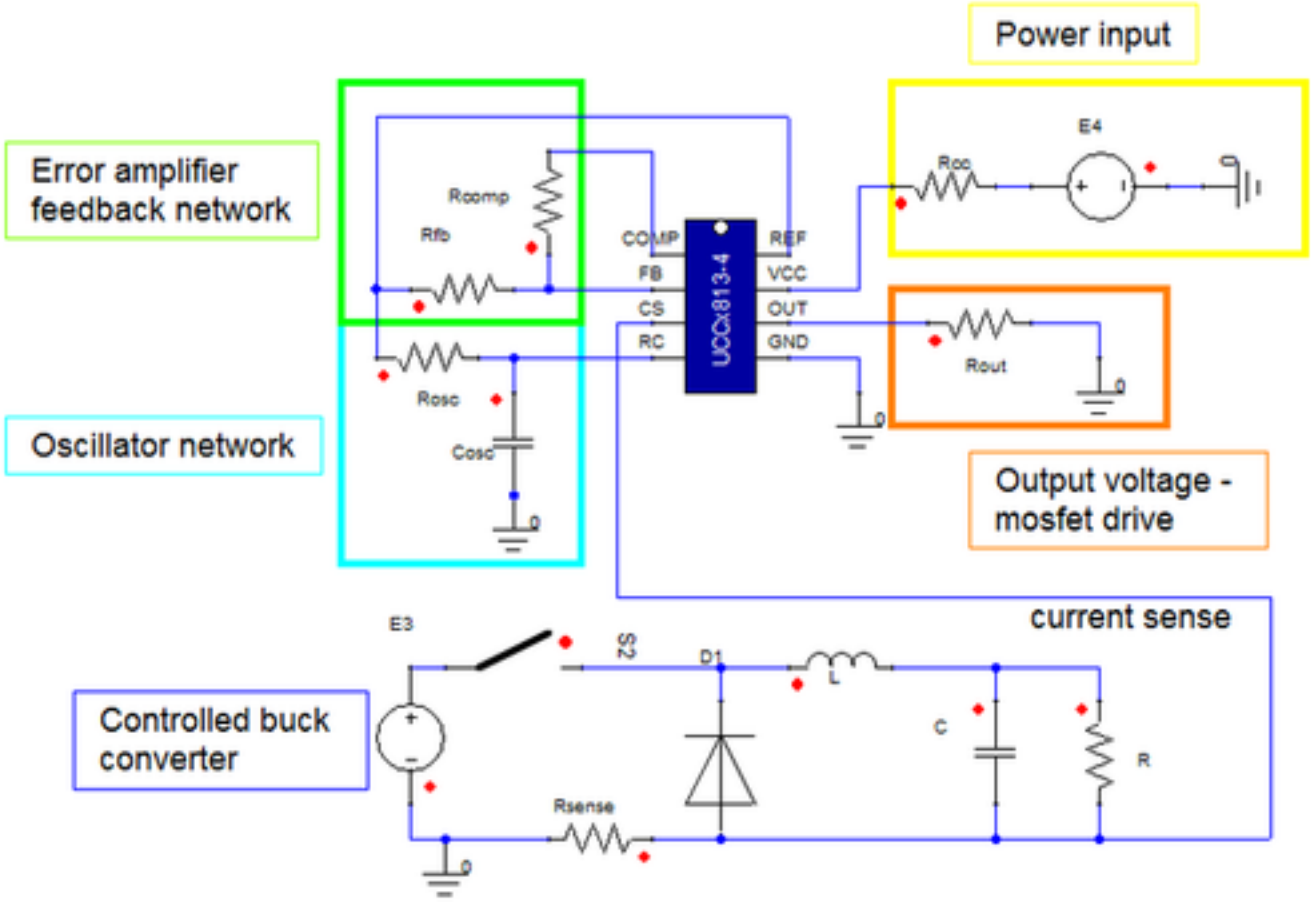

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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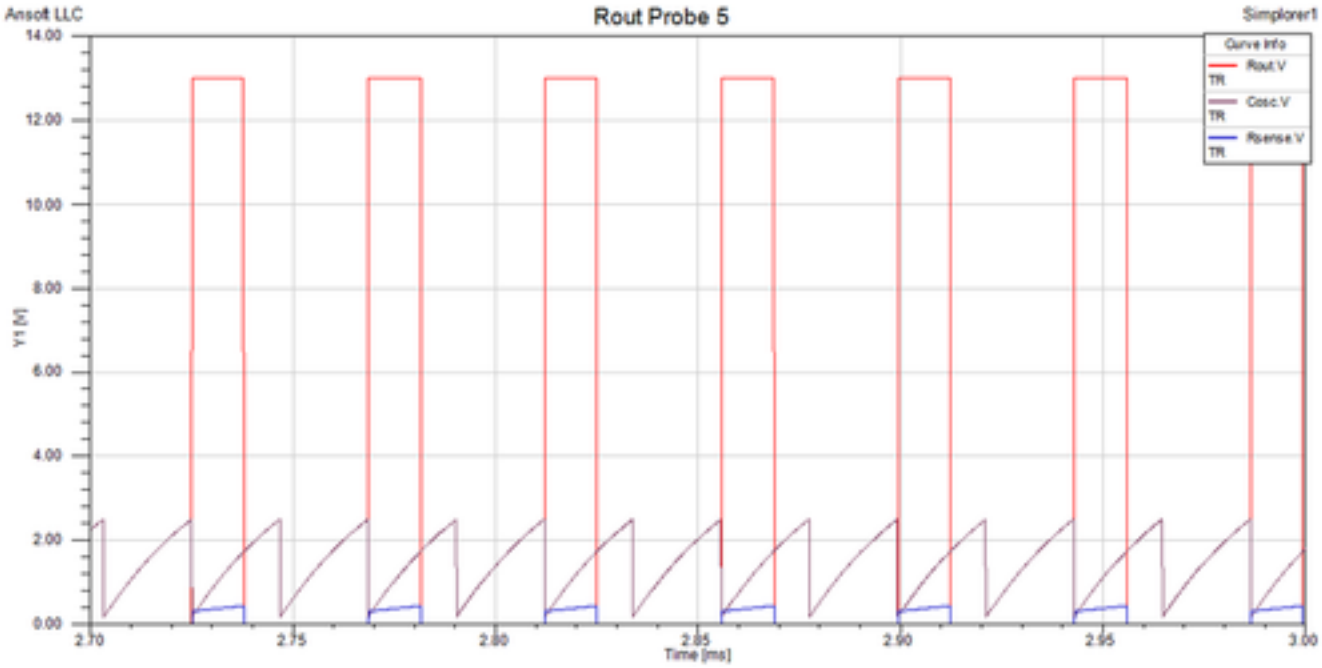

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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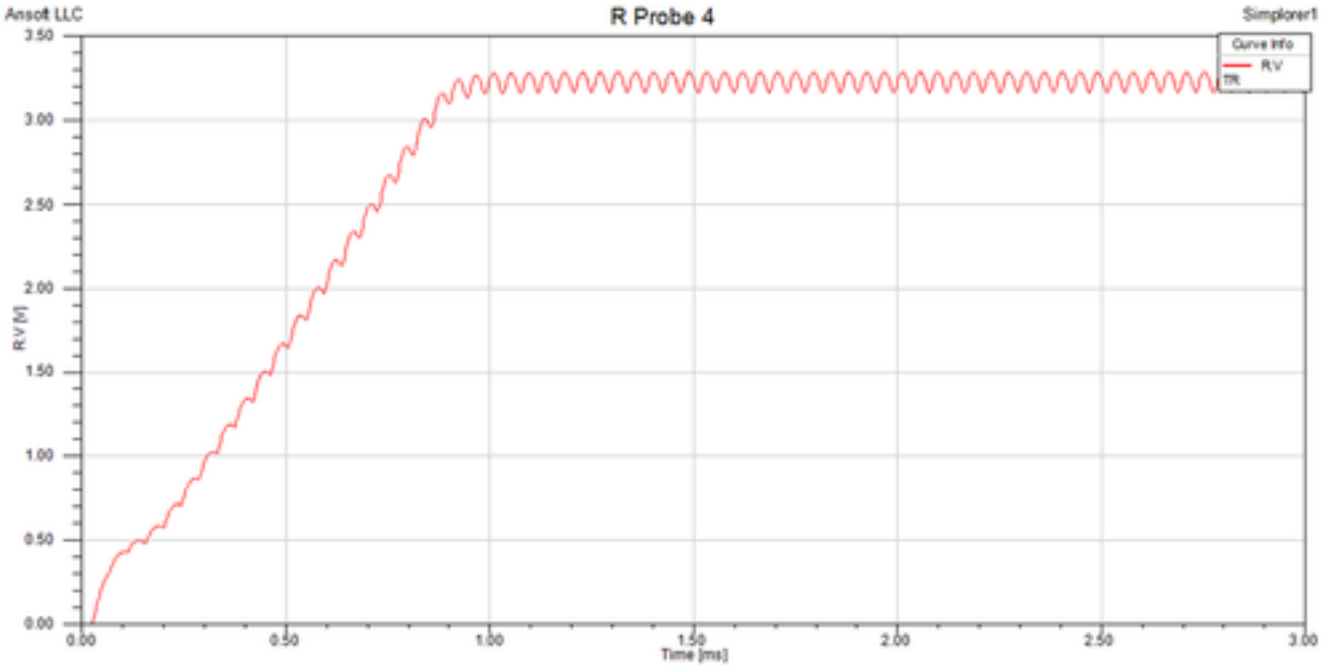

Red: converter output voltage. Note the ramp generated by the soft-start circuitry.

Figure 4. Simulation results(b)

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References

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UCCx813_5: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

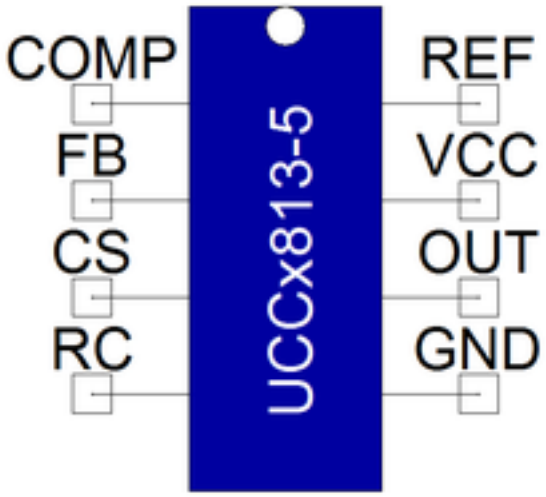

Figure 1. Component symbol

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Description

The *UCC3813-0/-1/-2/-3/-4/-5* family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the *UC3842/3/4/5* family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

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The *UCC3813-0/-1/-2/-3/-4/-5* family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the *UCC3813-3* and *UCC3813-5* fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the *UCC3813-2* and *UCC3813-4* make these ideal choices for use in off-line power supplies.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite. An ideal switch controlled by the main state machine models the leading-edge filtering disconnecting the voltmeter of the pin during the 100ns after a switching occurs.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It gets connected to ground through a 5k resistor if the power input falls below the under-voltage value.
• Power input: limited to 13.5V using a zener diode.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 3.6V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Conservative Pins

Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin

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Vref	Voltage reference
Vcc	Power input
OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for -40°C ≤ TA ≤ +85°C for UCC2813-x; 0°C ≤ TA ≤ +70°C for UCC3813-x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1 F capacitor from VREF to GND. TA=TJ.

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx813-5	MODEL	UNITS
Reference Section				
Output Voltage	T_J=+25°C,- ,I=0.2mA, UCCx800/1/2/4	4.00	4.00	V
Load Regulation	0.2mA<I<5mA	10-30	0	mV
Total Variation	UCCx800/1/2/4 (Note 7)	5.00	5.00	V
Output Noise Voltage	10Hz ≤f ≤10kHz,T_J =+25°C (N. 9)	130	0	µV
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)	5	0	mV
Output Short Circuit		-5 / -35	X	mA
Oscillator Section				
Oscillator Frequency	(Note 4)	31	32	kHz
Temperature Stability	(Note 9)	2.5	0	%
Amplitude peak-to-peak		2.4	2.4	V
Oscillator Peak Voltage		2.45	2.5	V

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Error Amplifier Section				
Input Voltage	COMP=2.5V;	2.5	2.5	V
Input Bias Current		-2/2	0	µA
Open Loop Voltage Gain		80	80	dB
COMP Sink Current	FB=2.7V, COMP-P=1.1V	2.0	X	mA
COMP Source Current	FB=1.8V, COMP-P=REF-1.2V	-0.5	X	mA
Gain Bandwidth Product	(Note 9)	2	X	MHz
PWM Section				
Maximum Duty Cycle		49	49	%
Minimum Duty Cycle	COMP=0V	0	0	%
Current Sense Section				
Gain	(Note 5)	1.65	1.65	V/V
Maximum Input Signal	COMP=5V (Note 6)	1.0	1.0	V
Input Bias Current		-200/200	X	nA
CS Blank Time		100	100	ns
Over-Current Threshold		1.55	1.55	V
COMP to CS Offset	CS=0V	0.9	X	V
Output Section				
OUT Low Level	I=20mA, allparts	0.1	0	V
	I=200mA, allparts	0.35	0	V
	I=20mA, VCC-C=0V, all parts	0.7	0	V
OUT High V_{SAT} (Vcc-OUT)	I=-20mA, allparts	0.15	0	V
	I=-200mA, allparts	1.0	0	V
Rise Time	CL=1nF	41	X	ns
Fall Time	CL=1nF	44	X	ns
Undervoltage Lockout Section				

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Start Threshold (Note 8)		4.1	4.1	V
Stop Threshold (Note 8)		3.6	3.6	V
Start to Stop Hysteresis		0.5	0.5	V
Soft Start Section				
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V	4	4	ms
Overall Section				
Start-up Current	VCC < StartThreshold	0.1	X	mA
Operating Supply Current	FB=0V, CS=0V	0.5	0	mA
Vcc Internal Zener Voltage	ICC=10mA (Note 8), (Note 10)	13.5	13.5	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	CS=0V	1.0	1.0	V

X: not modeled
Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx813-0, UCCx813-2 and UCCx813-3 is the output frequency. Oscillator frequency for the UCCx813-1, UCCx813-4 and UCCx813-5 is twice the output frequency.
Note 5: Gain is defined by: $A=\Delta Vcomp/\Delta Vcs$, $0 \le Vcs \le 0.8$
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.

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Input/Output Quantities

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Examples

Example circuit :

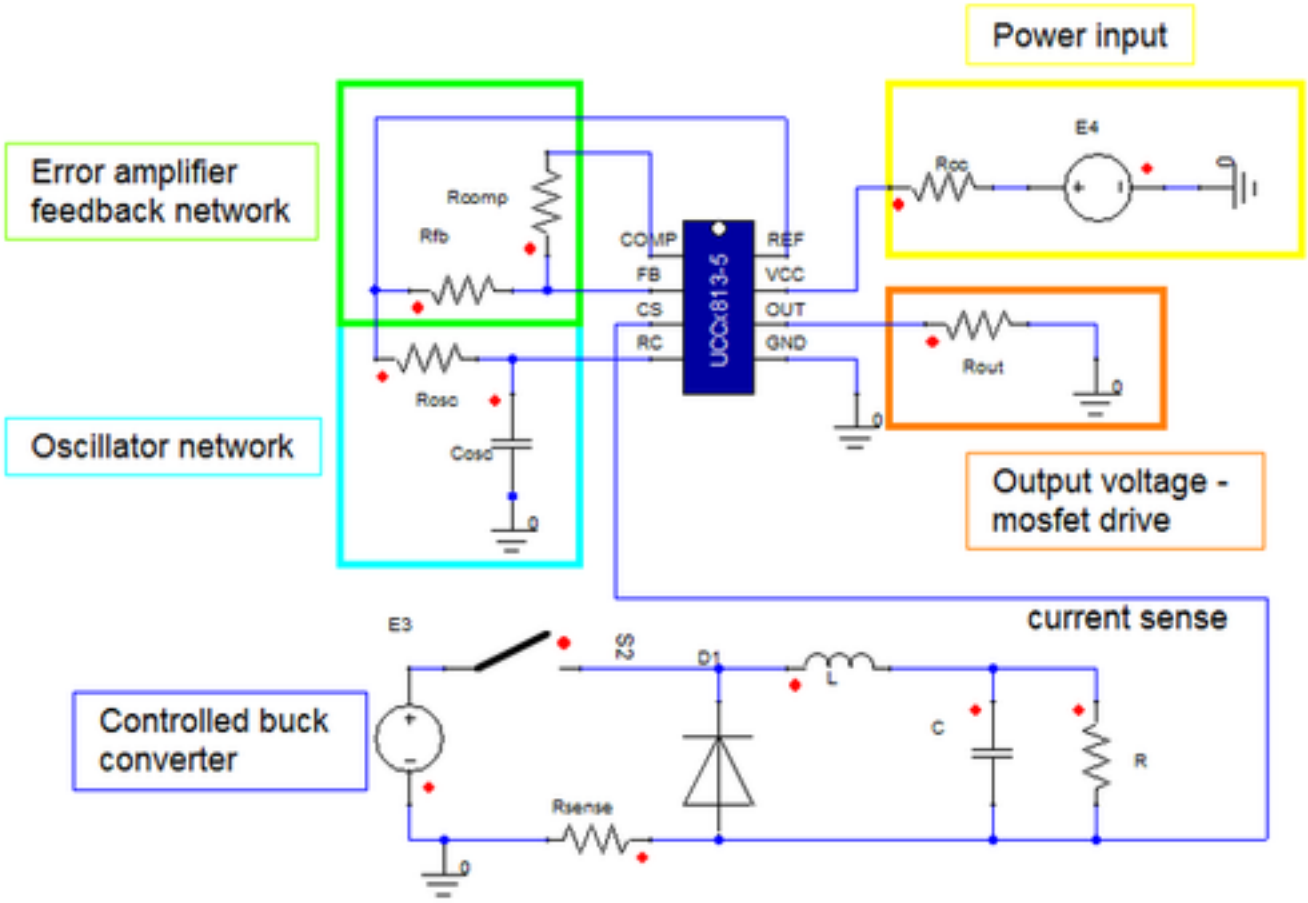

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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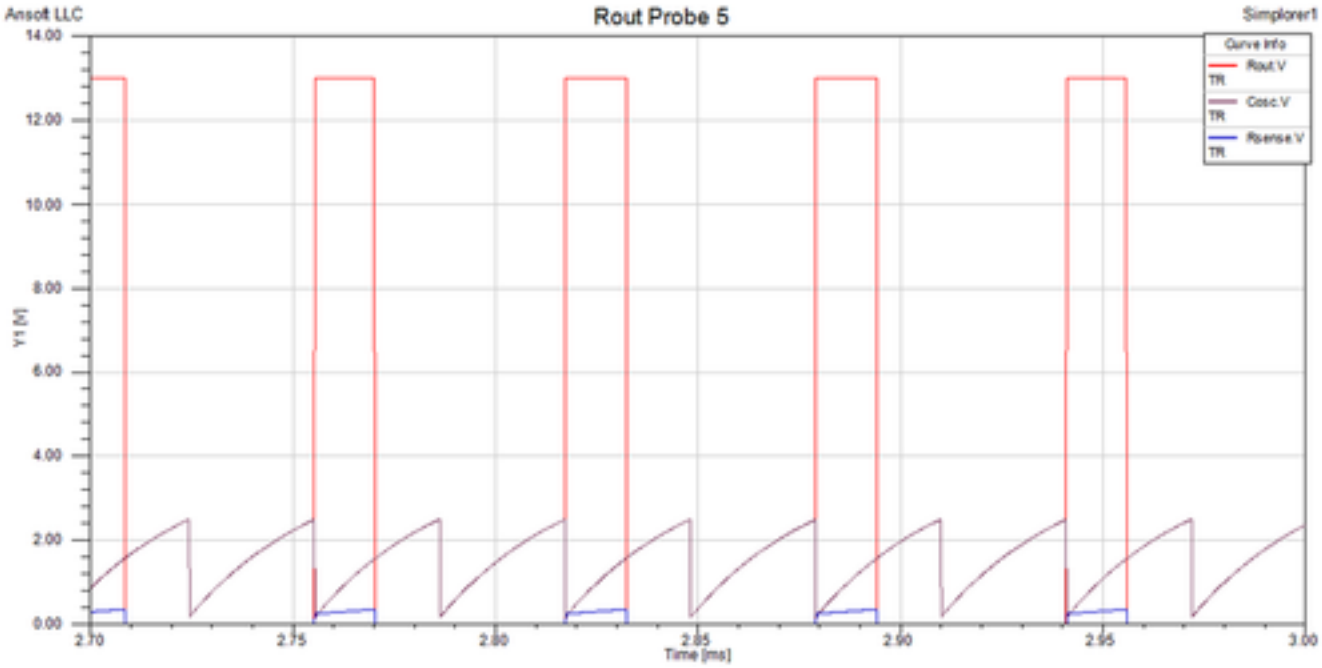

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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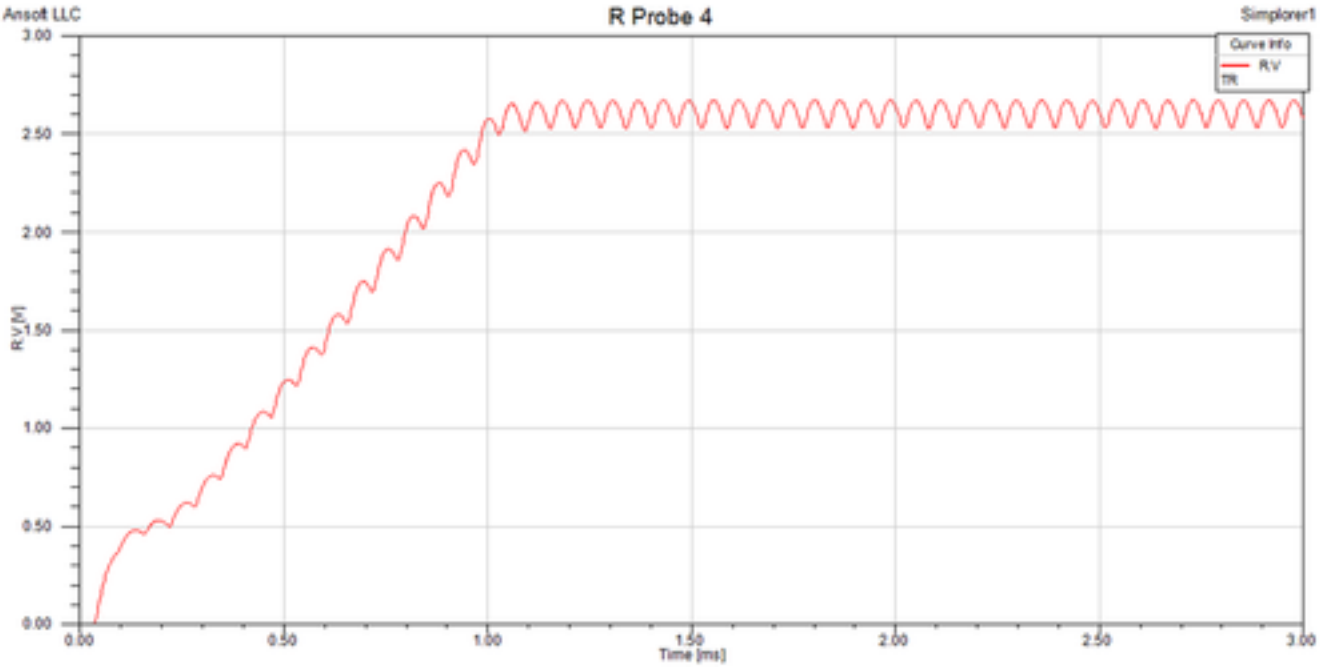

Red: converter output voltage. Note the ramp generated by the soft-start circuitry.

Figure 4. Simulation results(b)

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References

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UCCx895: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

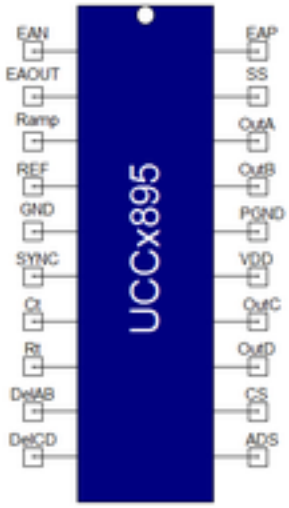

Figure 1. Component symbol

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Description

The *UCCx895* is a phase shift PWM controller that implements control of a full-bridge power stage by phase shifting the switching of one half-bridge with respect to the other. It allows constant frequency pulse-width modulation in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The part can be used either as a voltage mode or current mode controller.

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While the *UCCx895* maintains the functionality of the *UCx875/6/7/8* family and *UCx879*, it improves on that controller family with additional features such as enhanced control logic, adaptive delay set, and shutdown capability.

Since it is built in BCDMOS, it operates with dramatically less supply current than its bipolar counterparts. The *UCCx895* can operate with a maximum clock frequency of 1MHz.

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Table 1

Symbol	Description
SYNC	Bi-directional clock and synchronization pin
E/AOUT	Error amplifier output
CS	Current sense
Ct	Oscillator frequency set pin (capacitor)
Rt	Oscillator frequency set pin (resistor)
DEL_AB	Output delay control A-B
DEL_CD	Output delay control C-D
EAN	Error amplifier inverting input
EAP	Error amplifier non-inverting input
GND	Signal ground
OUT A	Output A
OUT B	Output B
OUT C	Output C
OUT D	Output D
PGND	Power ground

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RAMP	Voltage ramp
SLOPE	Adaptive Delay Set
ADS	Soft start
VDD	Output switch supply voltage
VREF	Reference voltage

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Parameters

Comparison between model and real component.

Unless otherwise specified, VDD=12V, RT=82k , CT=220pF, RDELAB=10k , RDELCD=10k , CREF=0.1 F, CVDD=1.0 F, no load at outputs. TA= TJ. TA = 0°C to 70°C for UCC3895x, -40°C to +85°C for UCC2895x, and -55°C to +125°C for UCC1895x.

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Table 2

PARAMETER	TEST CONDITIONS	UCCx895			MODEL	UNITS
		MIN	TYP	MAX		
UVLO Section						
Start Threshold		10.2	11	11.8	11	V
Stop Threshold		8.2	9	9.8	9	V
Hysteresis		1.0	2.0	3.0	2.0	V
Supply Current						
Start-up Current	VDD = 8V		150	250	0	µA
I_{DD} Active			5	6	0	mA
VDD Clamp Voltage	IDD = 10mA	16.5	17.5	18.5	17.5	V
Voltage Reference Section						
Output Voltage	T_J = 25°C	4.94	5.00	5.06	5.00	V
	10V < VDD < 17.5V, 0mA < IREF < 5mA, Temperature	4.85	5	5.15	5	V
Short CircuitCurrent	REF = 0V, T_J = 25°C	10	20		20	mA
Error AmplifierSection						
Common Mode Input Voltage Range		-0.1		3.6	X	V
Offset Voltage		-7		7	0	mV
Input Bias Current (EAP, EAN)		-1		1	0	µA
EAOUT VOH	EAP-EAN = 500mV, I_{EAOUT} = -0.5mA	4.0	4.5	5.0	4.5	V

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EAOUT VOL	EAP-EAN = -500mV, I_{EAOUT}= 0.5mA	0	0.2	0.4	0	V
EAOUT SourceCur-rent	EAP-EAN = 500mV, EAOUT= 2.5V	1.0	1.5		X	mA
EAOUT SinkCurrent	EAP-EAN = -500mV, EAOUT= 2.5V, (Note 4)	2.5	4.5		X	mA
Open Loop DC Gain		75	85			dB
Unity GainBand-width	(Note 3)	5.0	70		X	MHz
Slew Rate	EAN from 1V to 0V, EAP = 500mV, EAOUT from 0.5V to 3.0V, (Note 3)	1.5	2.2		X	V/ µs
No Load Comparator Turn-Off Threshold		0.45	0.50	0.55	0.5	V
No Load Comparator Turn-On Threshold		0.55	0.60	0.69	0.6	V
No Load Comparator Hysteresis		0.03-5	0.10-0	0.16-5	0.1	V
Oscillator Section						
Frequency	T_J = 25°C	473	500	527	495	kHz
Total Vari-ation	Line, Tem-perature (Note 3)		2.5	5	0	%
SYNC VIH		2.05	2.10	2.25	2.1	V
SYNC VIL		1.85	1.90	1.95	1.90	V

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SYNC VOH	I_{SYNC} = -400 µA, CT = 2.6V	4.1	4.5	5.0	4.5	V
SYNC VOL	I_{SYNC} = 100 µA, CT = 0V	0.0	0.5	1.0	0.5	V
SYNC Output Pulse Width	SYNC Load = 3.9kÂ Â and 30pF in parallel		85	135	84	ns
RT Voltage		2.9	3	3.1	3	V
CT PeakVoltage		2.25	2.35	2.50	2.35	V
CT Valley Voltage	UCC2895, UCC3895	0.0	0.2	0.4	0.2	V
PWM ComparatorSection						
EAOUT to RAMP Input Offset Voltage	RAMP = 0V, DELAB = DELCD = REF	0.72	0.85	1.05	0.85	V
Minimum Phase Shift (OUTA to OUTC, OUTB to OUTD)	RAMP = 0V, EAOUT = 650mV (Note 1)	0.00	0.85	1.40	3.9	%
RAMP to OUTC/OUTD Delay	RAMP from 0V to 2.5V, EAOUT = 1.2V, DELAB = DELCD = REF (Note 2)		70	120	0	ns
RAMP BiasCurrent	RAMP < 5V, CT < 2.2V	-5		5	0	µA
RAMP SinkCurrent	RAMP = 5V, CT < 2.6V	12	19		0	mA
Current SenseSection						
CS BiasCurrent	0 < CS , 2.5V, 0 < ADS < 2.5V	-4.5		20	0	µA
Peak Cur-		1.90	.200	2.10	0	V

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rent Threshold						
Overcurrent Threshold		2.4	2.5	2.6	2.5	V
CS to Output Delay	CS from 0 to 2.3V, DELAB = DELCD = REF		75	110	0	ns
Soft Start/ShutdownSection						
Soft StartSource Current	SS/DISB = 3.0V, CS < 1.9V	-40	-35	-30	-35	µA
Soft StartSinkCurrent	SS/DISB = 3.0V, CS > 2.6V	325	350	375	350	µA
Soft Start/Disable Comparator Threshold		0.44	0.50	0.56	0.5	V
Delay Set Section						
DELAB/DELCD Output Voltage	ADS = CS = 0V	0.45	0.50	0.55	0.5	V
	ADS = 0V, CS = 2.0V	1.9	2.0	2.1	2.0	V
Output Delay	ADS = CS = 0V (Notes 2 and 3)	450	525	600	502	ns
ADS BiasCurrent	0V < ADS < 2.5V, 0V < CS < 2.5V	-20		20	0	µA
Output Section						
VOH (all outputs)	IOUT = -10mA, VDD to Output		250	400	0	mV
VOL (all outputs)	IOUT = 10mA		150	250	0	mV
Rise Time	C_{LOAD} = 100pF, (Note 3)		20	35	X	ns
Fall Time	C_{LOAD} = 100pF, (Note 3)		20	35	X	ns

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X: not modeled
Note 1: Minimum phase shift is defined as followed:
$\Phi = t_{f(OUTA)} - t_{f(OUTC)} / t_{PERIOD}$, *or:*
$\Phi = t_{f(OUTB)} - t_{f(OUTD)} / t_{PERIOD}$, *where:*
$t_{f(OUTA)}$ *= falling edge of OUTA signal*
$t_{f(OUTB)}$ *= falling edge of OUTB signal*
$t_{f(OUTC)}$ *= falling edge of OUTC signal*
$t_{f(OUTD)}$ *= falling edge of OUTD signal*
$t_{f(PERIOD)}$ *= period of OUTA or OUTB signal*

Note 2. Output delay is measured between OUTA/OUTB or OUTC/OUTD. Output delay is defined as shown below, where:
$t_{f(OUTA)}$ *= falling edge of OUTA signal*
$t_{f(OUTB)}$ *= rising edge of OUTB signal*

Note 3: Ensured by design. Not 100% tested in production.
Note 4: For UCC1895, MIN limit is 2.2 mA at -55°C

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Example circuit :

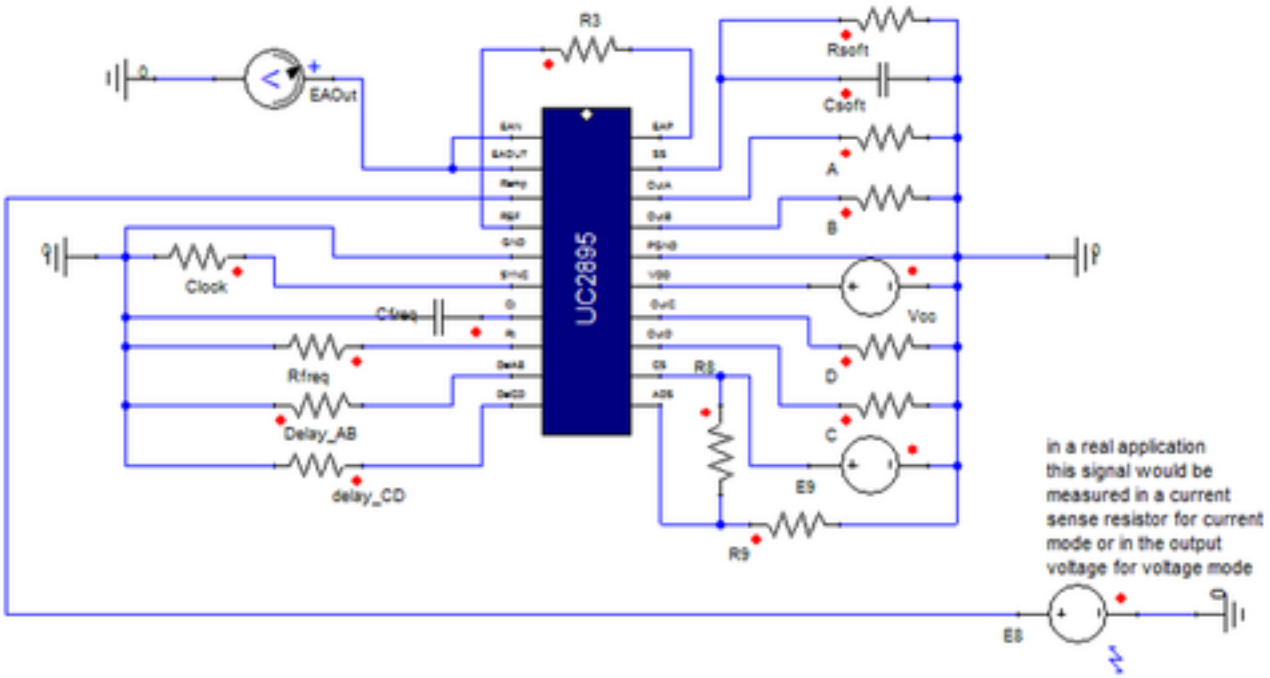

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Figure 2. Example Circuit

In a real application, the output pins would be connected to MOSFET gates or to a transformer. Here, they had been replaced with resistors. Using a simpler external circuit allows us to focus in the IC operation.

Another components connected to the IC are the resistor and the capacitor used to set the oscillator frequency, the feedback network of the error amplifier and the capacitors that set the behavior of the soft-start. A saw-tooth waveform voltage source has been connected to the ramp pin to model the waveform in a current sense resistor.

We can use the output resistors voltage to control the four switches of a full-bridge inverter:

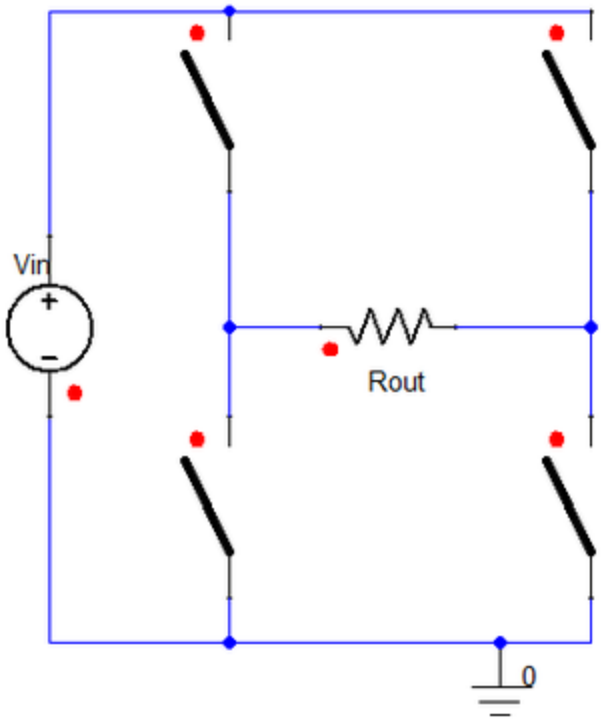

Figure 3. Four Switches Full-bridge Inverter

Simulation results :

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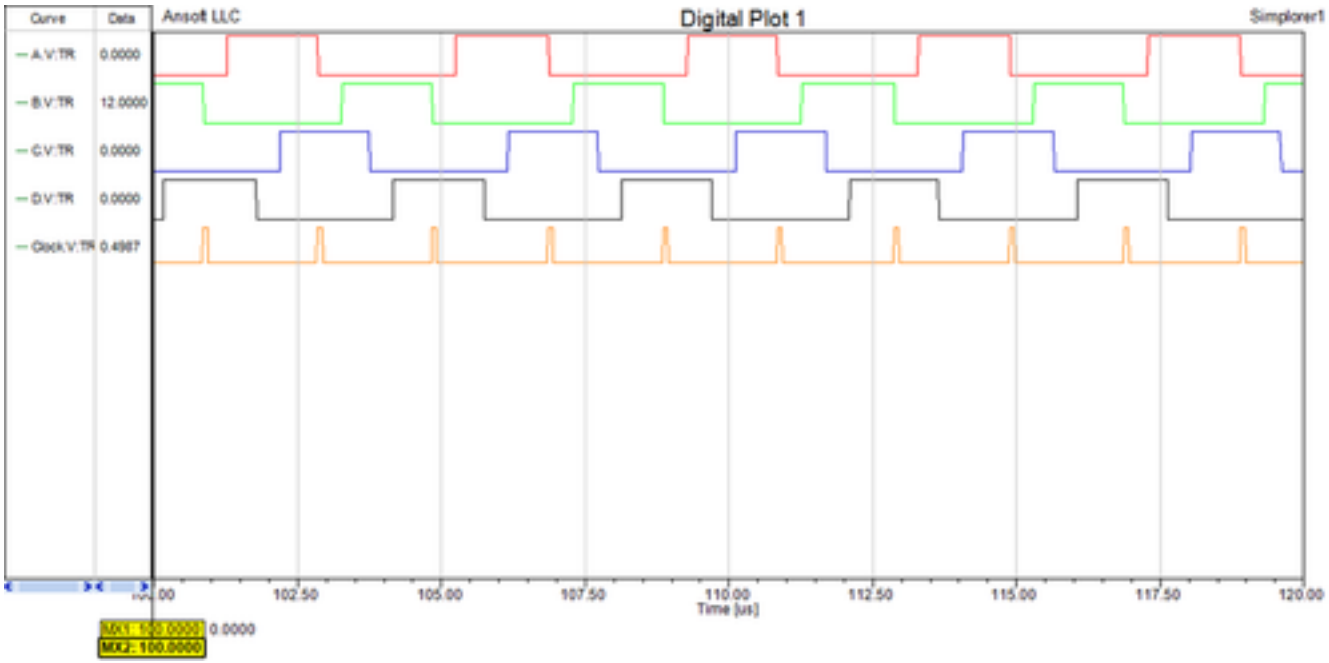

Figure 4 Simulation results(a)

In this figure we can see the four output waveforms. The comparison between the ramp voltage and the error amplifier output voltage sets the AB-CD shift. The shift value is changing in the figure because of the increasing error amplifier output voltage, as shown in the next diagram. The gap between the falling of C and the rising of D, as well as the one between A and B, is fixed by user by connecting a resistor in the delay control pin.

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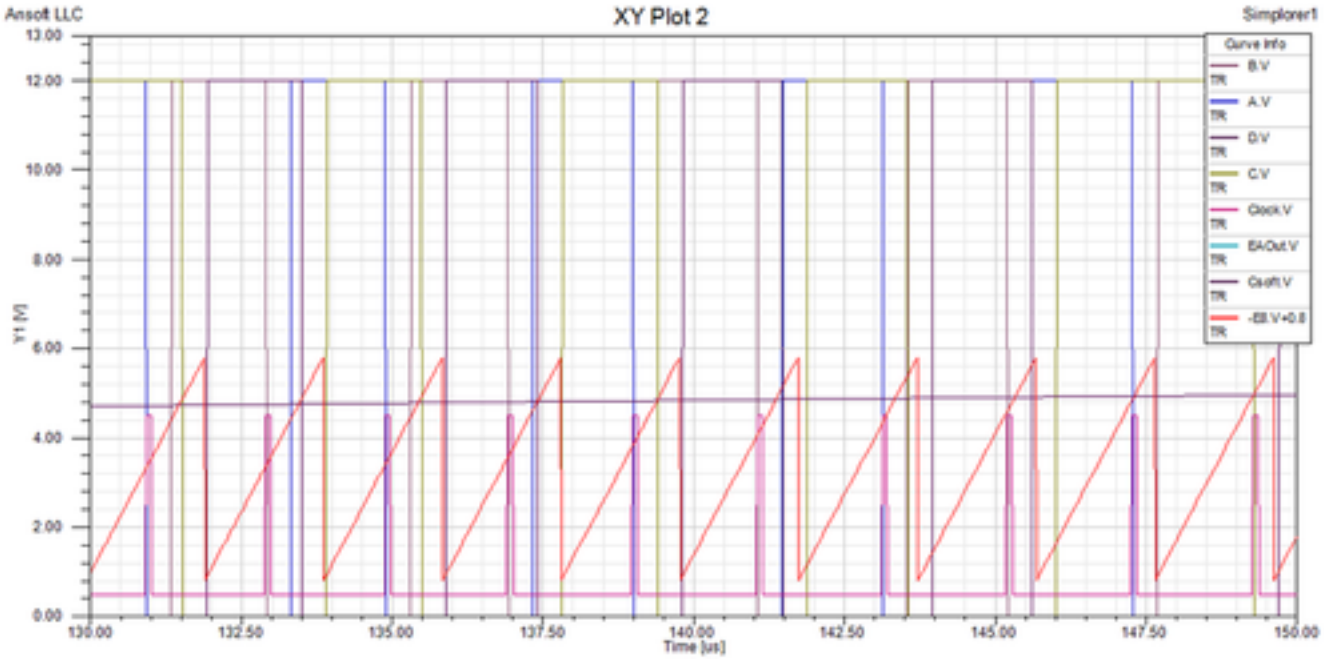

Figure 5. Simulation results(b)

When the error amplifier output voltage (light blue) reaches the ramp voltage (red), C output voltage -or D, depending on the period number- falls. The phase of the A and B outputs is constant and is the C and D the one which shifts.

In the following diagram we can see a detail of the oscillator voltage (red) and the synchronization signal (clock, in purple).

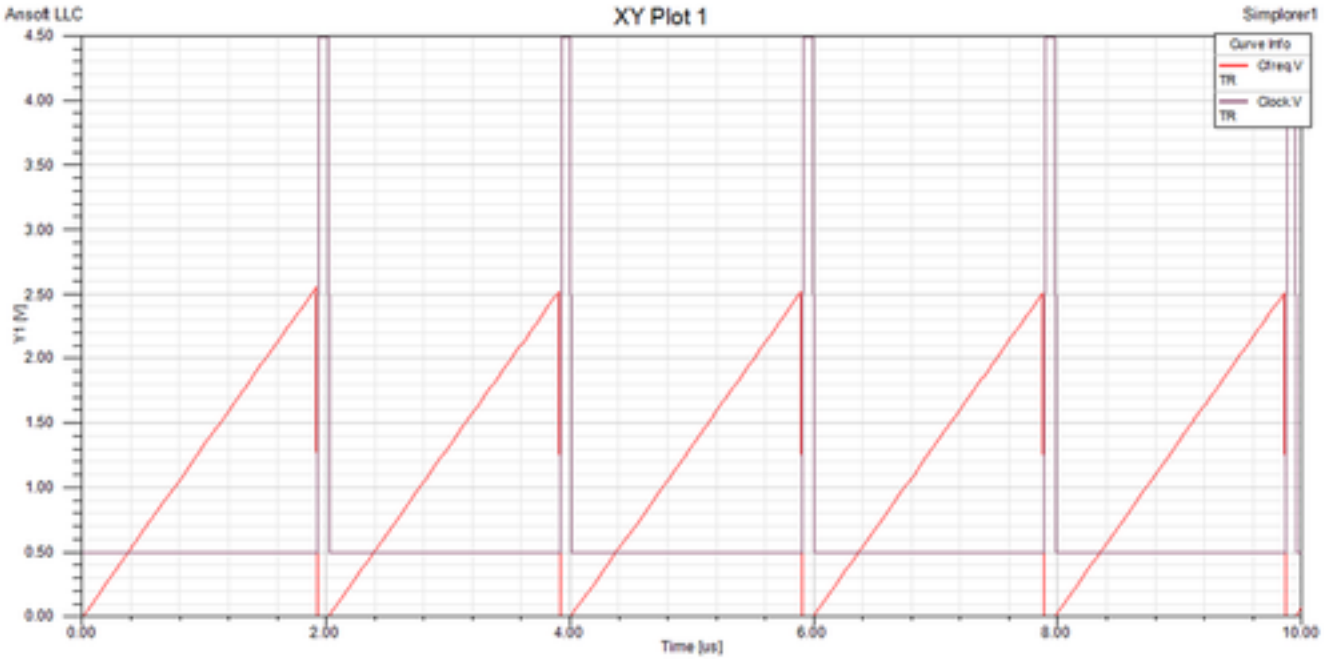

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Figure 6. Simulation results(c)

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UCCx8C40: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

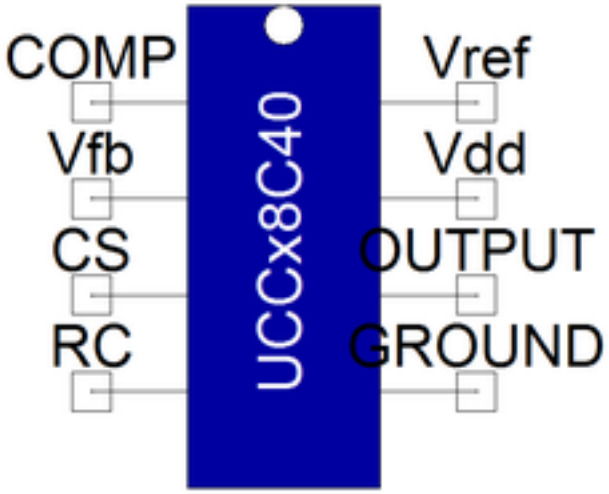

Figure 1. Component symbol

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Description

UCC38C4x family is a high-performance current mode PWM controller. It is an enhanced BiCMOS version with pin-for-pin compatibility to the industry standard *UC384xA* family and *UC384x* family of PWM controllers. In addition, lower startup voltage versions of 7 V are offered as *UCC38C40* and *UCC38C41*.

Providing necessary features to control fixed frequency, peak current-mode power supplies, this family offers the following performance advantages. The device offers high-frequency operation up to 1 MHz with low start-up and operating currents, thus minimizing start-up loss and low

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operating power consumption for improved efficiency. The device also features a very fast current-sense-to-output delay time of 35 ns and a±1 A peak output current capability with improved rise and fall times for driving large external MOSFETs directly.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: operating supply current has been modeled with a constant value current source.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 9V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vdd	Power input

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OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Electrical characteristics VDD = 15 V (See Note 1), RT = 10 kΩ, CT = 3.3 nF, CVDD = 0.1µF and no load on the outputs, TA = -40°C to 105°C for the UCC28C4x and TA = 0°C to 70°C for the UCC38C4x, TA = TJ (unless otherwise noted)

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx8C40 MIN	 TYP	 MAX	MODEL	UNIT
REFERENCE SECTION						
Output Voltage	T_A = 25 °C	4.90	5.00	5.10	5.00	V
Line Regulation	V_{DD}= 12V to 18 V		0.2	20	0.2	mV
Load Regulation	1mA to 20 mA		3	25	0	
Temp. Stability	See Note 2		0.2	0.4	0	mV/ °C
Total Output Variation	See Note 2	4.82		5.18	0	V
Output Noise Voltage	10 Hz to 10 kHz, TA = 25 C See Note 2		50		0	µV
Long TermStability	TA = 125 °C, 1000 Hrs See Note 2		5	25	0	mV
Output Short Circuit		-30	-45	-55	X	mA

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OSCILLATOR SECTION						
Initial Accuracy	TA = 25 °CSee Note 3	50.5	53	55	54	kHz
Voltage Stability	V_{DD}= 12V to 18 V		0.2%	1%	0 %	
Temp. Stability	TMIN toTMAX, See Note 2		1%	2.5%	0 %	
Amplitude	Rt/Ct Pin peak-to-peak		1.9		2.0	V
Discharge current	TA = 25 °C, Rt/Ct=2V See Note 4	7.7	8.4	9.0	8.4	mA
	Rt/Ct=2V, See Note 4	7.2	8.4	9.5	8.4	mA
ERROR AMPLIFIER SECTION						
Feedback Input Voltage	VCOMP= 2.5 V, TA = 25 °C	2.47-5	2.50-0	2.52-5	2.50	V
Input BiasCur-rent	VFB = 5.0V		-0.1	-2.0	0	µA
Open-loopGain (AVOL)	VOUT=2V to 4 V	65	90		90	dB
Unity GainBand-width	See Note 2	1.0	1.5		X	MH-z
PSRR	V_{DD}= 12V to 18 V	60			60	dB
Output SinkCur-rent	VFB = 2.7 V, VCOMP= 1.1 V	2	14		100	mA
Output SourceCur-rent	VFB = 2.3 V, VCOMP= 5 V	-0.5	-1.0		-1.0	
VOUT High	VFB= 2.3 V, RL = 15 k to GND	5	6.8		6.8	V
VOUT Low	VFB= 2.7 V, RL = 15 k to VREF		0.1	1.1	0.1	

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CURRENT SENSE SECTION						
Gain	See Note 5, 6	2.85	3.00	3.15	3.0	V/V
Maximum Input Signal	VFB < 2.4 V	0.9	1.0	1.1	1.0	V
PSRR	V_{DD}= 12V to 18 V, See Note 2, 5		70		X	dB
Input BiasCurrent			-2	-10	0	µA
CS to output delay			35	70	35	ns
COMP to CS offset			1.15		1.15	V
OUTPUT SECTION						
VOUT low (Rds pull-dwn)	Isink =200mA		5.5	15	5.5	Ω
VOUT high (Rds pull-up)	Isource =200mA		10	25	10	
Rise Time	TA = 25°C, CLOAD = 1 nF		50	150	X	ns
Fall Time	TA= 25°C, CLOAD = 1nF		50	150	X	
UNDER-VOLTAGE LOCKOUT SECTION						
Start Threshold		6.5	7	7.5	7	V
Min. Operating Voltage		6.1	6.6	7.1	9	
PWM SECTION						
Maximum DutyCycle		94%	96%		96%	
Minimum DutyCycle				0%	0%	
TOTAL STANDBY CURRENT						
Start-Up Current	VDD-D=UVLO		50	100	0	A

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	start threshold (-0.5)					
Operating SupplyCur-rent	VFB = VCS = 0 V		2.3	3.0	0	mA

X: not modeled
NOTE 1: Adjust VDD above the start threshold before setting at 15 V.
NOTE: 2. Ensured by design. Not production tested.
NOTE: 3. Output frequencies of the UCC38C41, UCC38C44 and the UCC38C45 are half the oscillator frequency.
NOTE: 4. Oscillator discharge current is measured with RT = 10 kΩ to VREF.
NOTE: 5. Parameter measured at trip point of latch with VFB = 0 V.
NOTE: 6. Gain is defined as ACS=ΔVcom/ΔVcs, 0V ≤ Vcs ≤ 900mV

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Example circuit :

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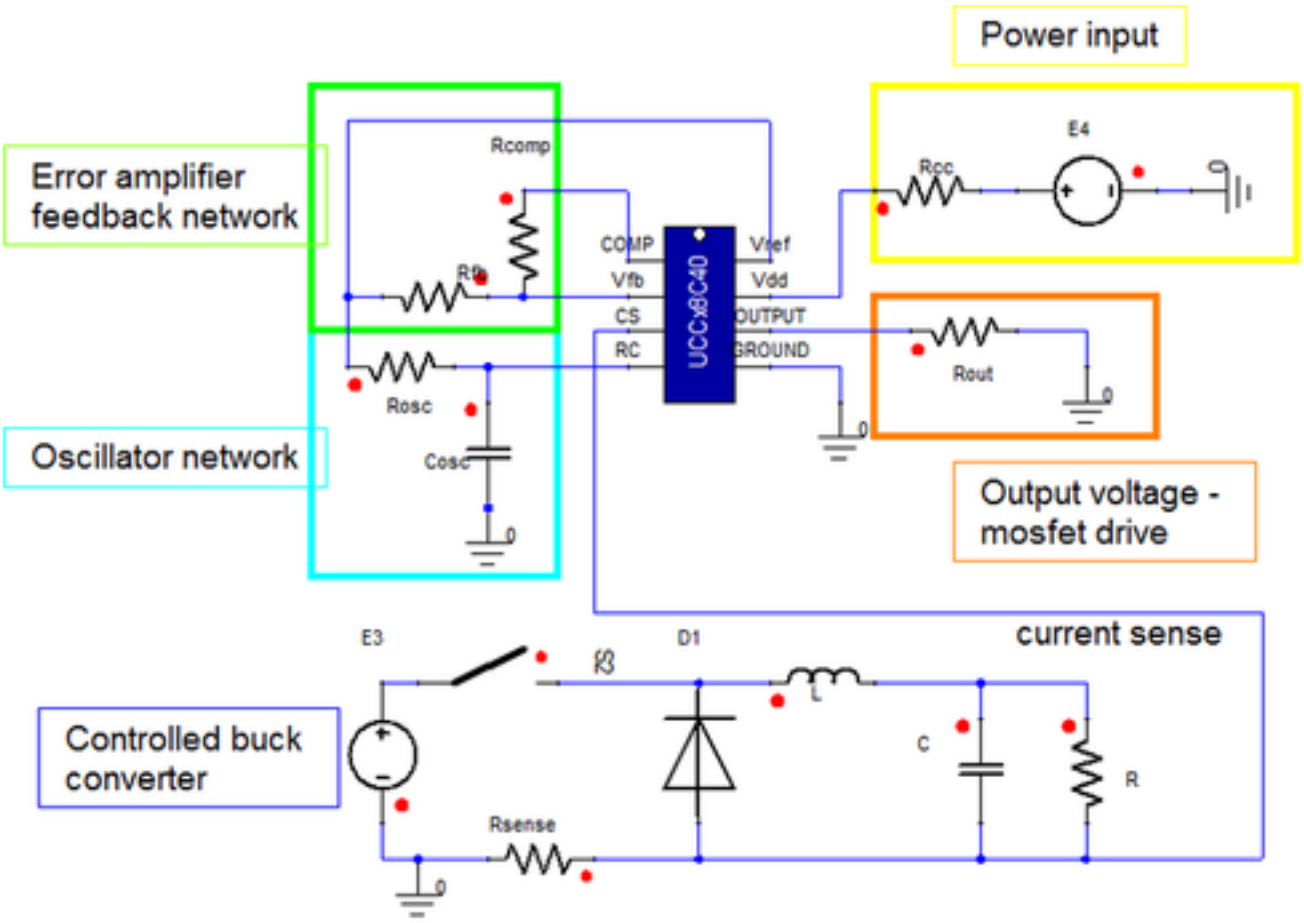

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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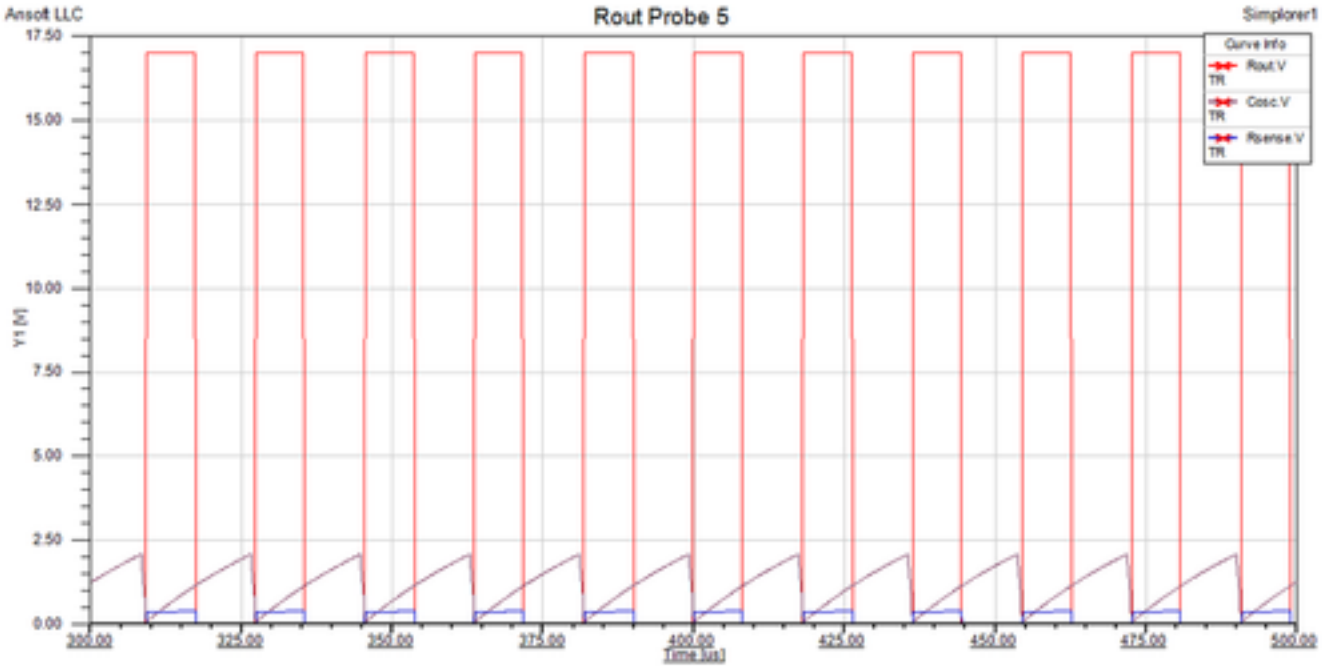

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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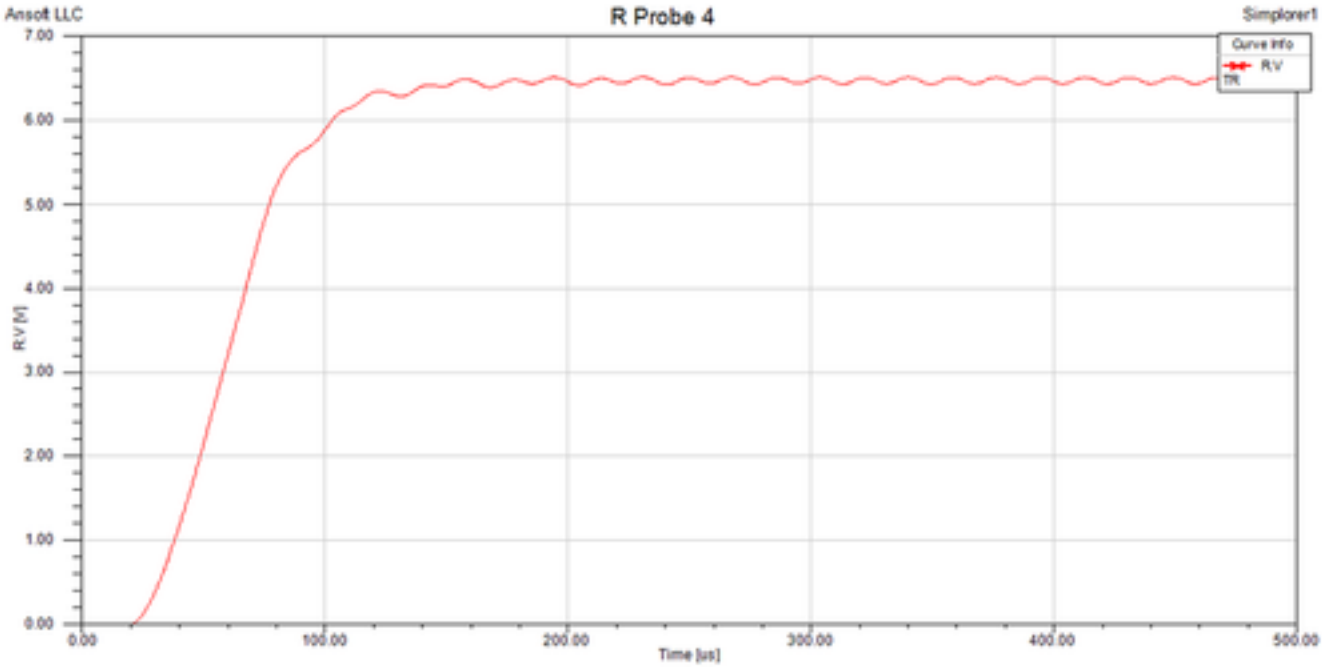

Red: converter output voltage.

Figure 4. Simulation results(b)

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References

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UCCx8C41: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

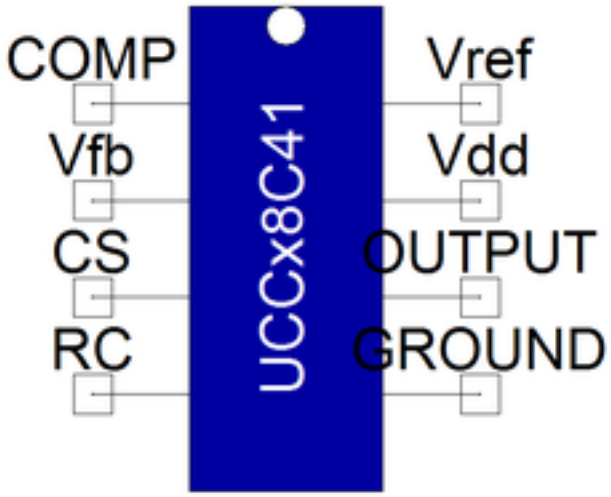

Figure 1. Component symbol

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Description

UCC38C4x family is a high-performance current mode PWM controller. It is an enhanced BiCMOS version with pin-for-pin compatibility to the industry standard *UC384xA* family and *UC384x* family of PWM controllers. In addition, lower startup voltage versions of 7 V are offered as *UCC38C40* and *UCC38C41*.

Providing necessary features to control fixed frequency, peak current-mode power supplies, this family offers the following performance advantages. The device offers high-frequency operation up to 1 MHz with low start-up and operating currents, thus minimizing start-up loss and low

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operating power consumption for improved efficiency. The device also features a very fast current-sense-to-output delay time of 35 ns and a±1 A peak output current capability with improved rise and fall times for driving large external MOSFETs directly.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: operating supply current has been modeled with a constant value current source.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 9V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Conservative Pins

Table 1

Symbol	Description
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Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vdd	Power input

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OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Electrical characteristics VDD = 15 V (See Note 1), RT = 10 kΩ, CT = 3.3 nF, CVDD = 0.1µF and no load on the outputs, TA = -40°C to 105°C for the UCC28C4x and TA = 0°C to 70°C for the UCC38C4x, TA = TJ (unless otherwise noted)

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx8C41 MIN	 TYP	 MAX	MODEL	UNIT
REFERENCE SECTION						
Output Voltage	T_A = 25 °C	4.90	5.00	5.10	5.00	V
Line Regulation	V_{DD}= 12V to 18 V		0.2	20	0.2	mV
Load Regulation	1mA to 20 mA		3	25	0	
Temp. Stability	See Note 2		0.2	0.4	0	mV/ °C
Total Output Variation	See Note 2	4.82		5.18	0	V
Output Noise Voltage	10 Hz to 10 kHz, TA = 25 C See Note 2		50		0	µV
Long TermStability	TA = 125 °C, 1000 Hrs See Note 2		5	25	0	mV
Output Short Circuit		-30	-45	-55	X	mA

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OSCILLATOR SECTION						
Initial Accuracy	TA = 25 °CSee Note 3	50.5	53	55	54	kHz
Voltage Stability	V_{DD}= 12V to 18 V		0.2%	1%	0 %	
Temp. Stability	TMIN toTMAX, See Note 2		1%	2.5%	0 %	
Amplitude	Rt/Ct Pin peak-to-peak		1.9		2.0	V
Discharge current	TA = 25 °C, Rt/Ct=2V See Note 4	7.7	8.4	9.0	8.4	mA
	Rt/Ct=2V, See Note 4	7.2	8.4	9.5	8.4	mA
ERROR AMPLIFIER SECTION						
Feedback Input Voltage	VCOMP= 2.5 V, TA = 25 °C	2.47-5	2.50-0	2.52-5	2.50	V
Input BiasCur-rent	VFB = 5.0V		-0.1	-2.0	0	µA
Open-loopGain (AVOL)	VOUT=2V to 4 V	65	90		90	dB
Unity GainBand-width	See Note 2	1.0	1.5		X	MH-z
PSRR	V_{DD}= 12V to 18 V	60			60	dB
Output SinkCur-rent	VFB = 2.7 V, VCOMP= 1.1 V	2	14		100	mA
Output SourceCur-rent	VFB = 2.3 V, VCOMP= 5 V	-0.5	-1.0		-1.0	
VOUT High	VFB= 2.3 V, RL = 15 k to GND	5	6.8		6.8	V
VOUT Low	VFB= 2.7 V, RL = 15 k to VREF		0.1	1.1	0.1	

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CURRENT SENSE SECTION						
Gain	See Note 5, 6	2.85	3.00	3.15	3.0	V/V
Maximum Input Signal	VFB < 2.4 V	0.9	1.0	1.1	1.0	V
PSRR	V_{DD}= 12V to 18 V, See Note 2, 5		70		X	dB
Input BiasCurrent			-2	-10	0	µA
CS to output delay			35	70	35	ns
COMP to CS offset			1.15		1.15	V
OUTPUT SECTION						
VOUT low (Rds pull-dwn)	Isink =200mA		5.5	15	5.5	Ω
VOUT high (Rds pull-up)	Isource =200mA		10	25	10	
Rise Time	TA = 25°C, CLOAD = 1 nF		50	150	X	ns
Fall Time	TA= 25°C, CLOAD = 1nF		50	150	X	
UNDER-VOLTAGE LOCKOUT SECTION						
Start Threshold		6.5	7	7.5	7	V
Min. Operating Voltage		6.1	6.6	7.1	9	
PWM SECTION						
Maximum DutyCycle		47%	48%		48%	
Minimum DutyCycle				0%	0%	
TOTAL STANDBY CURRENT						
Start-Up Current	VDD-D=UVLO		50	100	0	A

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	start threshold (-0.5)					
Operating SupplyCur-rent	VFB = VCS = 0 V		2.3	3.0	0	mA

X: not modeled
NOTE 1: Adjust VDD above the start threshold before setting at 15 V.
NOTE: 2. Ensured by design. Not production tested.
NOTE: 3. Output frequencies of the UCC38C41, UCC38C44 and the UCC38C45 are half the oscillator frequency.
NOTE: 4. Oscillator discharge current is measured with RT = 10 kΩ to VREF.
NOTE: 5. Parameter measured at trip point of latch with VFB = 0 V.
NOTE: 6. Gain is defined as ACS=ΔVcom/ΔVcs, 0V ≤ Vcs ≤ 900mV

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Example circuit :

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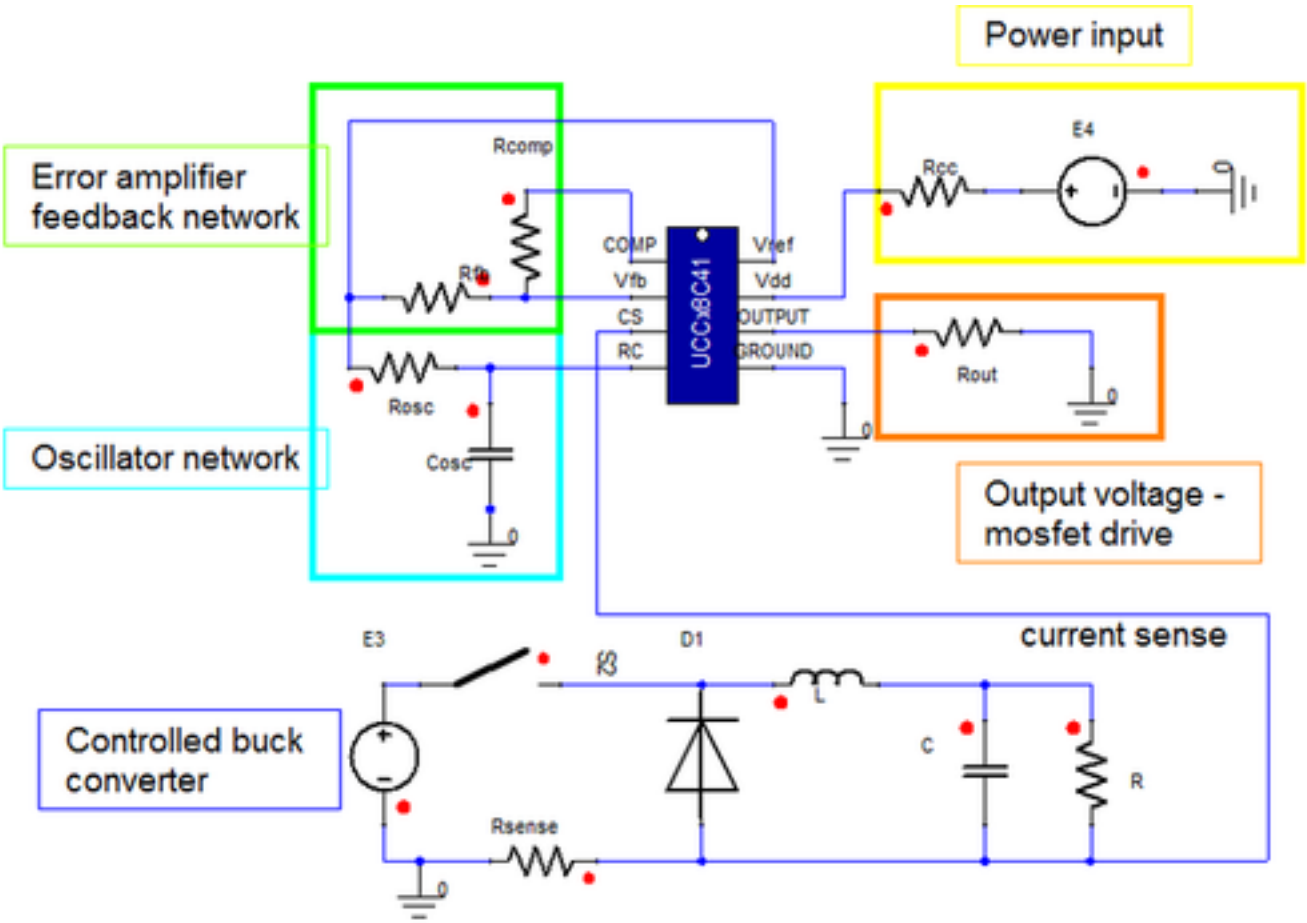

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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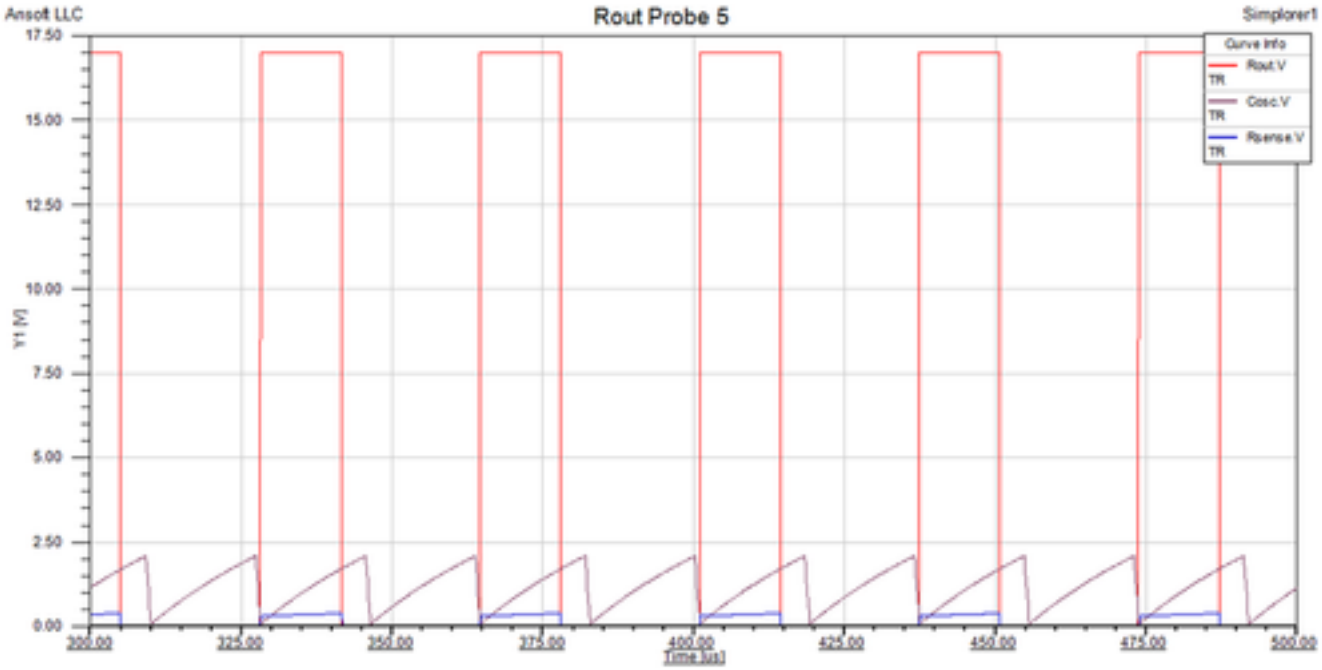

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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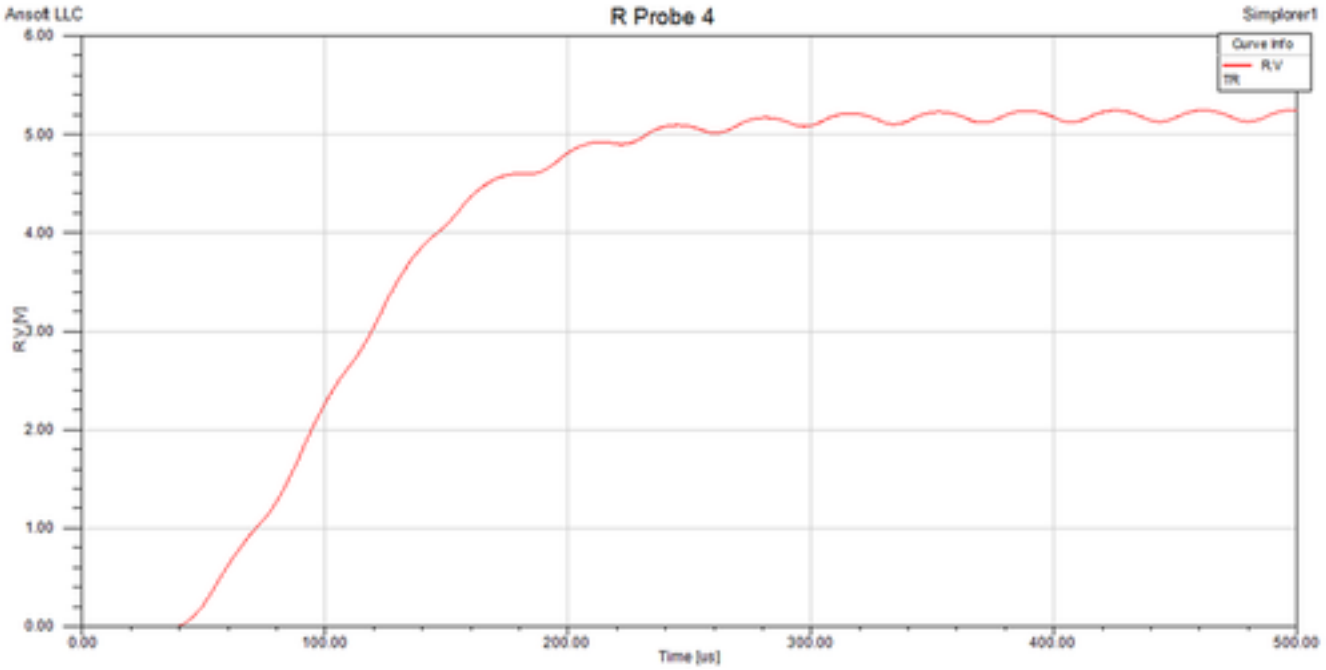

Red: converter output voltage.

Figure 4. Simulation results(b)

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UCCx8C42: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

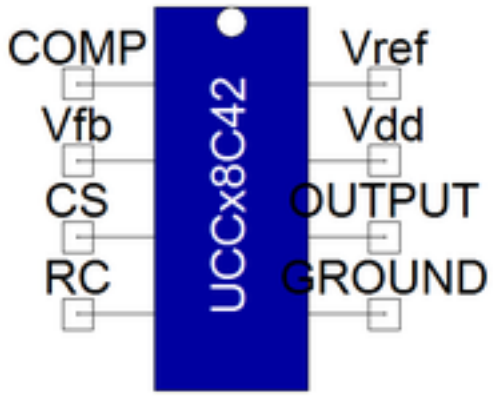

Figure 1. Component symbol

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Providing necessary features to control fixed frequency, peak current-mode power supplies, this family offers the following performance advantages. The device offers high-frequency operation up to 1 MHz with low start-up and operating currents, thus minimizing start-up loss and low

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operating power consumption for improved efficiency. The device also features a very fast current-sense-to-output delay time of 35 ns and a±1 A peak output current capability with improved rise and fall times for driving large external MOSFETs directly.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: operating supply current has been modeled with a constant value current source.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 9V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vdd	Power input

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OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Electrical characteristics VDD = 15 V (See Note 1), RT = 10 kΩ, CT = 3.3 nF, CVDD = 0.1µF and no load on the outputs, TA = -40°C to 105°C for the UCC28C4x and TA = 0°C to 70°C for the UCC38C4x, TA = TJ (unless otherwise noted)

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx8C42 MIN	 TYP	 MAX	MODEL	UNIT
REFERENCE SECTION						
Output Voltage	T_A = 25 °C	4.90	5.00	5.10	5.00	V
Line Regulation	V_{DD}= 12V to 18 V		0.2	20	0.2	mV
Load Regulation	1mA to 20 mA		3	25	0	
Temp. Stability	See Note 2		0.2	0.4	0	mV/°C
Total Output Variation	See Note 2	4.82		5.18	0	V
Output Noise Voltage	10 Hz to 10 kHz, TA = 25 C See Note 2		50		0	µV
Long TermStability	TA = 125 °C, 1000 Hrs See Note 2		5	25	0	mV
Output Short Circuit		-30	-45	-55	X	mA

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OSCILLATOR SECTION						
Initial Accuracy	TA = 25 °CSee Note 3	50.5	53	55	54	kHz
Voltage Stability	V_{DD}= 12V to 18 V		0.2%	1%	0 %	
Temp. Stability	TMIN toTMAX, See Note 2		1%	2.5%	0 %	
Amplitude	Rt/Ct Pin peak-to-peak		1.9		2.0	V
Discharge current	TA = 25 °C, Rt/Ct=2V See Note 4	7.7	8.4	9.0	8.4	mA
	Rt/Ct=2V, See Note 4	7.2	8.4	9.5	8.4	mA
ERROR AMPLIFIER SECTION						
Feedback Input Voltage	VCOMP= 2.5 V, TA = 25 °C	2.47-5	2.50-0	2.52-5	2.50	V
Input BiasCur-rent	VFB = 5.0V		-0.1	-2.0	0	µA
Open-loopGain (AVOL)	VOUT=2V to 4 V	65	90		90	dB
Unity GainBand-width	See Note 2	1.0	1.5		X	MH-z
PSRR	V_{DD}= 12V to 18 V	60			60	dB
Output SinkCur-rent	VFB = 2.7 V, VCOMP= 1.1 V	2	14		100	mA
Output SourceCur-rent	VFB = 2.3 V, VCOMP= 5 V	-0.5	-1.0		-1.0	
VOUT High	VFB= 2.3 V, RL = 15 k to GND	5	6.8		6.8	V
VOUT Low	VFB= 2.7 V, RL = 15 k to VREF		0.1	1.1	0.1	

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CURRENT SENSE SECTION						
Gain	See Note 5, 6	2.85	3.00	3.15	3.0	V/V
Maximum Input Signal	VFB < 2.4 V	0.9	1.0	1.1	1.0	V
PSRR	V_{DD}= 12V to 18 V, See Note 2, 5		70		X	dB
Input BiasCurrent			-2	-10	0	µA
CS to output delay			35	70	35	ns
COMP to CS offset			1.15		1.15	V
OUTPUT SECTION						
VOUT low (Rds pulldwn)	Isink =200mA		5.5	15	5.5	Ω
VOUT high (Rds pullup)	Isource =200mA		10	25	10	
Rise Time	TA = 25°C, CLOAD = 1 nF		50	150	X	ns
Fall Time	TA= 25°C, CLOAD = 1nF		50	150	X	
UNDER-VOLTAGE LOCKOUT SECTION						
Start Threshold		13.5	14.5	15.5	14.5	V
Min. Operating Voltage		8	9	10	9	
PWM SECTION						
Maximum DutyCycle		94%	96%		96%	
Minimum DutyCycle				0%	0%	
TOTAL STANDBY CURRENT						
Start-Up Current	VDD-D=UVLO		50	100	0	A

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	start threshold (-0.5)					
Operating SupplyCur-rent	VFB = VCS = 0 V		2.3	3.0	0	mA

X: not modeled
NOTE 1: Adjust VDD above the start threshold before setting at 15 V.
NOTE: 2. Ensured by design. Not production tested.
NOTE: 3. Output frequencies of the UCC38C41, UCC38C44 and the UCC38C45 are half the oscillator frequency.
NOTE: 4. Oscillator discharge current is measured with RT = 10 kΩ to VREF.
NOTE: 5. Parameter measured at trip point of latch with VFB = 0 V.
NOTE: 6. Gain is defined as ACS=ΔVcom/ΔVcs, 0V ≤ Vcs ≤ 900mV

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Example circuit :

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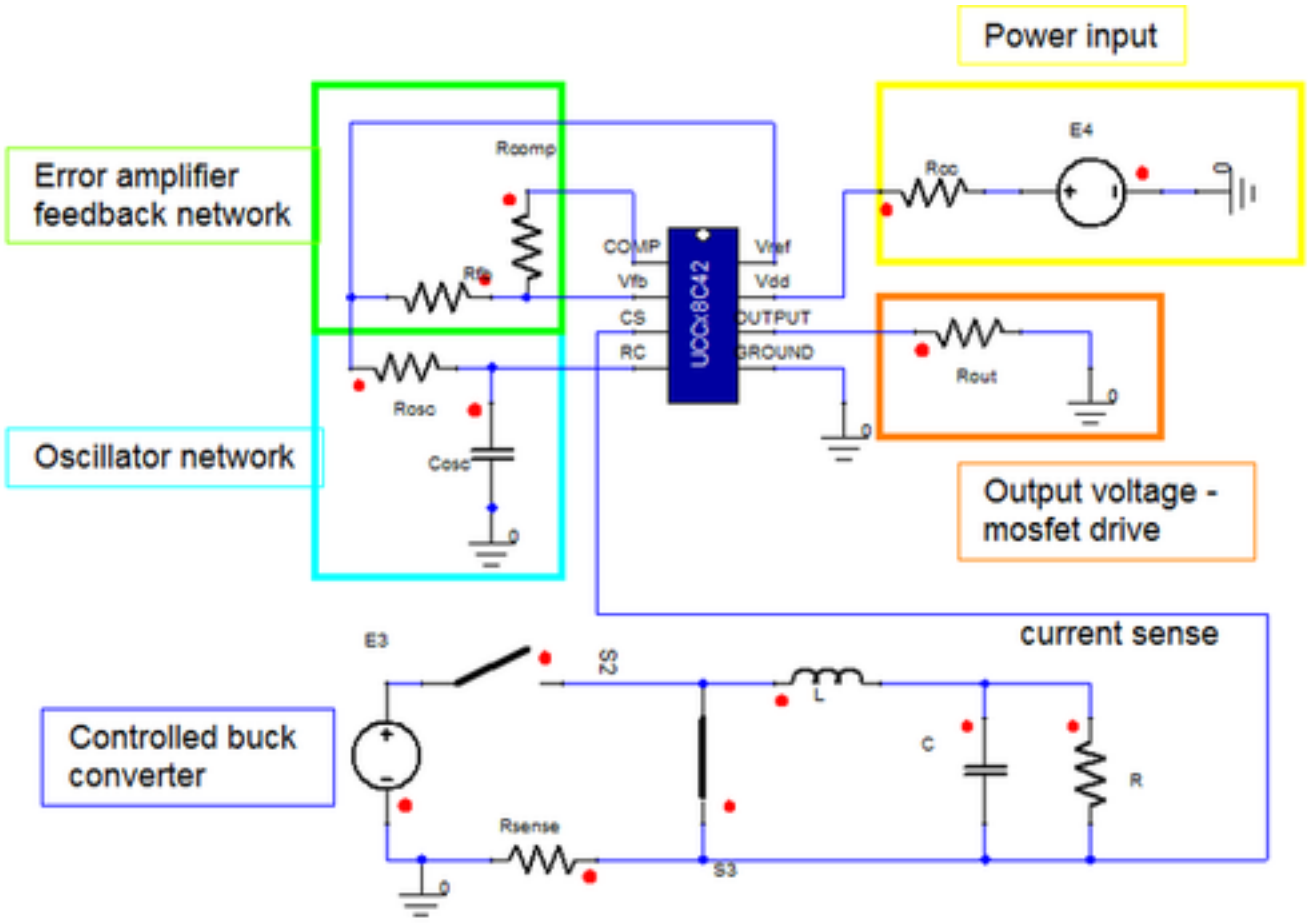

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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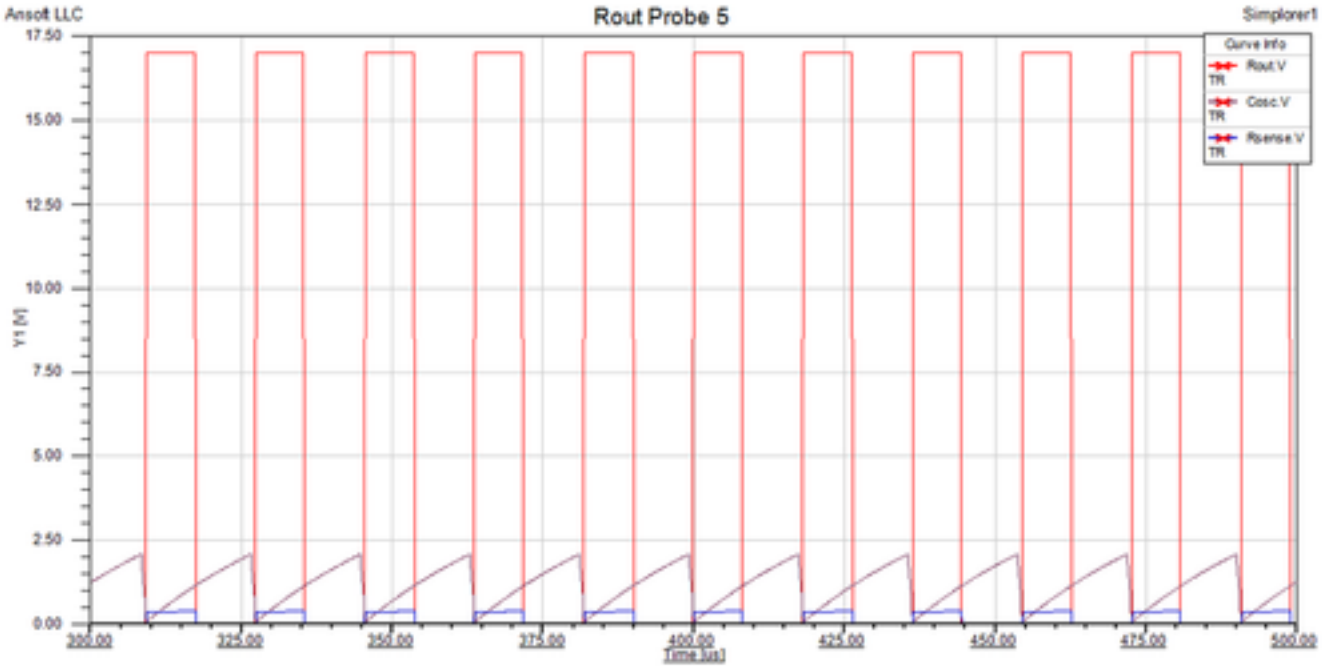

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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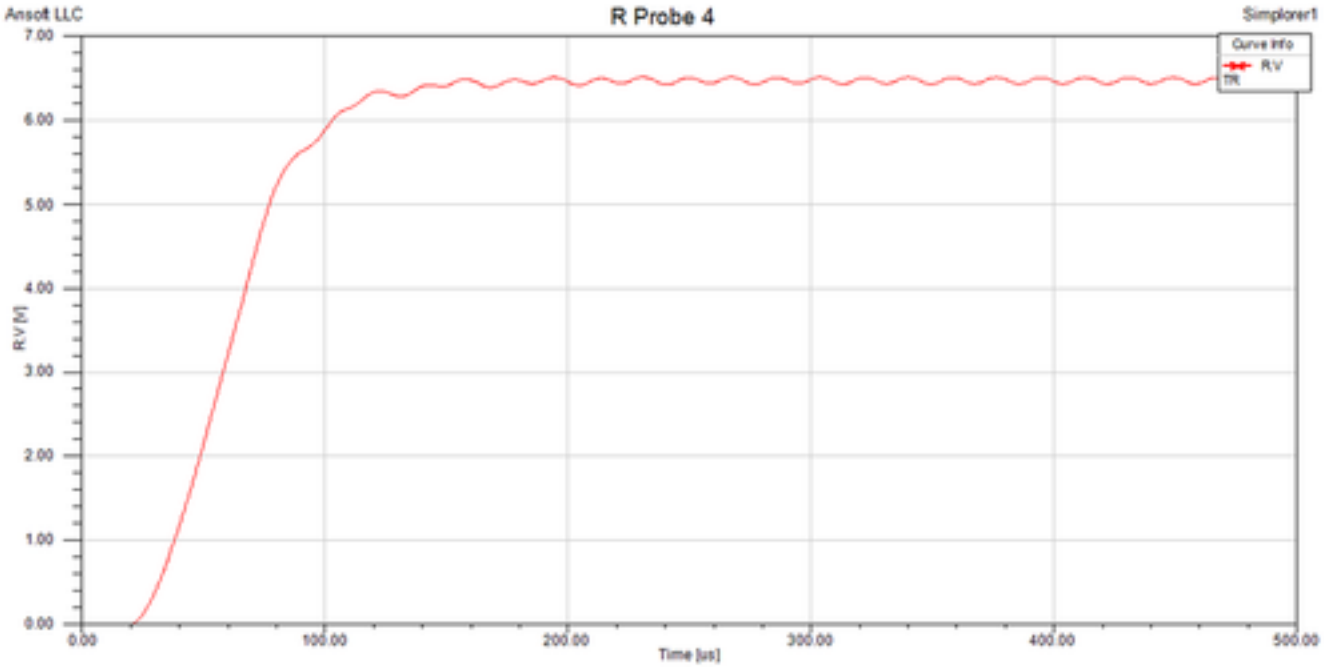

Red: converter output voltage.

Figure 4. Simulation results(b)

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References

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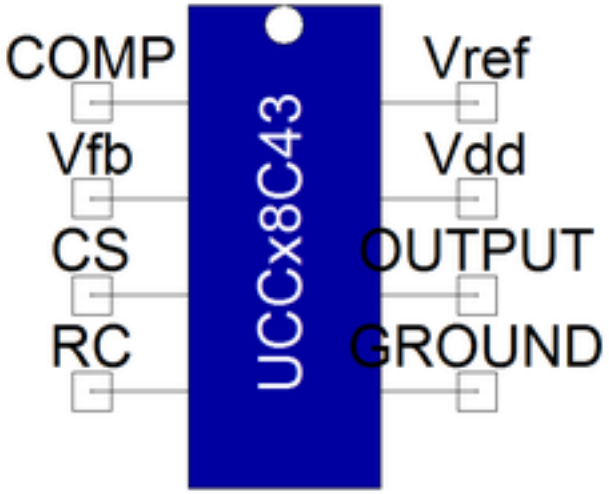
UCCx8C43: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

UCC38C4x family is a high-performance current mode PWM controller. It is an enhanced BiCMOS version with pin-for-pin compatibility to the industry standard *UC384xA* family and *UC384x* family of PWM controllers. In addition, lower startup voltage versions of 7 V are offered as *UCC38C40* and *UCC38C41*.

Providing necessary features to control fixed frequency, peak current-mode power supplies, this family offers the following performance advantages. The device offers high-frequency operation up to 1 MHz with low start-up and operating currents, thus minimizing start-up loss and low

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operating power consumption for improved efficiency. The device also features a very fast current-sense-to-output delay time of 35 ns and a±1 A peak output current capability with improved rise and fall times for driving large external MOSFETs directly.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: operating supply current has been modeled with a constant value current source.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 9V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vdd	Power input

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OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Electrical characteristics VDD = 15 V (See Note 1), RT = 10 kΩ, CT = 3.3 nF, CVDD = 0.1µF and no load on the outputs, TA = -40°C to 105°C for the UCC28C4x and TA = 0°C to 70°C for the UCC38C4x, TA = TJ (unless otherwise noted)

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx8C43 MIN	 TYP	 MAX	MODEL	UNIT
REFERENCE SECTION						
Output Voltage	T_A = 25 °C	4.90	5.00	5.10	5.00	V
Line Regulation	V_{DD}= 12V to 18 V		0.2	20	0.2	mV
Load Regulation	1mA to 20 mA		3	25	0	
Temp. Stability	See Note 2		0.2	0.4	0	mV/ °C
Total Output Variation	See Note 2	4.82		5.18	0	V
Output Noise Voltage	10 Hz to 10 kHz, TA = 25 C See Note 2		50		0	µV
Long TermStability	TA = 125 °C, 1000 Hrs See Note 2		5	25	0	mV
Output Short Circuit		-30	-45	-55	X	mA

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OSCILLATOR SECTION						
Initial Accuracy	TA = 25 °CSee Note 3	50.5	53	55	54	kHz
Voltage Stability	V_{DD}= 12V to 18 V		0.2%	1%	0 %	
Temp. Stability	TMIN toTMAX, See Note 2		1%	2.5%	0 %	
Amplitude	Rt/Ct Pin peak-to-peak		1.9		2.0	V
Discharge current	TA = 25 °C, Rt/Ct=2V See Note 4	7.7	8.4	9.0	8.4	mA
	Rt/Ct=2V, See Note 4	7.2	8.4	9.5	8.4	mA
ERROR AMPLIFIER SECTION						
Feedback Input Voltage	VCOMP= 2.5 V, TA = 25 °C	2.47-5	2.50-0	2.52-5	2.50	V
Input BiasCur-rent	VFB = 5.0V		-0.1	-2.0	0	µA
Open-loopGain (AVOL)	VOUT=2V to 4 V	65	90		90	dB
Unity GainBand-width	See Note 2	1.0	1.5		X	MH-z
PSRR	V_{DD}= 12V to 18 V	60			60	dB
Output SinkCur-rent	VFB = 2.7 V, VCOMP= 1.1 V	2	14		100	mA
Output SourceCur-rent	VFB = 2.3 V, VCOMP= 5 V	-0.5	-1.0		-1.0	
VOUT High	VFB= 2.3 V, RL = 15 k to GND	5	6.8		6.8	V
VOUT Low	VFB= 2.7 V, RL = 15 k to VREF		0.1	1.1	0.1	

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CURRENT SENSE SECTION						
Gain	See Note 5, 6	2.85	3.00	3.15	3.0	V/V
Maximum Input Signal	VFB < 2.4 V	0.9	1.0	1.1	1.0	V
PSRR	V_{DD}= 12V to 18 V, See Note 2, 5		70		X	dB
Input BiasCurrent			-2	-10	0	µA
CS to output delay			35	70	35	ns
COMP to CS offset			1.15		1.15	V
OUTPUT SECTION						
VOUT low (Rds pull-dwn)	Isink =200mA		5.5	15	5.5	Ω
VOUT high (Rds pull-up)	Isource =200mA		10	25	10	
Rise Time	TA = 25°C, CLOAD = 1 nF		50	150	X	ns
Fall Time	TA= 25°C, CLOAD = 1nF		50	150	X	
UNDER-VOLTAGE LOCKOUT SECTION						
Start Threshold		7.8	8.4	9.0	8.4	V
Min. Operating Voltage		7.0	7.6	8.2	7.6	
PWM SECTION						
Maximum DutyCycle		94%	96%		96%	
Minimum DutyCycle				0%	0%	
TOTAL STANDBY CURRENT						
Start-Up Current	VDD-D=UVLO		50	100	0	A

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	start threshold (-0.5)					
Operating SupplyCur-rent	VFB = VCS = 0 V		2.3	3.0	0	mA

X: not modeled
NOTE 1: Adjust VDD above the start threshold before setting at 15 V.
NOTE: 2. Ensured by design. Not production tested.
NOTE: 3. Output frequencies of the UCC38C41, UCC38C44 and the UCC38C45 are half the oscillator frequency.
NOTE: 4. Oscillator discharge current is measured with RT = 10 kΩ to VREF.
NOTE: 5. Parameter measured at trip point of latch with VFB = 0 V.
NOTE: 6. Gain is defined as ACS=ΔVcom/ΔVcs, 0V ≤ Vcs ≤ 900mV

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Example circuit :

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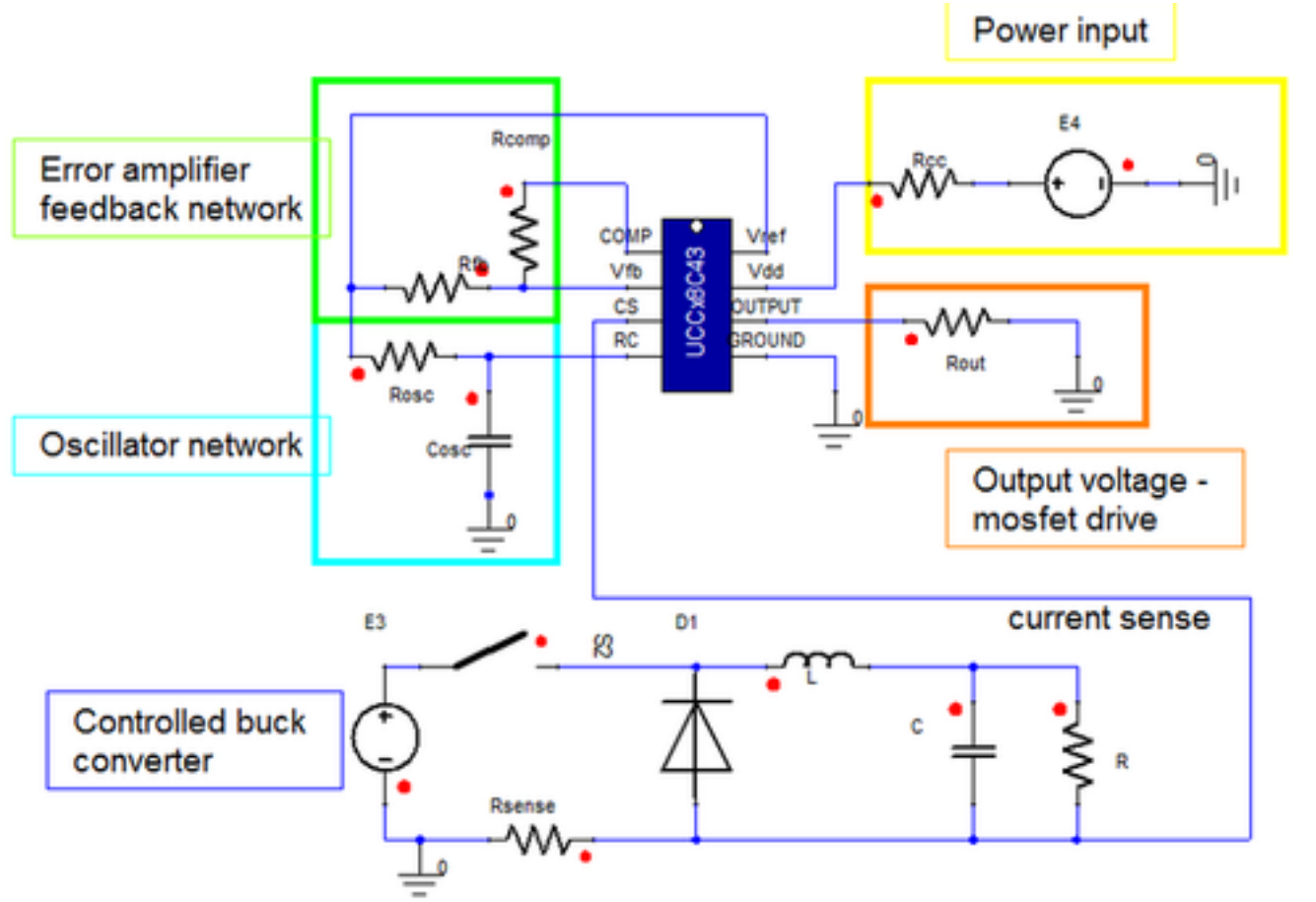

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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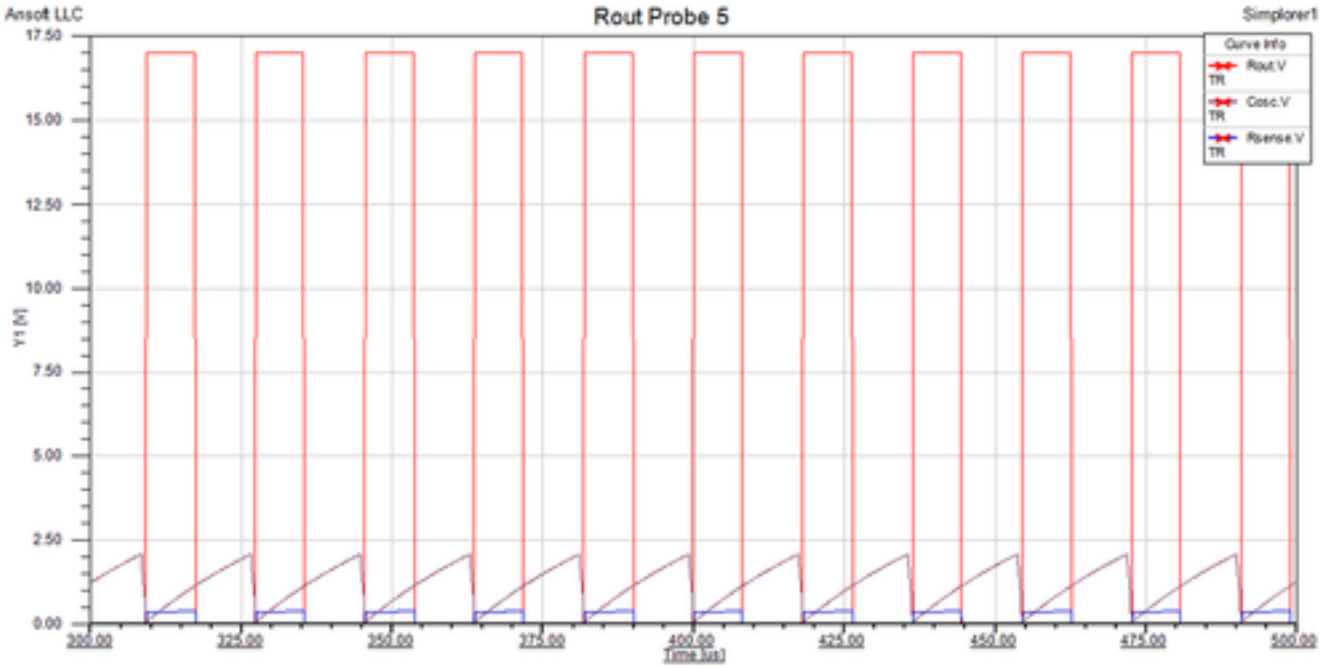

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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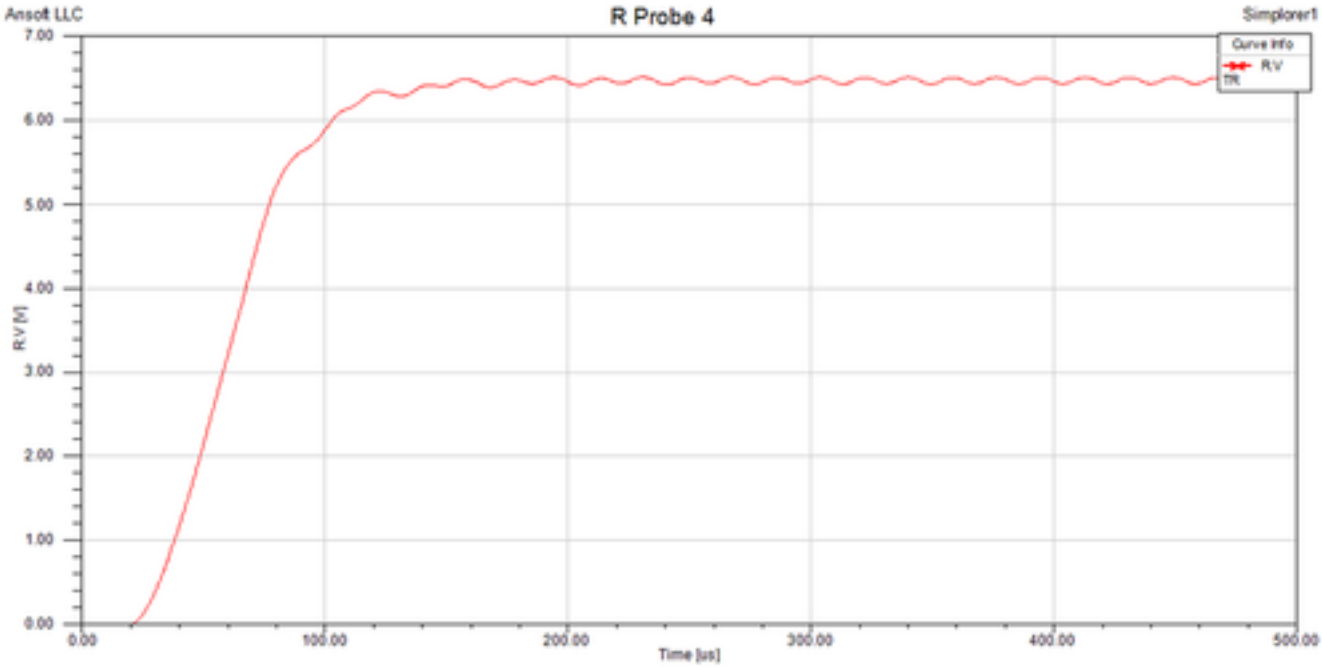

Red: converter output voltage.

Figure 4. Simulation results(b)

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References

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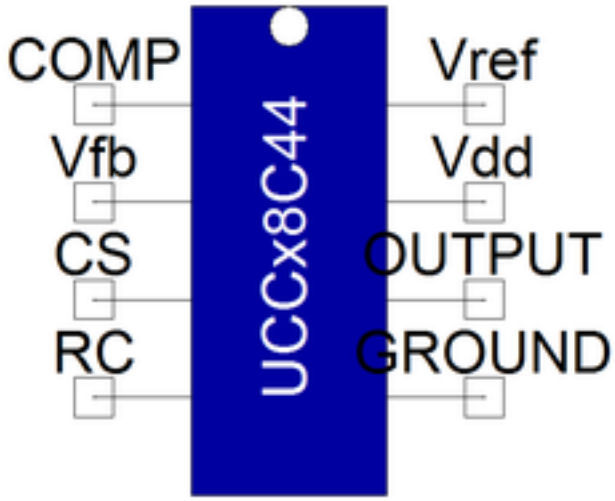
UCCx8C44: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

UCC38C4x family is a high-performance current mode PWM controller. It is an enhanced BiCMOS version with pin-for-pin compatibility to the industry standard *UC384xA* family and *UC384x* family of PWM controllers. In addition, lower startup voltage versions of 7 V are offered as *UCC38C40* and *UCC38C41*.

Providing necessary features to control fixed frequency, peak current-mode power supplies, this family offers the following performance advantages. The device offers high-frequency operation up to 1 MHz with low start-up and operating currents, thus minimizing start-up loss and low

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operating power consumption for improved efficiency. The device also features a very fast current-sense-to-output delay time of 35 ns and a±1 A peak output current capability with improved rise and fall times for driving large external MOSFETs directly.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: operating supply current has been modeled with a constant value current source.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 9V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vdd	Power input

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OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Electrical characteristics VDD = 15 V (See Note 1), RT = 10 kΩ, CT = 3.3 nF, CVDD = 0.1µF and no load on the outputs, TA = -40°C to 105°C for the UCC28C4x and TA = 0°C to 70°C for the UCC38C4x, TA = TJ (unless otherwise noted)

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx8C44 MIN	 TYP	 MAX	MODEL	UNIT
REFERENCE SECTION						
Output Voltage	T_A = 25 °C	4.90	5.00	5.10	5.00	V
Line Regulation	V_{DD}= 12V to 18 V		0.2	20	0.2	mV
Load Regulation	1mA to 20 mA		3	25	0	
Temp. Stability	See Note 2		0.2	0.4	0	mV/°C
Total Output Variation	See Note 2	4.82		5.18	0	V
Output Noise Voltage	10 Hz to 10 kHz, TA = 25 C See Note 2		50		0	µV
Long TermStability	TA = 125 °C, 1000 Hrs See Note 2		5	25	0	mV
Output Short Circuit		-30	-45	-55	X	mA

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OSCILLATOR SECTION						
Initial Accuracy	TA = 25 °CSee Note 3	50.5	53	55	54	kHz
Voltage Stability	V_{DD}= 12V to 18 V		0.2%	1%	0 %	
Temp. Stability	TMIN toTMAX, See Note 2		1%	2.5%	0 %	
Amplitude	Rt/Ct Pin peak-to-peak		1.9		2.0	V
Discharge current	TA = 25 °C, Rt/Ct=2V See Note 4	7.7	8.4	9.0	8.4	mA
	Rt/Ct=2V, See Note 4	7.2	8.4	9.5	8.4	mA
ERROR AMPLIFIER SECTION						
Feedback Input Voltage	VCOMP= 2.5 V, TA = 25 °C	2.47-5	2.50-0	2.52-5	2.50	V
Input BiasCur-rent	VFB = 5.0V		-0.1	-2.0	0	µA
Open-loopGain (AVOL)	VOUT=2V to 4 V	65	90		90	dB
Unity GainBand-width	See Note 2	1.0	1.5		X	MH-z
PSRR	V_{DD}= 12V to 18 V	60			60	dB
Output SinkCur-rent	VFB = 2.7 V, VCOMP= 1.1 V	2	14		100	mA
Output SourceCur-rent	VFB = 2.3 V, VCOMP= 5 V	-0.5	-1.0		-1.0	
VOUT High	VFB= 2.3 V, RL = 15 k to GND	5	6.8		6.8	V
VOUT Low	VFB= 2.7 V, RL = 15 k to VREF		0.1	1.1	0.1	

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CURRENT SENSE SECTION						
Gain	See Note 5, 6	2.85	3.00	3.15	3.0	V/V
Maximum Input Signal	VFB < 2.4 V	0.9	1.0	1.1	1.0	V
PSRR	V_{DD}= 12V to 18 V, See Note 2, 5		70		X	dB
Input BiasCurrent			-2	-10	0	µA
CS to output delay			35	70	35	ns
COMP to CS offset			1.15		1.15	V
OUTPUT SECTION						
VOUT low (Rds pulldwn)	Isink =200mA		5.5	15	5.5	Ω
VOUT high (Rds pullup)	Isource =200mA		10	25	10	
Rise Time	TA = 25°C, CLOAD = 1 nF		50	150	X	ns
Fall Time	TA= 25°C, CLOAD = 1nF		50	150	X	
UNDER-VOLTAGE LOCKOUT SECTION						
Start Threshold		13.5	14.5	15.5	14.5	V
Min. Operating Voltage		8	9	10	9	
PWM SECTION						
Maximum DutyCycle		47%	48%		48%	
Minimum DutyCycle				0%	0%	
TOTAL STANDBY CURRENT						
Start-Up Current	VDD-D=UVLO		50	100	0	A

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	start threshold (-0.5)					
Operating SupplyCur-rent	VFB = VCS = 0 V		2.3	3.0	0	mA

X: not modeled
NOTE 1: Adjust VDD above the start threshold before setting at 15 V.
NOTE: 2. Ensured by design. Not production tested.
NOTE: 3. Output frequencies of the UCC38C41, UCC38C44 and the UCC38C45 are half the oscillator frequency.
NOTE: 4. Oscillator discharge current is measured with RT = 10 kΩ to VREF.
NOTE: 5. Parameter measured at trip point of latch with VFB = 0 V.
NOTE: 6. Gain is defined as ACS=ΔVcom/ΔVcs, 0V ≤ Vcs ≤ 900mV

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Example circuit :

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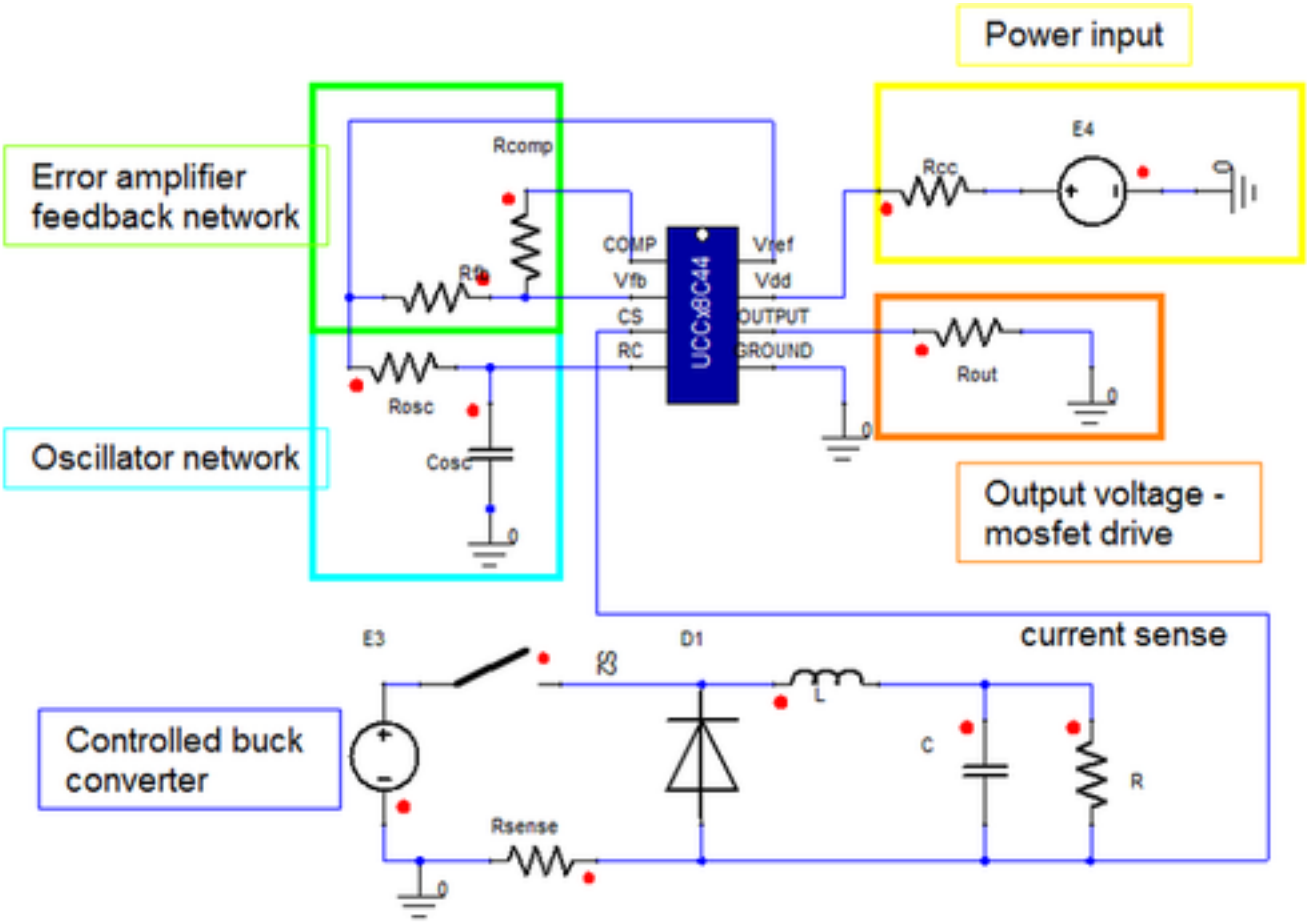

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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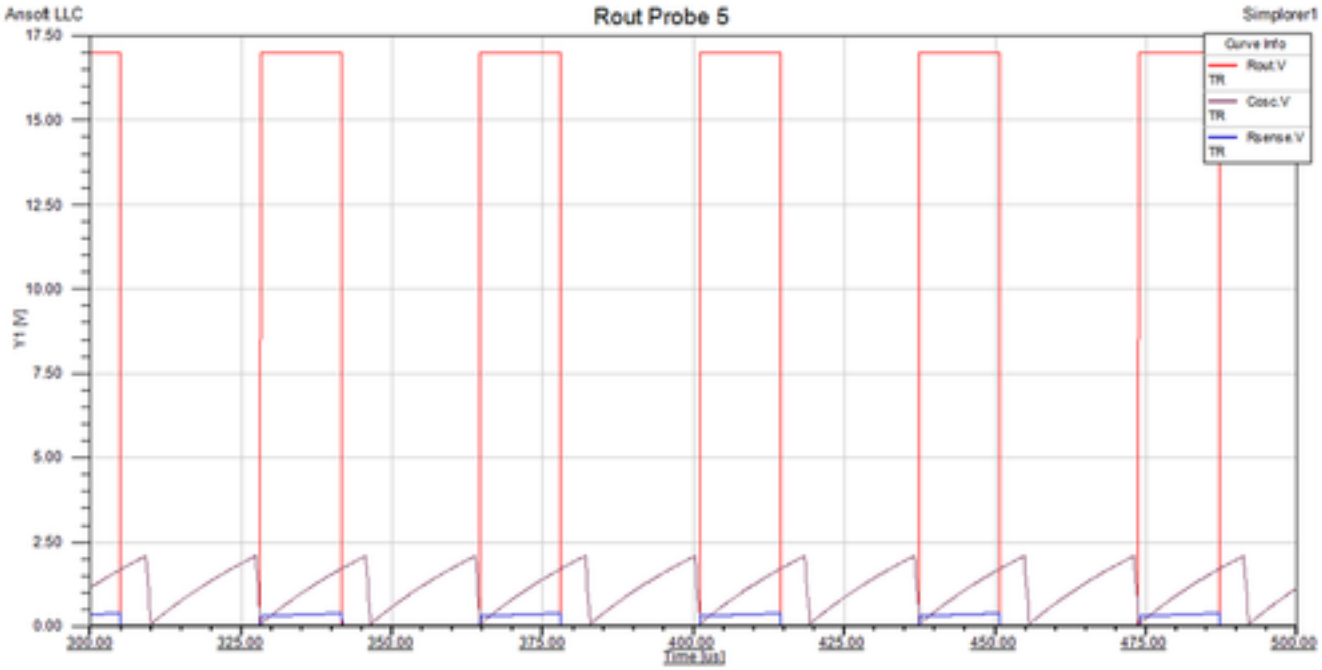

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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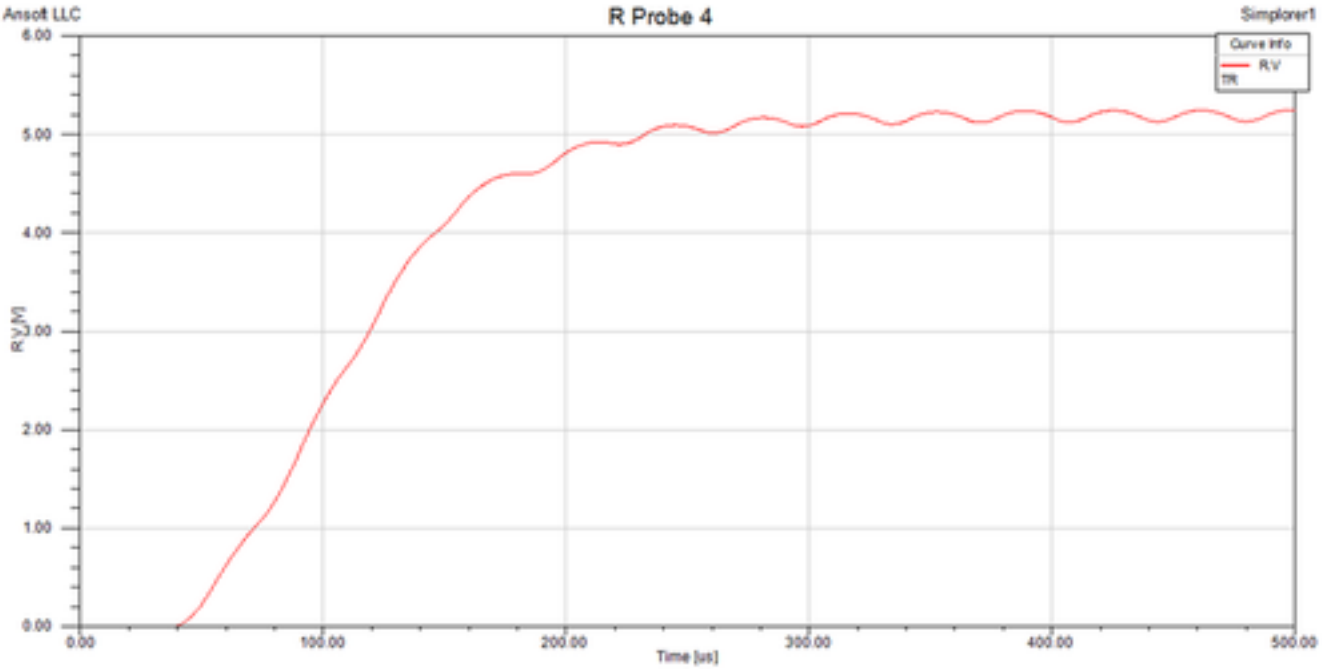

Red: converter output voltage.

Figure 4. Simulation results(b)

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References

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UCCx8C45: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

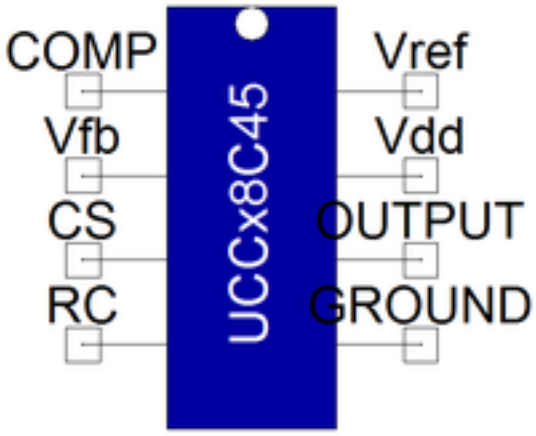

Figure 1. Component symbol

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Description

UCC38C4x family is a high-performance current mode PWM controller. It is an enhanced BiCMOS version with pin-for-pin compatibility to the industry standard *UC384xA* family and *UC384x* family of PWM controllers. In addition, lower startup voltage versions of 7 V are offered as *UCC38C40* and *UCC38C41*.

Providing necessary features to control fixed frequency, peak current-mode power supplies, this family offers the following performance advantages. The device offers high-frequency operation up to 1 MHz with low start-up and operating currents, thus minimizing start-up loss and low

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operating power consumption for improved efficiency. The device also features a very fast current-sense-to-output delay time of 35 ns and a±1 A peak output current capability with improved rise and fall times for driving large external MOSFETs directly.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: operating supply current has been modeled with a constant value current source.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 9V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator
RC	Oscillator timing pin
Vref	Voltage reference
Vdd	Power input

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OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Electrical characteristics VDD = 15 V (See Note 1), RT = 10 kΩ, CT = 3.3 nF, CVDD = 0.1µF and no load on the outputs, TA = -40°C to 105°C for the UCC28C4x and TA = 0°C to 70°C for the UCC38C4x, TA = TJ (unless otherwise noted)

Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCCx8C45 MIN	 TYP	 MAX	MODEL	UNIT
REFERENCE SECTION						
Output Voltage	T_A = 25 °C	4.90	5.00	5.10	5.00	V
Line Regulation	V_{DD}= 12V to 18 V		0.2	20	0.2	mV
Load Regulation	1mA to 20 mA		3	25	0	
Temp. Stability	See Note 2		0.2	0.4	0	mV/ °C
Total Output Variation	See Note 2	4.82		5.18	0	V
Output Noise Voltage	10 Hz to 10 kHz, TA = 25 C See Note 2		50		0	µV
Long TermStability	TA = 125 °C, 1000 Hrs See Note 2		5	25	0	mV
Output Short Circuit		-30	-45	-55	X	mA

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OSCILLATOR SECTION						
Initial Accuracy	TA = 25 °CSee Note 3	50.5	53	55	54	kHz
Voltage Stability	V_{DD}= 12V to 18 V		0.2%	1%	0 %	
Temp. Stability	TMIN toTMAX, See Note 2		1%	2.5%	0 %	
Amplitude	Rt/Ct Pin peak-to-peak		1.9		2.0	V
Discharge current	TA = 25 °C, Rt/Ct=2V See Note 4	7.7	8.4	9.0	8.4	mA
	Rt/Ct=2V, See Note 4	7.2	8.4	9.5	8.4	mA
ERROR AMPLIFIER SECTION						
Feedback Input Voltage	VCOMP= 2.5 V, TA = 25 °C	2.47-5	2.50-0	2.52-5	2.50	V
Input BiasCur-rent	VFB = 5.0V		-0.1	-2.0	0	µA
Open-loopGain (AVOL)	VOUT=2V to 4 V	65	90		90	dB
Unity GainBand-width	See Note 2	1.0	1.5		X	MH-z
PSRR	V_{DD}= 12V to 18 V	60			60	dB
Output SinkCur-rent	VFB = 2.7 V, VCOMP= 1.1 V	2	14		100	mA
Output SourceCur-rent	VFB = 2.3 V, VCOMP= 5 V	-0.5	-1.0		-1.0	
VOUT High	VFB= 2.3 V, RL = 15 k to GND	5	6.8		6.8	V
VOUT Low	VFB= 2.7 V, RL = 15 k to VREF		0.1	1.1	0.1	

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CURRENT SENSE SECTION						
Gain	See Note 5, 6	2.85	3.00	3.15	3.0	V/V
Maximum Input Signal	VFB < 2.4 V	0.9	1.0	1.1	1.0	V
PSRR	V_{DD}= 12V to 18 V, See Note 2, 5		70		X	dB
Input BiasCurrent			-2	-10	0	µA
CS to output delay			35	70	35	ns
COMP to CS offset			1.15		1.15	V
OUTPUT SECTION						
VOUT low (Rds pull-dwn)	Isink =200mA		5.5	15	5.5	Ω
VOUT high (Rds pull-up)	Isource =200mA		10	25	10	
Rise Time	TA = 25°C, CLOAD = 1 nF		50	150	X	ns
Fall Time	TA= 25°C, CLOAD = 1nF		50	150	X	
UNDER-VOLTAGE LOCKOUT SECTION						
Start Threshold		7.8	8.4	9.0	8.4	V
Min. Operating Voltage		7.0	7.6	8.2	7.6	
PWM SECTION						
Maximum DutyCycle		47%	48%		48%	
Minimum DutyCycle				0%	0%	
TOTAL STANDBY CURRENT						
Start-Up Current	VDD-D=UVLO		50	100	0	A

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	start threshold (-0.5)					
Operating SupplyCur-rent	VFB = VCS = 0 V		2.3	3.0	0	mA

X: not modeled
NOTE 1: Adjust VDD above the start threshold before setting at 15 V.
NOTE: 2. Ensured by design. Not production tested.
NOTE: 3. Output frequencies of the UCC38C41, UCC38C44 and the UCC38C45 are half the oscillator frequency.
NOTE: 4. Oscillator discharge current is measured with RT = 10 kΩ to VREF.
NOTE: 5. Parameter measured at trip point of latch with VFB = 0 V.
NOTE: 6. Gain is defined as ACS=ΔVcom/ΔVcs, 0V ≤ Vcs ≤ 900mV

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Example circuit :

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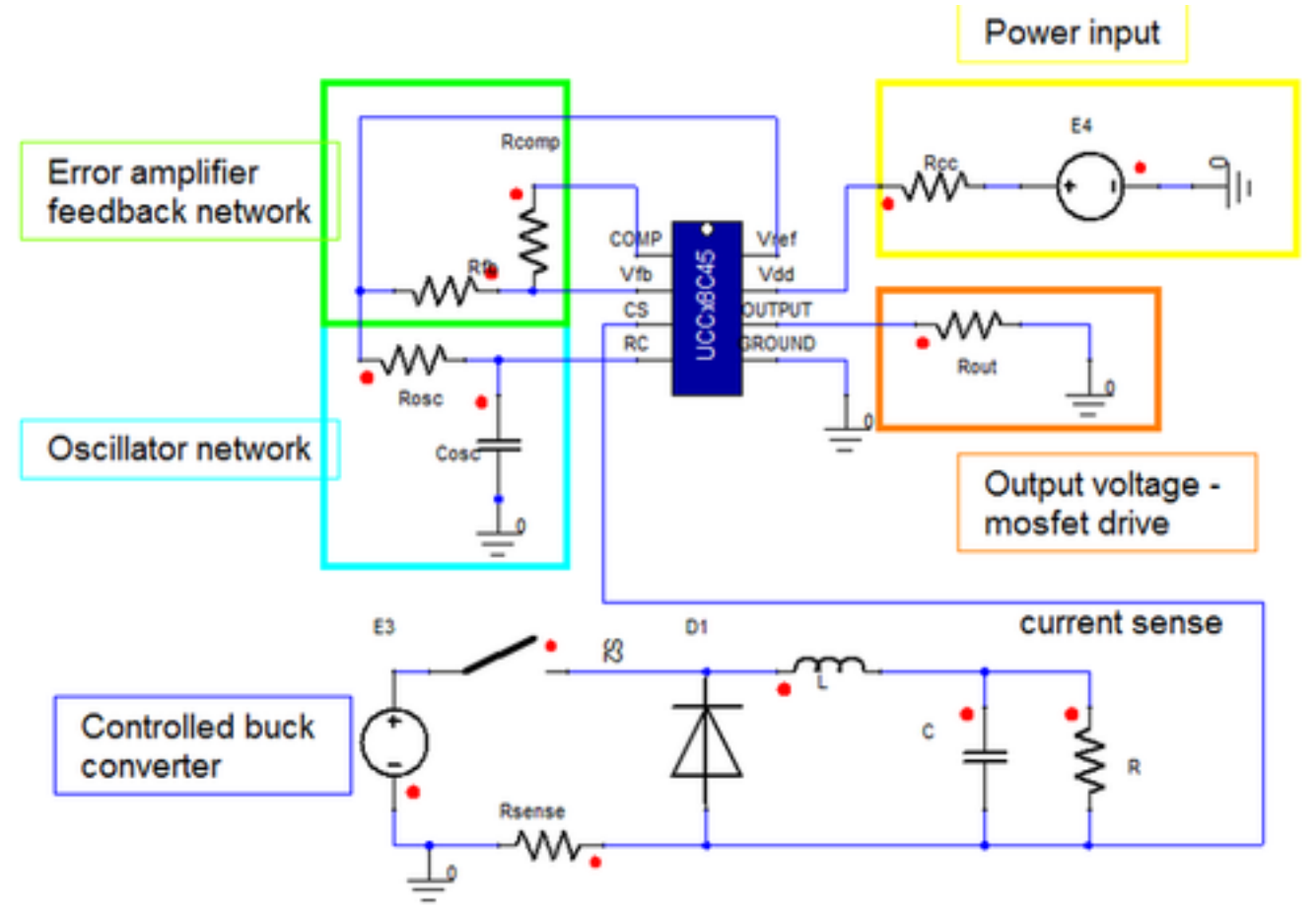

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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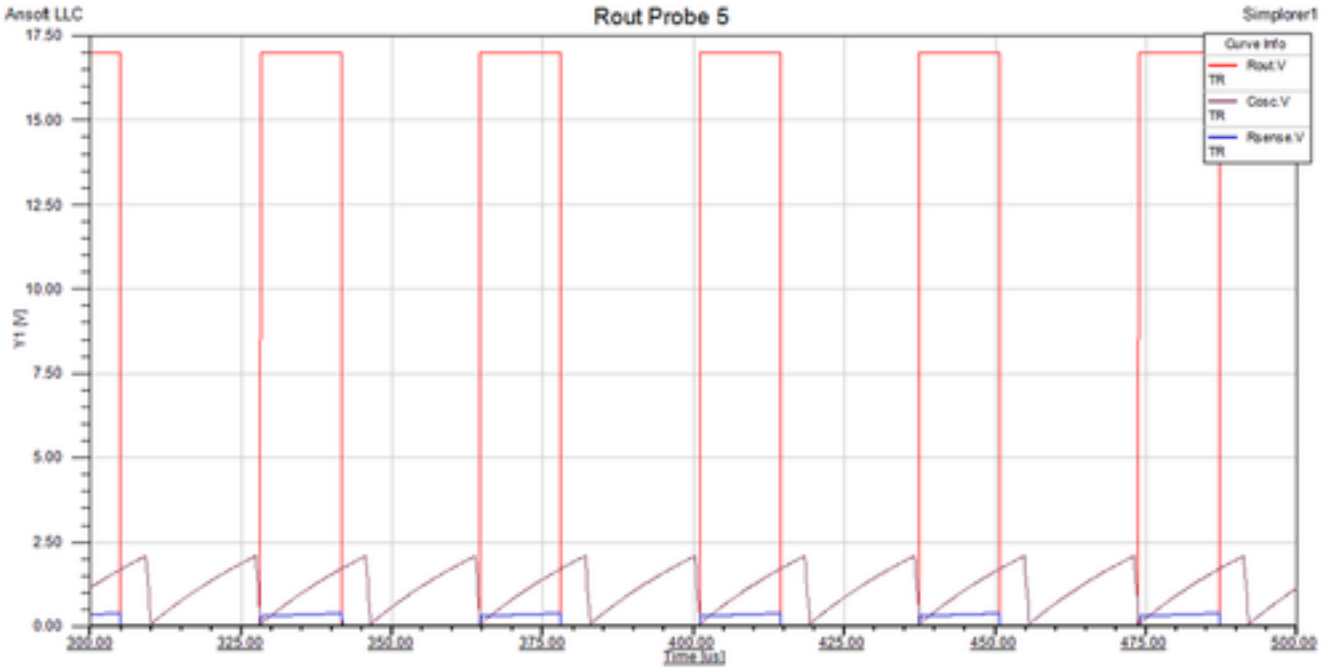

Red: output driver voltage

Purple: oscillator voltage

Blue: shunt resistor voltage

Figure 3. Simulation results(a)

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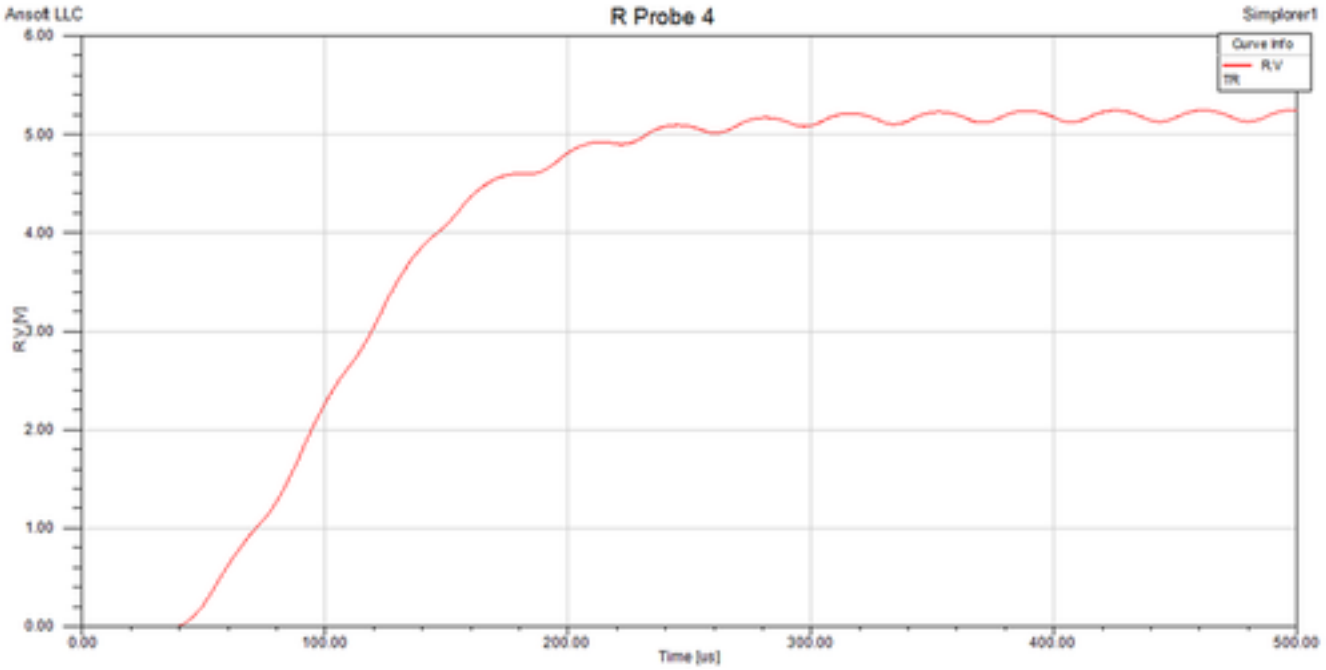

Red: converter output voltage.

Figure 4. Simulation results(b)

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References

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UCx524: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

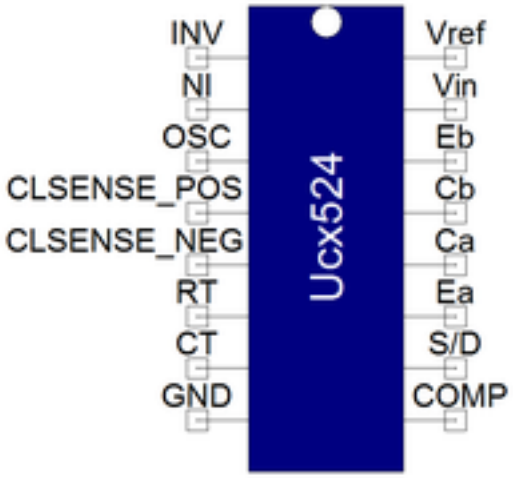

Figure 1. Component symbol

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Description

The *UC1524*, *UC2524* and *UC3524* incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The *UC1524* family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain

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comparator, and current-limiting and shut-down circuitry. The *UC1524* is characterized for operation over the full military temperature range of -55°C to +125°C. The *UC2524* and *UC3524* are designed for operation from -25°C to +85°C and 0° to +70°C, respectively.

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Table 1

PIN	NAME	FUNCTION
1	INV INPUT	Error Amplifier inverting input
2	NON INV INPUT	Error Amplifier non inverting input
3	OSC OUT	Oscilator output and syncrhonous operation input
4	CLSENSE(+)	Current limit inverting input
5	CLSENSE(-)	Current limit non inverting input
6	RT	Timing Resistor
7	CT	Timing Capacitor
8	GND	Ground
9	COMP	Compensation
10	S/D	Shutdown
11	Ea	A Output Emitter
12	Ca	A Output Collector
13	Cb	B Output Emitter
14	Eb	B Output Collector
15	Vin	Input Voltage
16	Vref	Voltage Reference

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Parameters

Comparison between model and real component.

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Table 2

PARAMETE-RS	TEST CONDITIO-NS	MIN	TYP	MA-X	MODE-L	UNIT-S
Reference Section						
Output Voltage		4.8	5.0	5.2	5	V
Line Regu-lation	Vin = 8 to 40 V		10	20	0	mV
Load Regu-lation	IL = 0 to 20 mA		20	50	20	mV
Ripple Rejec-tion	f = 120 Hz		66		-	dB
Short CircuitCurrent Limit	Vref = 0		100		100	mA
Temperature Stability	Over Oper-atingTem-perature Range		0.3		-	%
Long TermStability	T = 1000 Hrs		20		-	mV
OscillatorSection						
Maximum Fre-quency	C = 0.001 mF, R = 2 kohm		300		*	kHz
Initial Accur-acy	RT and CT constant		5		*	%
Voltage Stab-ility	Vin = 8 to 40 V			1	0	%
Temperature Stability	Over Oper-atingTem-perature Range			5	-	%
Output Amplitude			3.5		3.5	V
Output Pulse Width	CT = 0.01mF		0.5		0.5	us
Error AmplifierSection						
Input Offset Voltage	Vcm = 2.5V		0.5	5	0.5	mV
Input BiasCur-rent	Vcm = 2.5V		2	10	2	uA
Open LoopVoltage Gain		72	80		80	dB
Common		1.8		3.4	0.5/3.8	V

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ModeVoltage						
Common ModeRejec-tion Ratio			70		-	dB
Small SignalBand-width	Av = 0 dB		3		3	MHz
Output Voltage		0.5		3.8	0.5 / 3.8	V
ComparatorSection						
Duty Cycle	% Each Out-put On	0		45	0 / 45	%
Input Threshold	Zero Duty-Cycle		1		0.5	V
	Maximum Duty-Cycle		3.5		3.8	V
Input Bias Current			1		-	uA
Current Limiting Section						
Sense Voltage		190	200	210	200	mV
Sense Voltage T.C.			0.2		-	mV/°C
Common Mode Voltage		-1		+1	-	V
Output Section (Each Output)						
Collector-Emitter Voltage		40			-	V
Collector Leakage Cur-rent	Vce = 40V		0.1	50	0	uA
Saturation Voltage	Ic = 50mA		1	2	1	V
Emitter Out-put Voltage	Vin = 20V	17	18		-	V
Rise Time	Rc = 2kΩ		0.2		0.1	us
Fall Time	Rc = 2kΩ		0.1		0.1	us
Total Standby Current	Vin = 40V		8	10	8	mA

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Examples

Example circuit :

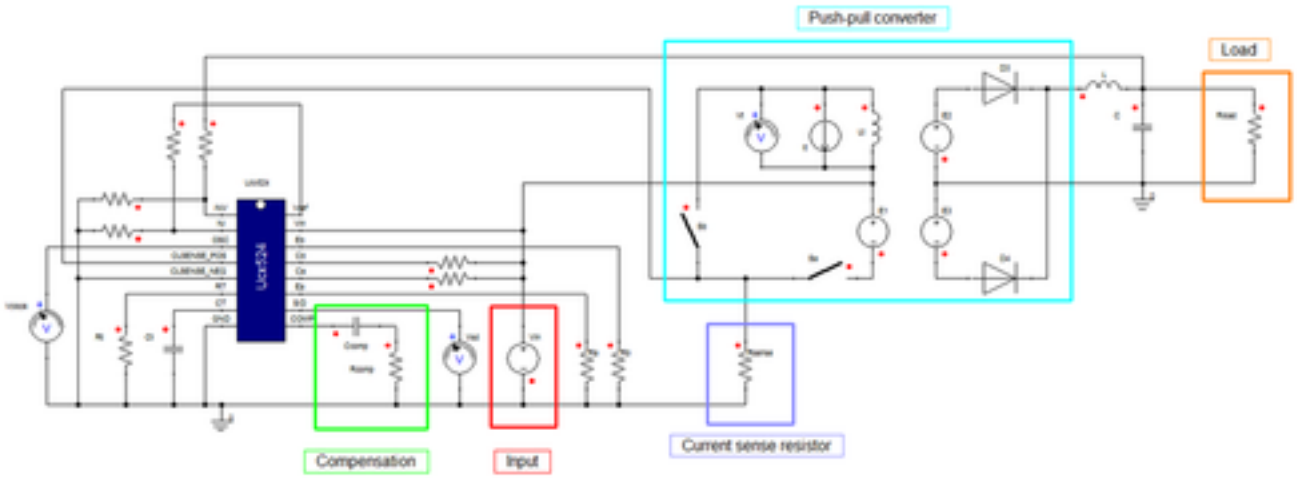

Figure 2. Example Circuit

Simulation results :

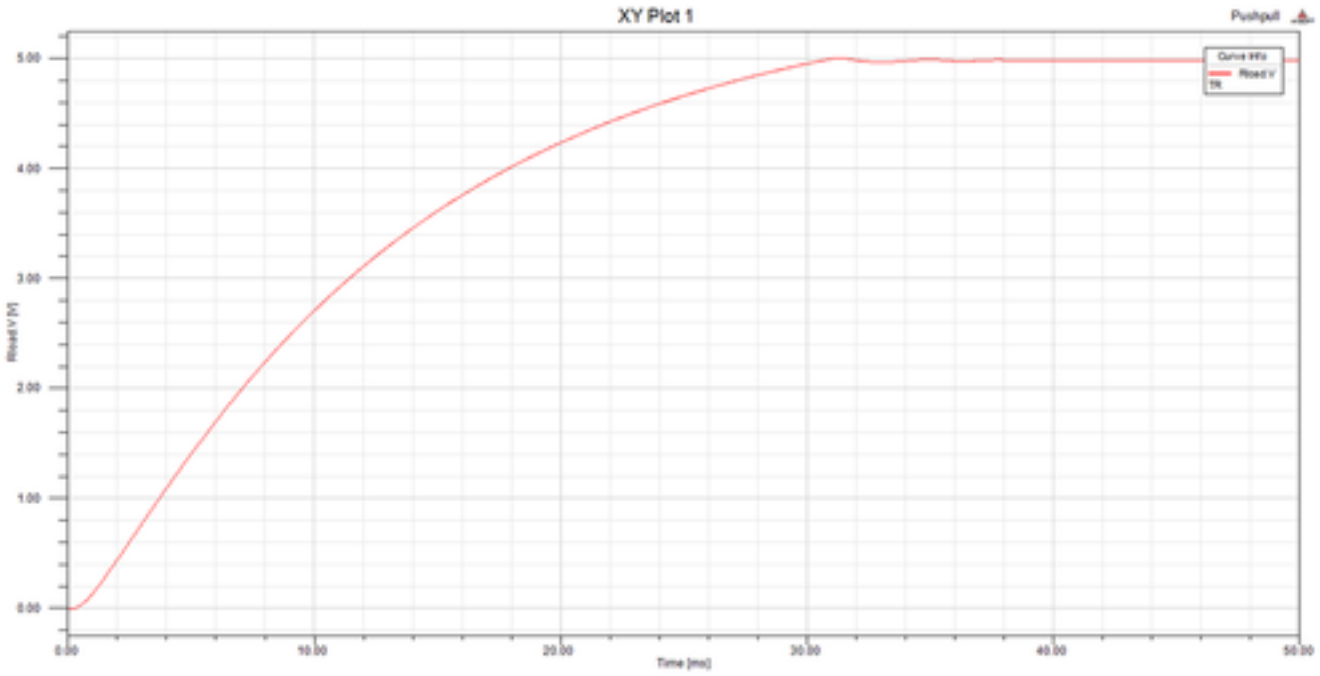

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Figure 3. Simulation results

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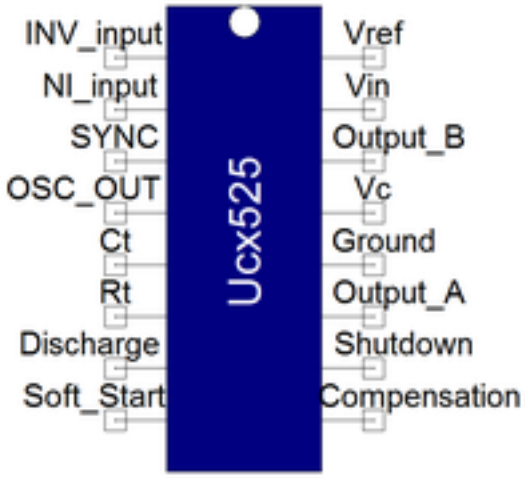
UCx525: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UC1525A/1527A* series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1-V reference is trimmed to 1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be made secondary or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provides a wide range of dead-time adjustment.

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These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	INV INPUT	Error Amplifier inverting input
2	NI INPUT	Error Amplifier non inverting input
3	SYNC	Synchronization Pin
4	OSC Output	Oscilator output and syncrhonous operation input
5	CT	Timing Capacitor
6	RT	Timing Resistor
7	Discharge	Timing Capacitor Discharge Pin
8	Soft Start	Soft Start
9	COMP	Compensation
10	Shutdown	Shutdown
11	Output A	Output A
12	Ground	Ground
13	Vc	Collector Voltage
14	Output B	Output B
15	Vin	Input Voltage
16	Vref	Voltage Reference

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Parameters

Comparison between model and real component.

Table 2

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MODEL	UNITS
Reference						
Output voltage		4.05	5.10	5.15	5.1	V
Line regulation	Vin = 8 to 35 V		10	20	0	mV
Load regulation	IL = 0 to 20 mA		20	50	20	mV
Temperature stability	Over OperatingTemperature Range		20	50	-	mV
Total output variation	f = 120 Hz	5.0		5.2	5.08/5.-1	V
Short circuitcurrent limit	Vref = 0		80	100	80	mA
Output noisevoltage			40	200	-	uVrms
Long termstability	T = 1000 Hrs		20	50	0	mV
Oscillator Section						
Initial accuracy			2	6	-	%
Voltage stability	Vin = 8 to 35 V		0.3	1	-	%
Temperature stability	Over operatingrange		3%	6%	-	%
Minimum frequency	C = 0.1 uF R = 200 kohm			120	-	Hz
Maximum frequency	C = 470 pF R = 2 kohm	400			-	kHz
Current mirror	Irt = 2 mA	1.7	2	2.2	2	mA
Clock amplitude		3	3.5		3.5	V

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Clock width		0.3	0.5	1.0	0.5	us
Syn-cronization threshold		1.2	2.0	2.8		V
Sync input cur-rent	Sync vol-gate = 3.5		1	2.5		mA
Error AmplifierSection						
Input offset voltage			0.5	5	0	mV
Input biascur-rent			1	10	0	uA
Input offset cur-rent			1	10	0	uA
DC open loopGain	RL ≥ 10 MΩ	60	75		75	dB
Gain-band-width product	AV = 0 dB	1	2		2	MHz
DC transcon-ductance	30 kΩ ≤ RL ≤ 1 MΩ	1.1	1.5		1.5	mS
Low-level out-put volgate			0.2	0.5	0.2	V
High-level out-put volgate		3.8	5.6		5.6	V
Common moderejection		60	75		-	dB
Supply voltaje rejection		50	60		-	dB
PWM Comparator						
Minimum dutycycle				0	0	%
Maximum dutycycle		45	49		49	%
Input Threshold	Zero Duty-Cycle	0.7	0.9		0.7	V
	Max Duty-Cycle		3.3	3.6	3.5	V
Input Bias Cur-rent			0.05	1	0	uA
Shutdown						
Soft-start cur-rent	VSD = 0 V, VSS = 0 V	25	50	80	50	uA
Soft-start low level	VSD = 2.5 V		0.4	0.7	0	V
Shutdown threshold		0.6	0.8	1.0	0.8	V
Shutdown input current	VSD = 2.5 V		0.4	1.0	0	mA

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Shutdown delay	VSD = 2.5 V		0.2	0.5	0.2	us
Output Drivers (each output)						
Low-level output voltage	Isink = 20 mA		0.2	0.4	0	V
PARAMETERS	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MODEL**	**UNITS**
	Isink = 100 mA		1.0	2.0	0	V
High-level output voltage	Isource = 20 mA	18	19		19.6	V
	Isource = 100 mA	17	18		18	V
Undervoltage lockout	Vcomp, VSS = High	6	7	8	7	V
VCÂ OFF Current				200	0	uA
Rise Time	CL = 1 nF		100	600	100	ns
Fall Time	CL = 1 nF		50	300	50	ns
Total Sandby Current	VIN = 35 V		14	20	14	mA

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Example circuit :

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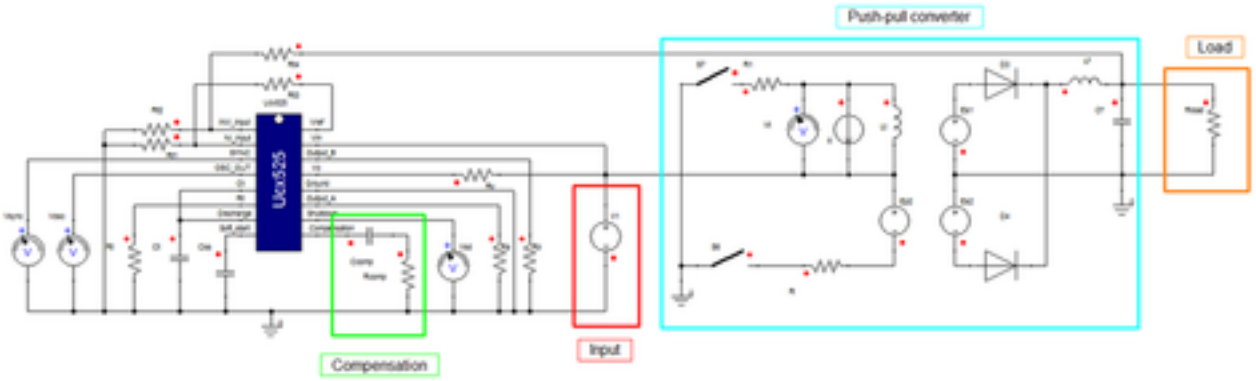

Figure 2. Example Circuit

Simulation results :

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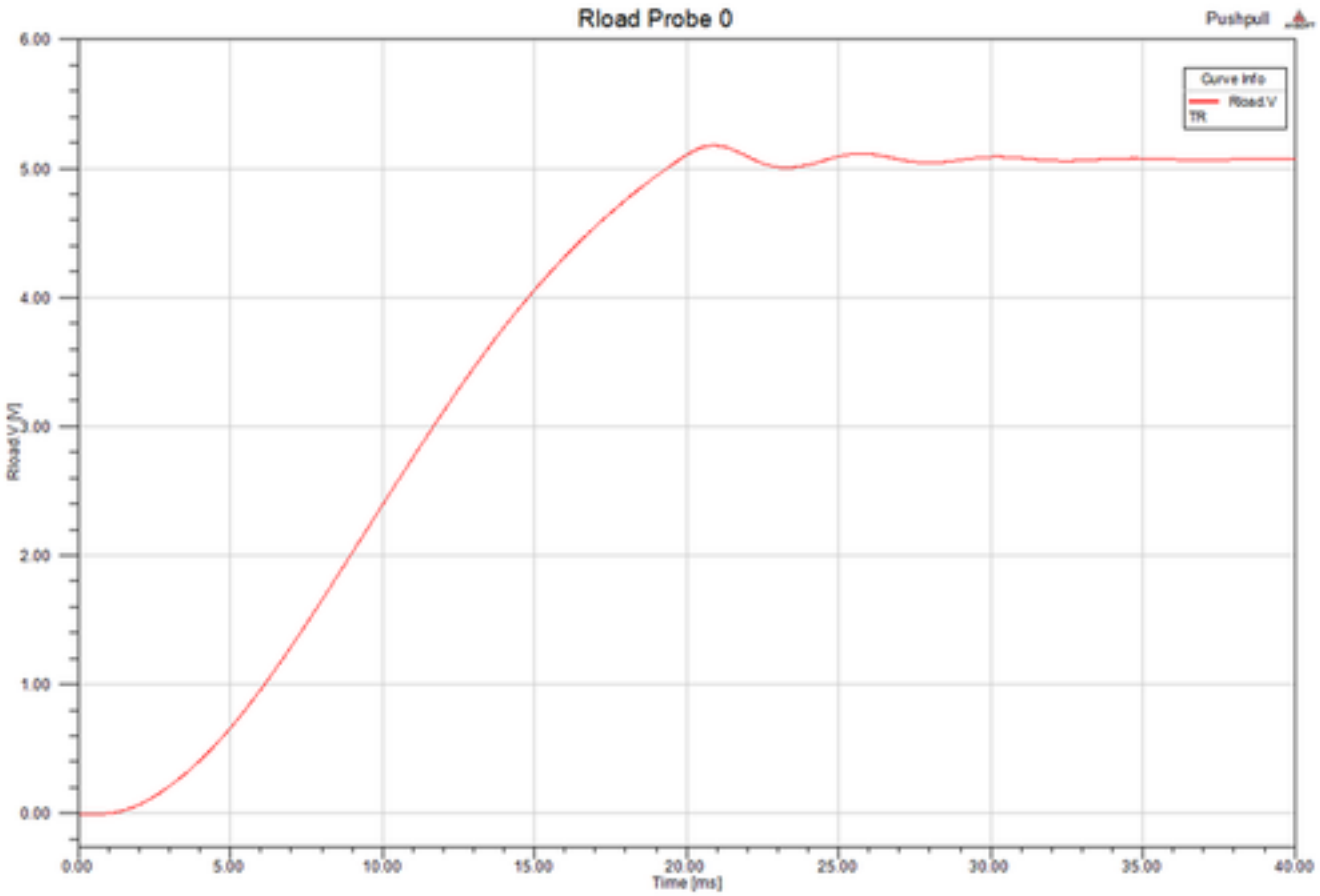

Figure 3. Simulation results

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References

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UCx823: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

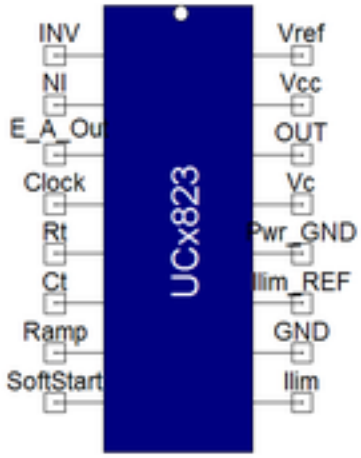

Figure 1. Component symbol

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Description

The *UCx823* family of PWM control ICs is optimized for high frequency switched mode power supply applications. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the

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output is high impedance. The current limit reference is a DC input voltage to the current limit comparator.

These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current and voltage sense: a voltmeter measures the voltage on Ramp pin. The input impedance is infinite.
• Current limit and current limit reference: voltmeters measure the voltage on these pins to set the overcurrent protection limits. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5.1V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 9.2V, the protection activates and the output and the reference fall to zero), the oscillator, the output voltage and the overcurrent protection.

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Conservative Pins

Table 1

Symbol	Description
INV	Error amplifier inverting intput
NI	Error amplifier non-inverting input
E_A_Out	Output of the error amplifier
Clock	Clock output

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Rt	Oscillator resistor pin
Ct	Oscillator capacitor pin
Ramp	Ramp comparator input
SoftStart	Soft start timing configuration pin
Vref	Voltage reference
Vcc	Logic supply voltage
OUT	Driver output
Vc	Input voltage
Pwr_GND	Power ground
Ilim_REF	Current limit reference
GND	Reference ground
Ilim	Current limit comparator input

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Parameters

Comparison between model and real component.

Unless otherwise noted, these specifications apply for RT = 3.65k, CT = 1nF, VCC = 15V, 0°C < TA < +70°C for the UC3823, -25°C < TA < +85°C for the UC2823, and -55°C < TA < +125°C for the UC1823, TA = TJ.

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Table 2

PARAMETER	TEST CONDITIONS	UCx823			MODEL	UNITS
		MIN	TYP	MAX		
Reference Section						
Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	5.10	V
Line Regulation	10 < V_{CC} < 30V		2	20	2	mV
Load Regulation	1 < I_O < 10mA		5	20	0	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4	0	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	5.10-5.20	
Output Noise Voltage*	10Hz < f < 10kHz		50		0	µV
Long TermStability*	T_J = 125°C, 1000 hrs.		5	25	0	mV
Short CircuitCurrent	V_{REF}=0V	-15	-50	-100	∞	mA
Oscillator Section						
Initial Accuracy*	T_J=25°C	360	400	440	386	kHz
Voltage Stability*	10 < V_{CC} < 30V		0.2	2	0	%
Temperature Stability*	T_{MIN} <T_A < T_{MAX}		5		X	%
Total Variation*	Line, Temp.	340		460	386	kHz
Clock Out High		3.9	4.5		4.5	V
Clock OutLow			2.3	2.9	2.3	V
Ramp Peak*		2.6	2.8	3.0	2.8	V
Ramp Valley*		0.7	1.0	1.25	1.0	V
Ramp Valley toPeak*		1.6	1.8	2.0	1.8	V

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Error AmplifierSection						
Input Offset Voltage				10	0	mV
Input BiasCurrent			0.6	3	0	µA
Input Offset Current			0.1	1	0	µA
Open LoopGain	1 < V_O < 4V	60	95		95	dB
CMRR	1.5 < V_{CM} < 5.5V	75	95		95	dB
PSRR	10 < V_{CC} < 30V	85	110		110	dB
Output SinkCurrent	$V_{PIN\ 3}$ =1V	1	2.5		0	mA
Output SourceCur-rent	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		0	mA
Output High Voltage	$I_{PIN\ 3}$ = 0.5mA	4.0	4.7	5.0	4.8	V
Output LowVoltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	V
Unity GainBand-width*		3	5.5		X	MHz
Slew Rate*		6	12		X	V/ S
PWM ComparatorSection						
Pin 7 BiasCurrent	$V_{PIN\ 7}$ = 0V		-1	-5	0	µA
Duty CycleRange		0		85	90	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.25	V
Delay to Out-put*			50	80	0	ns
Soft-Start Section						
Charge Cur-rent	$V_{PIN\ 8}$ = 0.5V	3	9	20	9	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			∞	mA
Current Limit/ShutdownSection						
Pin 9 BiasCurrent	0 < $V_{PIN\ 9}$ < 4V			10	0	µA

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Current Limit Offset	$V_{PIN\ 11}$ = 1.1V			15	0	mV
Current Limit Common Mode Range ($V_{PIN\ 11}$)		1.0		1.25		V
Shutdown Threshold		1.25	1.40	1.55	1.4	V
Delay to Output*			50	80	0	ns
Output Section						
Output LowLevel	I_{OUT} = 20mA		0.25	0.40	0	V
	I_{OUT} = 200mA		1.2	2.2	0	V
Output High Level	I_{OUT} = 20mA	13.0	13.5		15	V
	I_{OUT} = 200mA	12.0	13.0		15	V
Collector Leakage	V_C = 30V		100	500	0	µA
Rise/Fall Time*	C_L = 1nF		30	60	0	ns
Under-Voltage Lockout Section						
Start Threshold		8.8	9.2	9.6	9.2	V
UVLO Hysteresis		0.4	0.8	1.2	0.8	V
Supply Current						
Start Up Current	V_{CC} = 8V		1.1	2.5	0	mA
I_{CC}	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ =0V, $V_{PIN\ 2}$ = 1V		22	33	0	mA

**This parameter is not 100% tested in production but guaranteed by design*
X: Not implemented

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Input/Output Quantities

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Examples

Example circuit :

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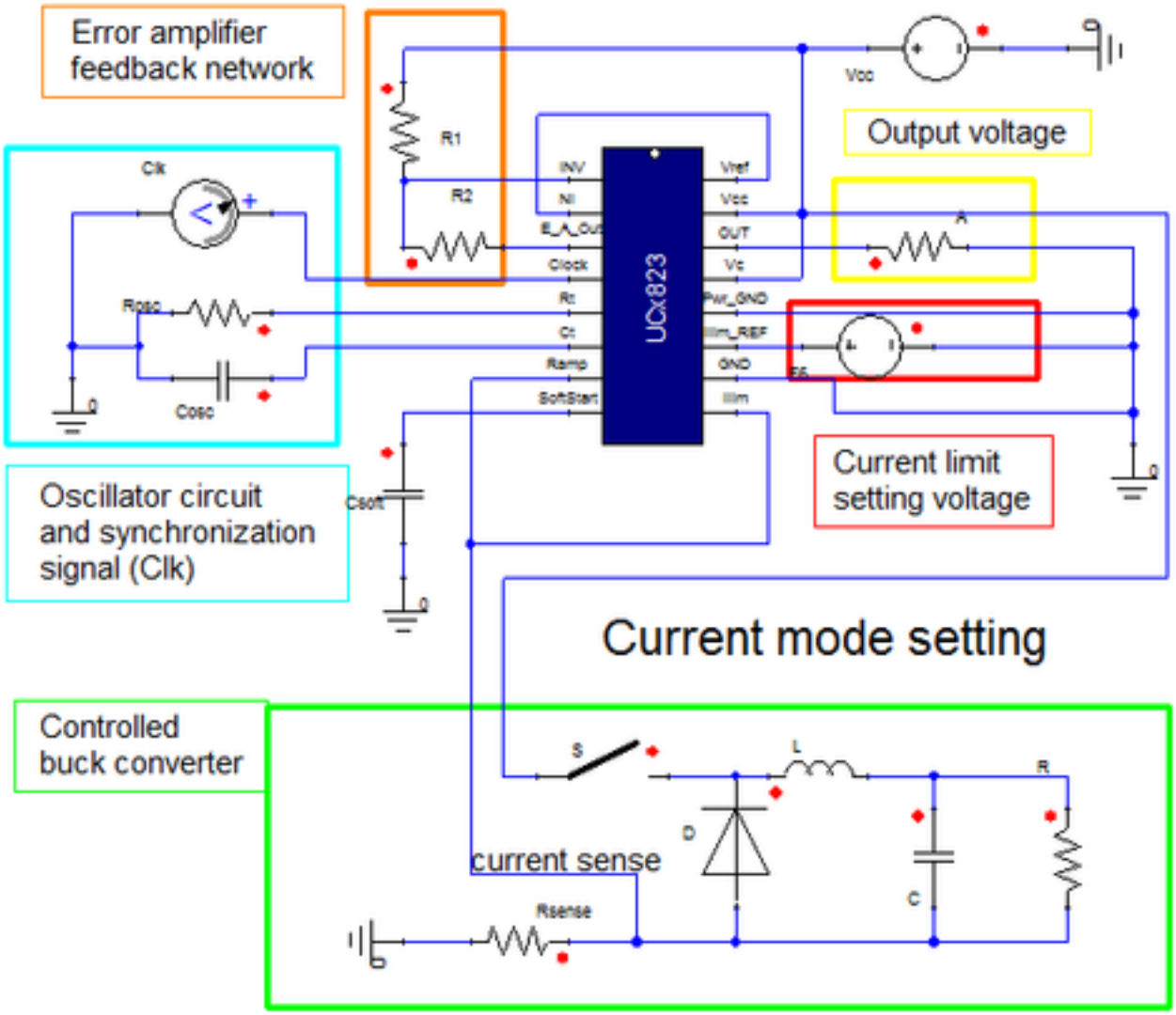

Figure 2. Example Circuit

In this application we are using a UCx823 to control a buck converter in current mode. Apart from the converter itself, the external circuit needed for a proper operation consists of: oscillator circuit (a resistor and a capacitor), error amplifier feedback network, soft-start capacitor and input and current limit reference voltage.

In a real application the output would be connected to a MOSFET gate or a driver input pin. Here we are using a simple resistor whose voltage value opens and closes the converter switch.

Simulation results :

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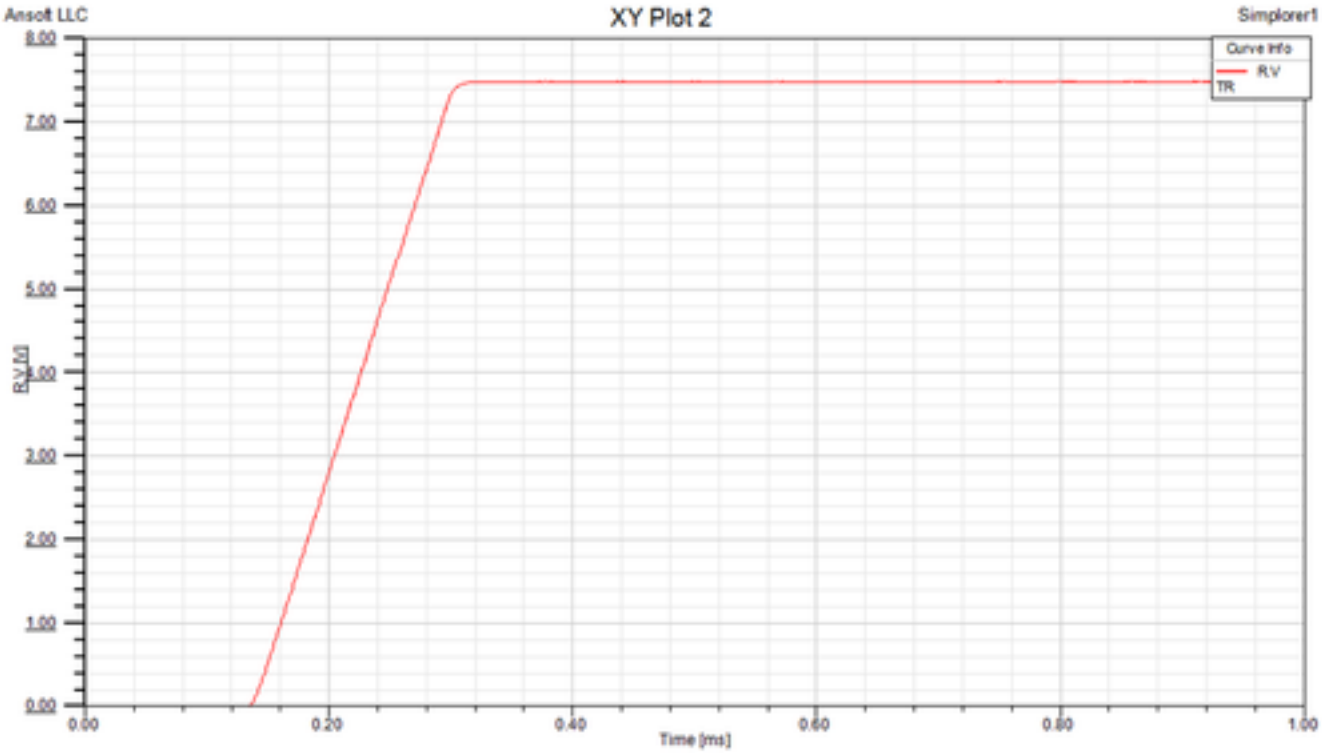

Red: load voltage

Figure 3. Simulation results(a)

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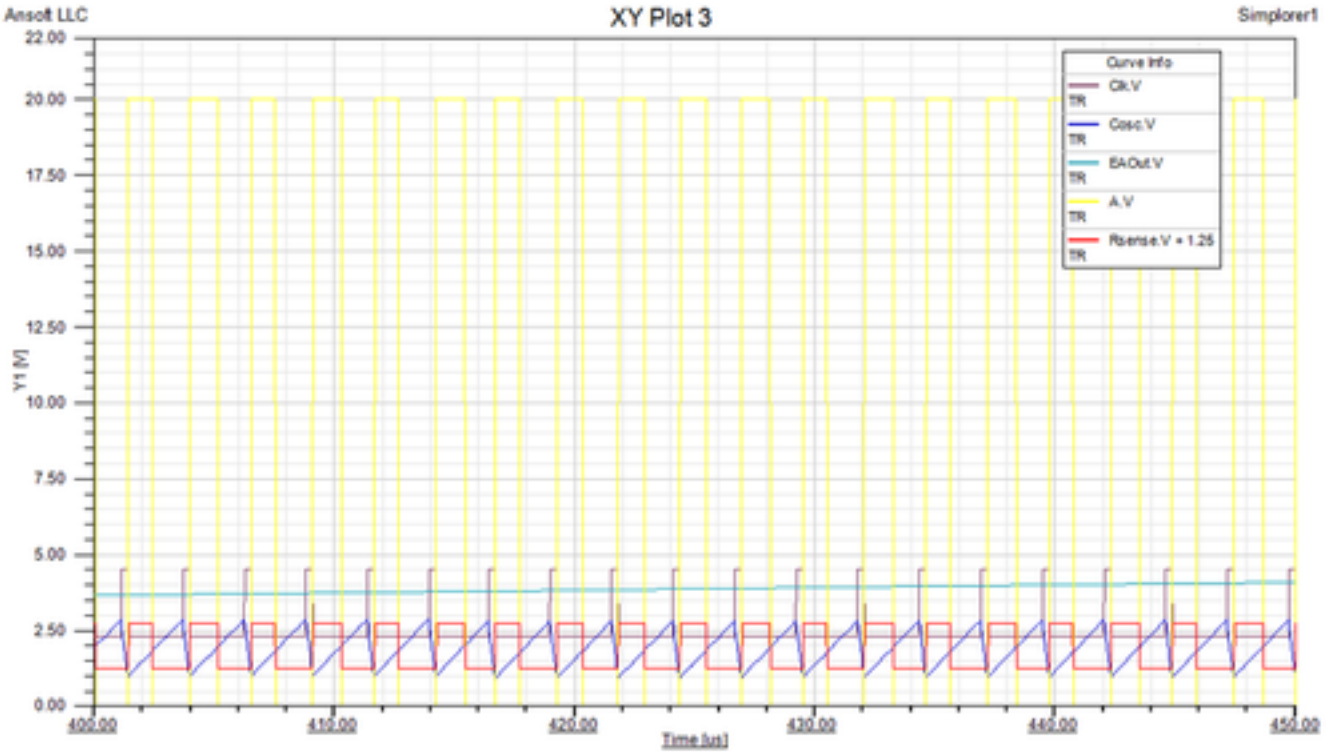

Yellow: output voltage (PWM)

Red: sense resistor voltage + 1.25V offset

Light blue: error amplifier output voltage

Blue: oscillator voltage

Brown: clock

Figure 4. Simulation results(b)

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References

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UCx824: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

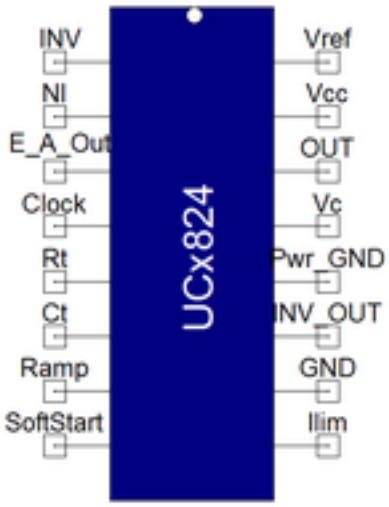

Figure 1. Component symbol

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Description

The *UCx823* family of PWM control ICs is optimized for high frequency switched mode power supply applications. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the

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output is high impedance. The current limit reference is a DC input voltage to the current limit comparator.

These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:
• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current and voltage sense: a voltmeter measures the voltage on Ramp pin. The input impedance is infinite.
• Current limit: a voltmeter measures the voltage on this pin to set the overcurrent protection. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5.1V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Output voltage: controlled by a state machine. Its output impedance is zero.
• Complementary output voltage: controlled by the same state machine, its state is the opposite. Its output impedance is zero too.

The state machines control the under-voltage protection (when the input voltage falls below 9.2V, the protection activates and the output and the reference fall to zero), the oscillator, the output voltage and the overcurrent protection.

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Conservative Pins

Table 1

Symbol	Description
INV	Error amplifier inverting intput
NI	Error amplifier non-inverting input
E_A_Out	Output of the error amplifier

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Clock	Clock output
Rt	Oscillator resistor pin
Ct	Oscillator capacitor pin
Ramp	Ramp comparator input
SoftStart	Soft start timing configuration pin
Vref	Voltage reference
Vcc	Logic supply voltage
OUT	Driver output
Vc	Input voltage
Pwr_GND	Power ground
INV_OUT	Complementary output
GND	Reference ground
Ilim	Current limit comparator input

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Parameters

Comparison between model and real component.

Unless otherwise noted, these specifications apply for RT = 3.65k, CT = 1nF, VCC = 15V, 0°C < TA < +70°C for the UC3824, -25°C < TA < +85°C for the UC2824, and -55°C < TA < +125°C for the UC1824, TA = TJ.

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Table 2

PARAMETER	TEST CONDITIONS	UCx82 4			MODEL	UNITS
		MIN	TYP	MAX		
Reference Section						
Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	5.10	V
Line Regulation	10 < V_{CC} < 30V		2	20	2	mV
Load Regulation	1 < I_O < 10mA		5	20	0	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4	0	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	5.10-5.20	
Output NoiseVoltage*	10Hz < f < 10kHz		50		0	µV
Long TermStability*	T_J = 125°C, 1000 hrs.		5	25	0	mV
Short CircuitCurrent	V_{REF}=0V	-15	-50	-100	∞	mA
Oscillator Section						
Initial Accuracy*	T_J=25°C	360	400	440	386	kHz
Voltage Stability*	10 < V_{CC} < 30V		0.2	2	0	%
Temperature Stability*	T_{MIN} <T_A < T_{MAX}		5		X	%
Total Variation*	Line, Temp.	340		460	386	kHz
Clock Out High		3.9	4.5		4.5	V
Clock OutLow			2.3	2.9	2.3	V
Ramp Peak*		2.6	2.8	3.0	2.8	V
Ramp Valley*		0.7	1.0	1.25	1.0	V
Ramp Valley toPeak*		1.6	1.8	2.0	1.8	V
Error AmplifierSection						
Input Offset Voltage				10	0	mV
Input BiasCurrent			0.6	3	0	µA
Input Offset			0.1	1	0	µA

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Current						
Open LoopGain	1 < V_O < 4V	60	95		95	dB
CMRR	1.5 < V_{CM} < 5.5V	75	95		95	dB
PSRR	10 < V_{CC} < 30V	85	110		110	dB
Output SinkCurrent	$V_{PIN\ 3}$ =1V	1	2.5		0	mA
Output SourceCurrent	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		0	mA
Output High Voltage	$I_{PIN\ 3}$ = 0.5mA	4.0	4.7	5.0	4.8	V
Output LowVoltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	V
Unity GainBandwidth*		3	5.5		X	MHz
Slew Rate*		6	12		X	V/ S
PWM ComparatorSection						
Pin 7 BiasCurrent	$V_{PIN\ 7}$ = 0V		-1	-5	0	µA
Duty CycleRange		0		85	90	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.25	V
Delay to Output*			50	80	0	ns
Soft-Start Section						
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	9	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			∞	mA
Current Limit/ShutdownSection						
Pin 9 BiasCurrent	0 < $V_{PIN\ 9}$ < 4V			10	0	µA
Current Limit Offset	$V_{PIN\ 11}$ = 1.1V			15	0	mV
Current Limit Common Mode Range ($V_{PIN\ 11}$)		1.0		1.25		V

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Shutdown Threshold		1.25	1.40	1.55	1.4	V
Delay to Output*			50	80	0	ns
Output Section						
Output LowLevel	I_{OUT} = 20mA		0.25	0.40	0	V
	I_{OUT} = 200mA		1.2	2.2	0	V
Output High Level	I_{OUT} = 20mA	13.0	13.5		15	V
	I_{OUT} = 200mA	12.0	13.0		15	V
Collector Leakage	V_C = 30V		100	500	0	µA
Rise/Fall Time*	C_L = 1nF		30	60	0	ns
Under-Voltage Lockout Section						
Start Threshold		8.8	9.2	9.6	9.2	V
UVLO Hysteresis		0.4	0.8	1.2	0.8	V
Supply Current						
Start Up Current	V_{CC} = 8V		1.1	2.5	0	mA
I_{CC}	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ =0V, $V_{PIN\ 2}$ = 1V		22	33	0	mA

**This parameter is not 100% tested in production but guaranteed by design*
X: Not implemented

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Input/Output Quantities

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Examples

Example circuit :

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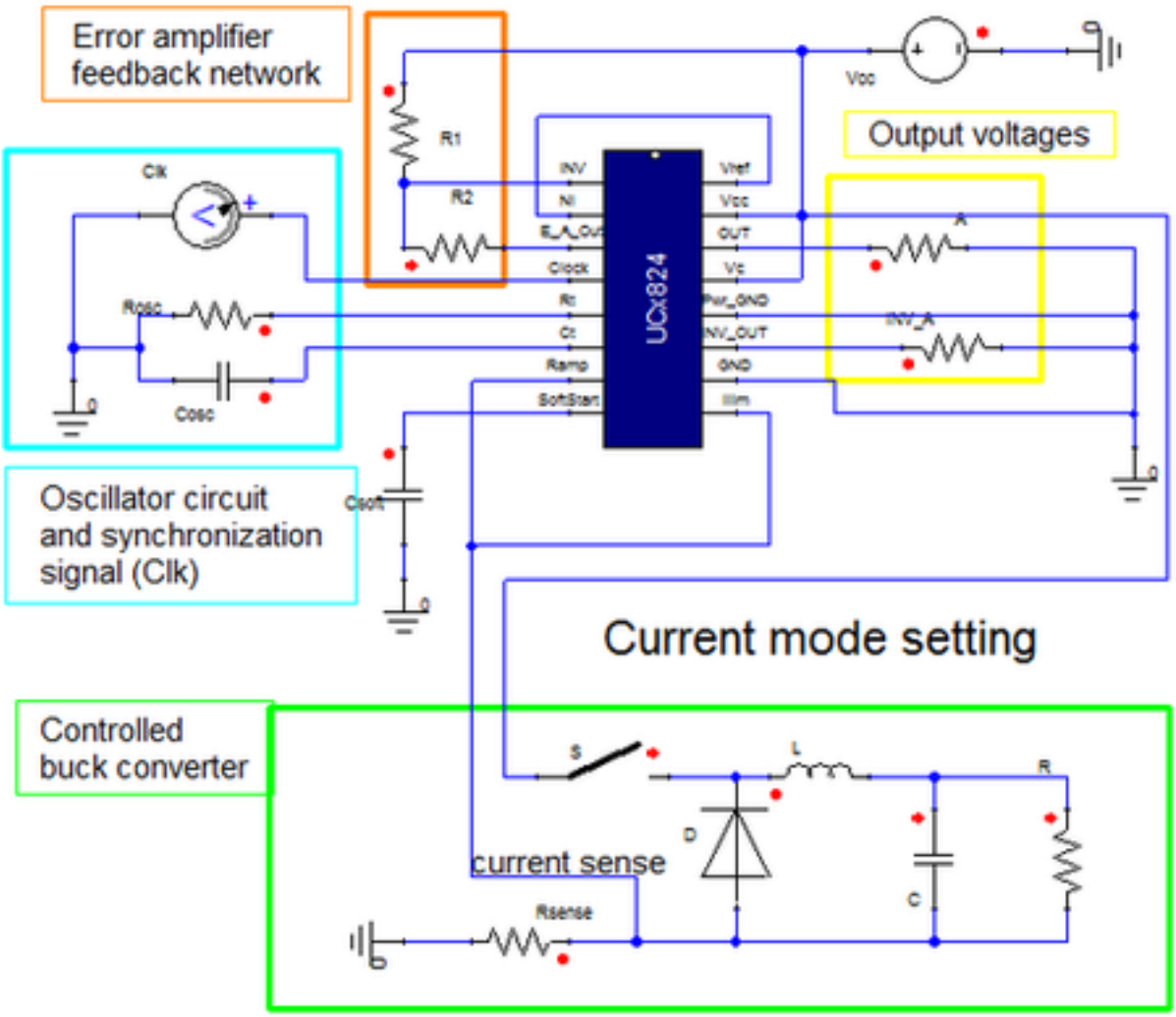

Figure 2. Example Circuit

In this application we are using a UC3824 to control a buck converter in current mode. Apart from the converter itself, the external circuit needed for a proper operation consists of: oscillator circuit (a resistor and a capacitor), error amplifier feedback network, soft-start capacitor and input voltage.

In a real application the output would be connected to a MOSFET gate or a driver input pin. Here we are using a simple resistor whose voltage value opens and closes the converter switch.

Simulation results :

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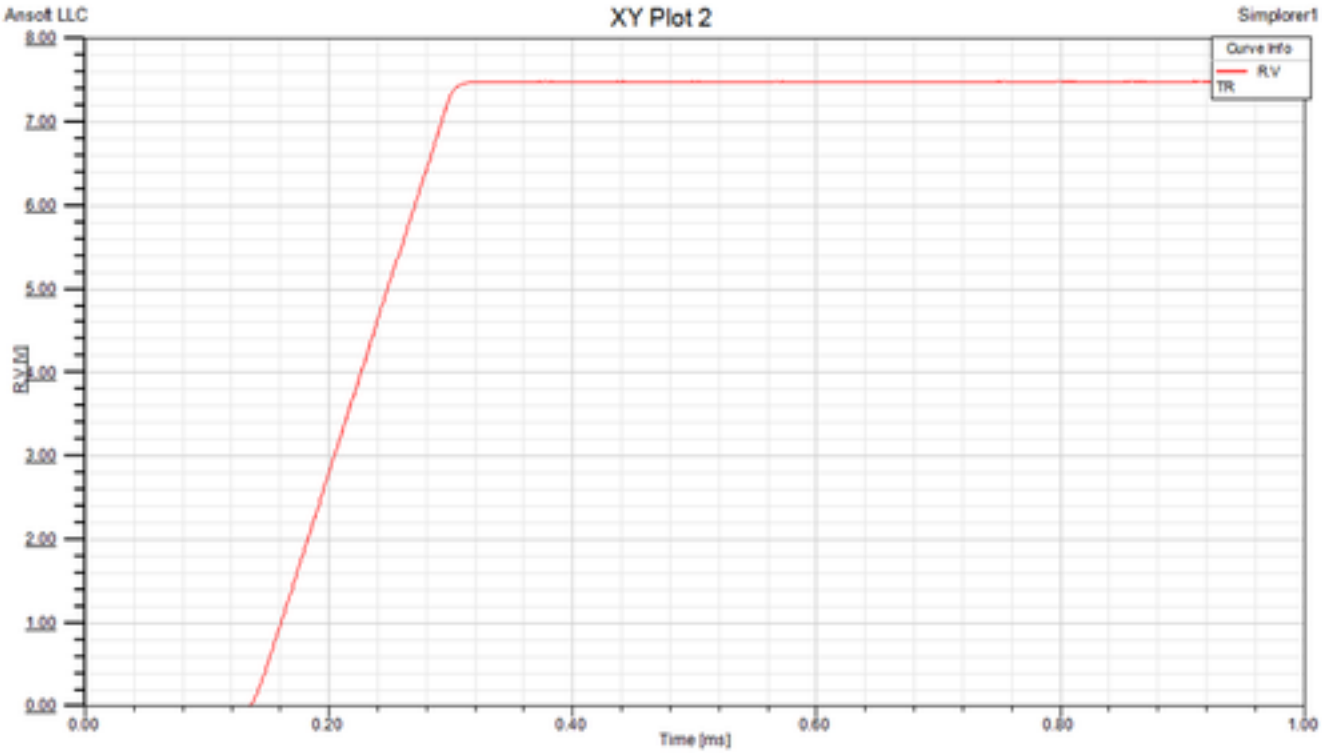

Red: load voltage

Figure 3. Simulation results(a)

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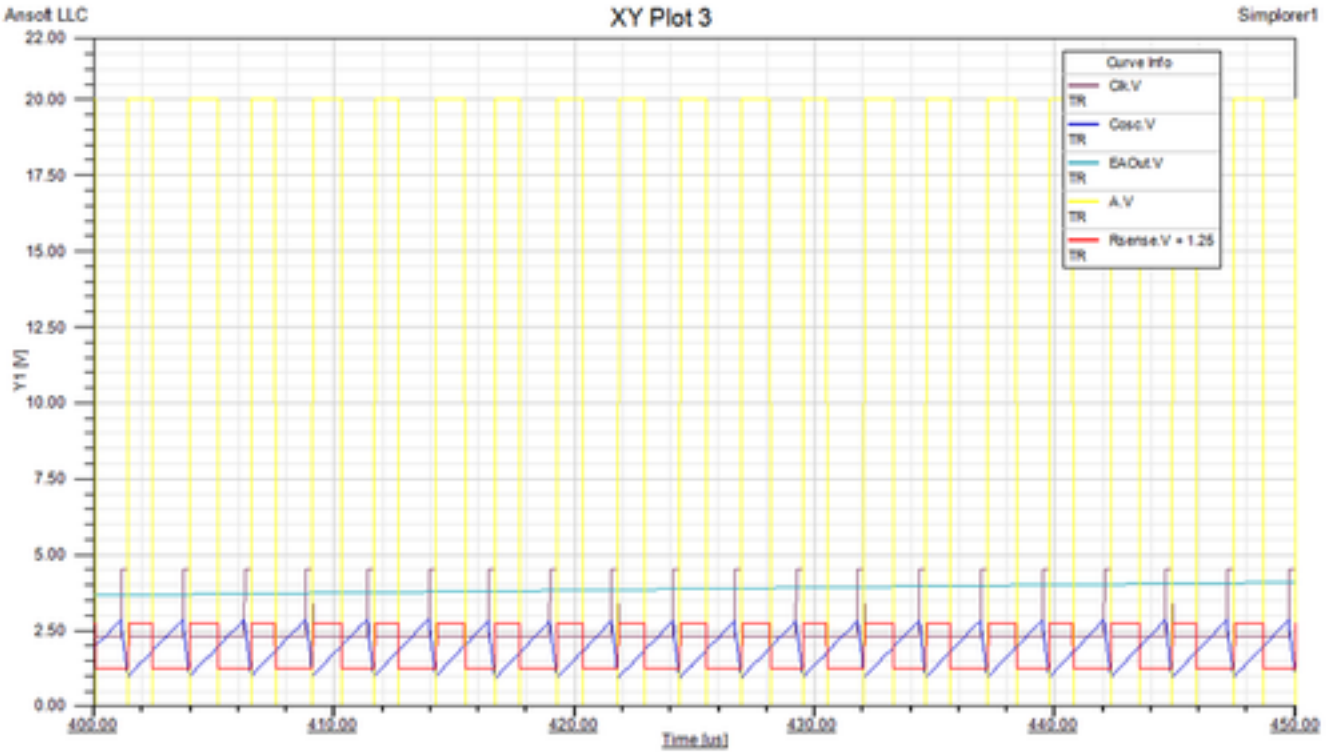

Yellow: output voltage (PWM)

Red: sense resistor voltage + 1.25V offset

Light blue: error amplifier output voltage

Blue: oscillator voltage

Brown: clock

Figure 4. Simulation results(b)

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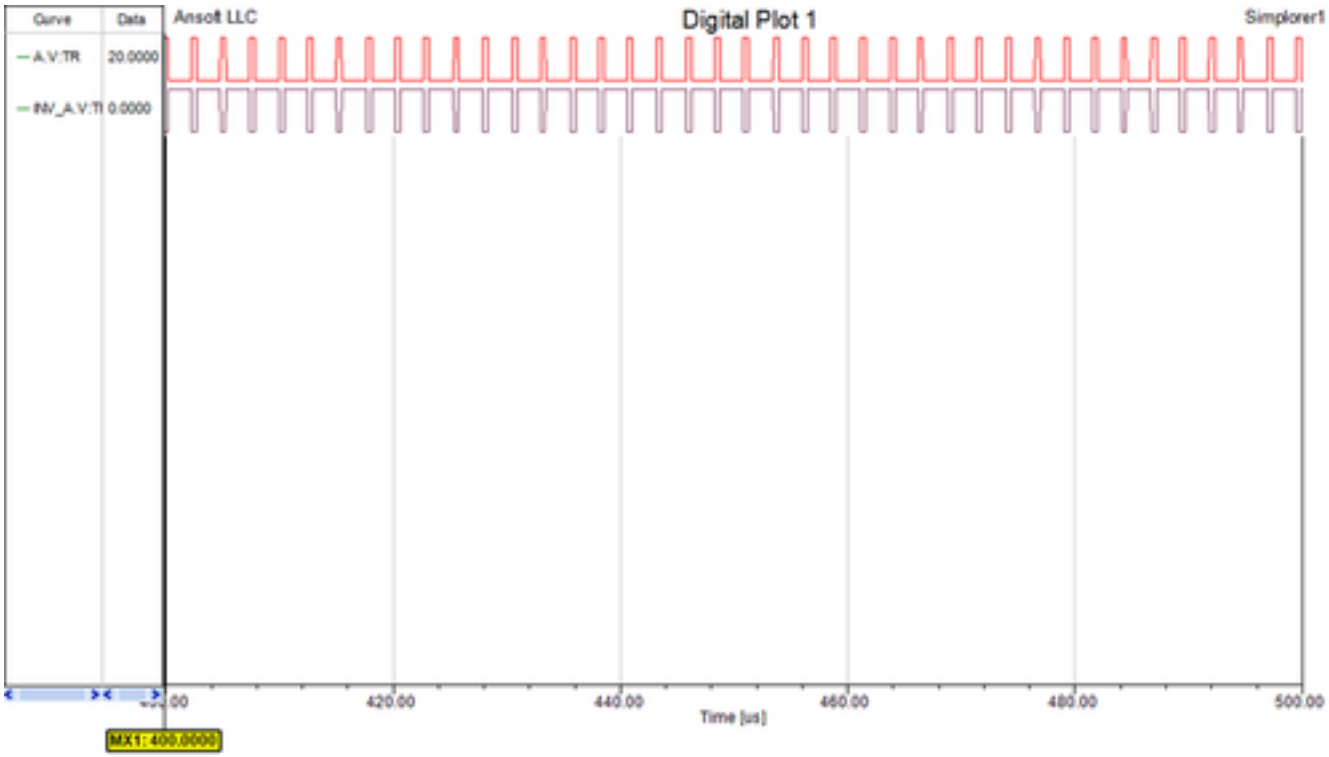

Red: output voltage

Purple: complementary output voltage

Figure 5. Simulation results(c)

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References

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UCx825: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

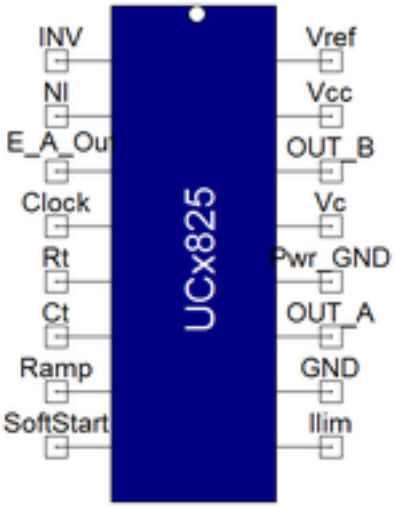

Figure 1. Component symbol

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Description

The *UCx823* family of PWM control ICs is optimized for high frequency switched mode power supply applications. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the

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output is high impedance. The current limit reference is a DC input voltage to the current limit comparator.

These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

This model consists of three main parts: the inputs, the logic and the outputs.
- The inputs basically are the inputs of the error amplifier, the ramp and shutdown pin and the supply voltages.
- The outputs can be divided into two groups: the main outputs (OUT_A and OUT_B), and the auxiliary outputs, which are the visible end of auxiliary circuitry such as the reference voltage, the oscillator and clock and the soft start circuit.
- The logic is the non-electrical part of the model, which controls the other parts. It consists of four state machines. The main machine controls the major operation of the model, opening and closing the output switches as a result of the changes in the input signals. The other state machines control the oscillator and the undervoltage and overcurrent protections.

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Assumptions and Limitations

Temperature related features have not been modeled.

A 1ns simulation minimum step is required to achieve an accurate oscillator waveform.

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Table 1

Symbol	Description
INV	Error amplifier inverting intput
NI	Error amplifier non-inverting input
E_A_Out	Output of the error amplifier
Clock	Clock output
Rt	Oscillator resistor pin
Ct	Oscillator capacitor pin
Ramp	Ramp comparator input

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SoftStart	Soft start timing configuration pin
Vref	Voltage reference
Vcc	Logic supply voltage
OUT_B	Driver output B
Vc	Input voltage
Pwr_GND	Power ground
OUT_A	Driver output A
GND	Reference ground
Ilim	Current limit comparator input

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for , RT = 3.65k, CT = 1nF, VCC= 15V, -55°C < TA < 125°C for the UC1825, -40°C < TA < 85°C, TA=TO.

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Table 2

PARAMETERS	TEST CONDITIONS	UCx825			MODEL	UNITS
		MIN	TOP	MAX		
Reference Section						
Output Voltage	T_O = 25°C, I_O = 1mA	5.05	5.10	5.15	5.1	V
Line Regulation	10V < V_{CC} < 30V		2	20	2	mV
Load Regulation	1mA < I_O < 10mA		5	20	0	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4	0	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	5.05 - 5.20	V
Output NoiseVoltage*	10Hz < f < 10kHz		50		0	µV
Long TermStability*	T_J = 125°C, 1000hrs.		5	25	0	mV
Short CircuitCurrent	V_{REF} = 0V	-15	-50	-100	X	mA
Oscillator Section						
Initial Accuracy*	T_J = 2°C	360	400	440	410	kHz
Voltage Stability*	10V < V_{CC} < 30V		0.2	2	0	%
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		5		0	%
Total Variation*	Line, Temperature	340		460	410	kHz
Oscillator Section (cont.)						
Clock Out High		3.9	4.5		4.5	V
Clock OutLow			2.3	2.9	2.3	V
Ramp Peak*		2.6	2.8	3.0	2.8	V
Ramp Valley*		0.7	1.0	1.25	1.1	V
Ramp Valley toPeak*		1.6	1.8	2.0	1.7	V
Error AmplifierSection						
Input Offset Voltage				10	0	mV

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Input BiasCurrent			0.6	3	0	µA
Input Offset Current			0.1	1	0	µA
Open LoopGain	1V < V_O < 4V	60	95		100	dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		95	dB
PSRR	10V < V_{CC} < 30V	85	110		110	dB
Output SinkCurrent	$V_{PIN\ 3}$ = 1V	1	2.5		0	mA
Output SourceCurrent	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		0	mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	5	V
Output LowVoltage	$I_{PIN\ 3}$ = 1mA	0	0 .5	1.0	0	V
Unity GainBandwidth*		3	5.5		X	MHz
Slew Rate*		6	12		X	V/µs
PWM ComparatorSection						
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5	0	µA
Duty Cycle Range		0		80	0 - 85	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.25	V
Delay to Output*			50	80	0	ns
Soft-Start Section						
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	9	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			∞	mA

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rent						
Current Limit / ShutdownSection						
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			15	0	µA
Current Limit Threshold		0.9	1.0	1.1	1.0	V
Shutdown Threshold		1.25	1.40	1.55	1.4	V
Delay to Output			50	80	0	ns
Output Section						
Output Low Level	I_{OUT} = 20mA		0.25	0.40	0	V
	I_{OUT} = 200mA		1.2	2.2	0	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		15	V
	I_{OUT} = -200mA	12.0	13.0		15	V
Collector Leakage	V_C = 30V		100	500	0	µA
Rise/ Fall Time*	CL = 1nF		30	60	0	ns
Under-Voltage Lockout Section						
Start Threshold		8.8	9.2	9.6	9.2	V
UVLO Hysteresis		0.4	0.8	1.2	0.8	V
Supply CurrentSection						
Start Up Current	V_{CC} = 8V		1.1	2.5	X	mA

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rent						
ICC	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V; $V_{PIN\ 2}$ = 1V		22	33	X	m-A

**This parameter is not 100% tested in production but guaranteed by design*
X: Not implemented

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Example circuit :

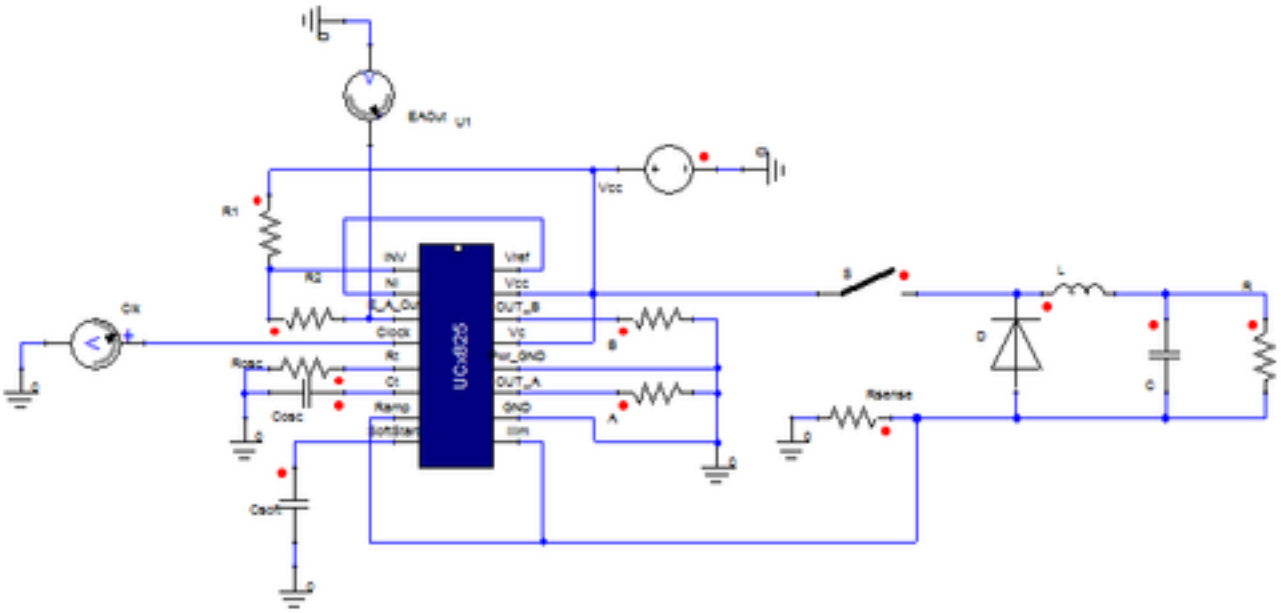

Figure 2. Example Circuit

Simulation results :

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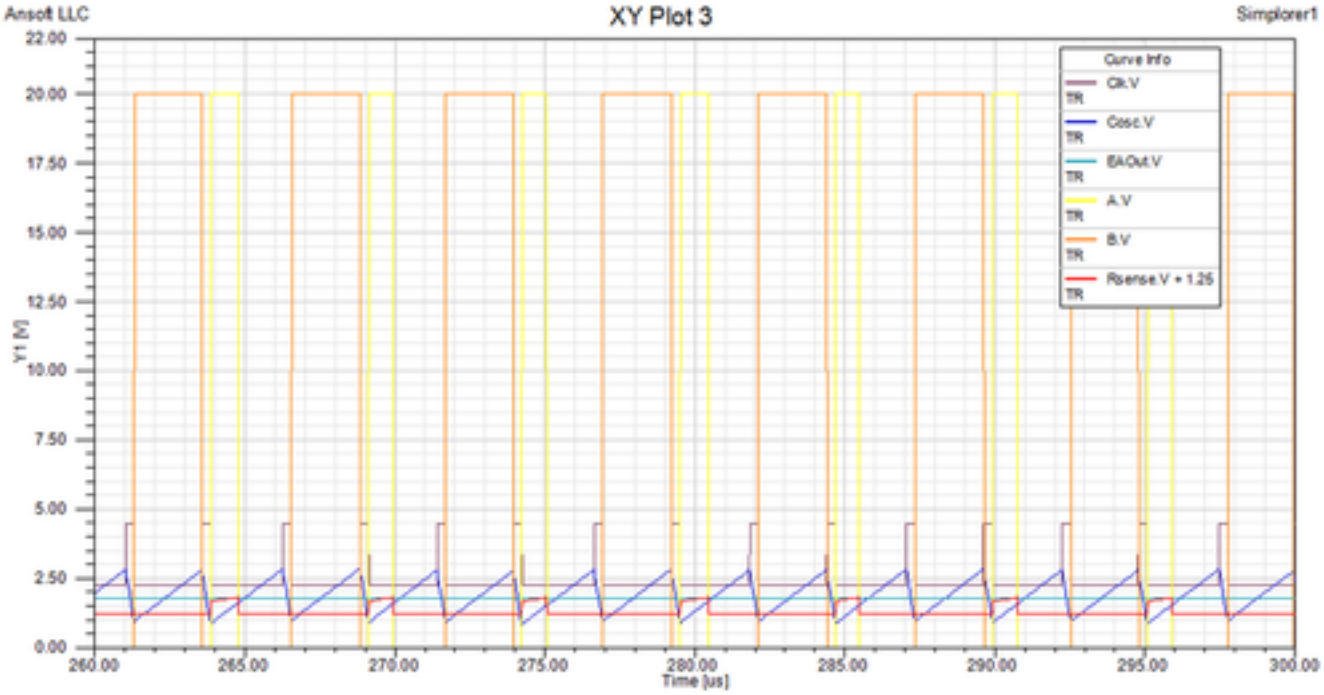

Figure 3. Simulation results(a)

Figure above shows the normal operation of the device. Yellow and orange signals represent the A and B outputs, respectively. Outputs rise in opposite clock cycles, achieving this way, a maximum 50% duty cycle. Blue signal is the oscillator and the purple one is the clock.

Duty cycle is controlled by comparing the ramp voltage and the error amplifier output (red and light blue signals respectively).

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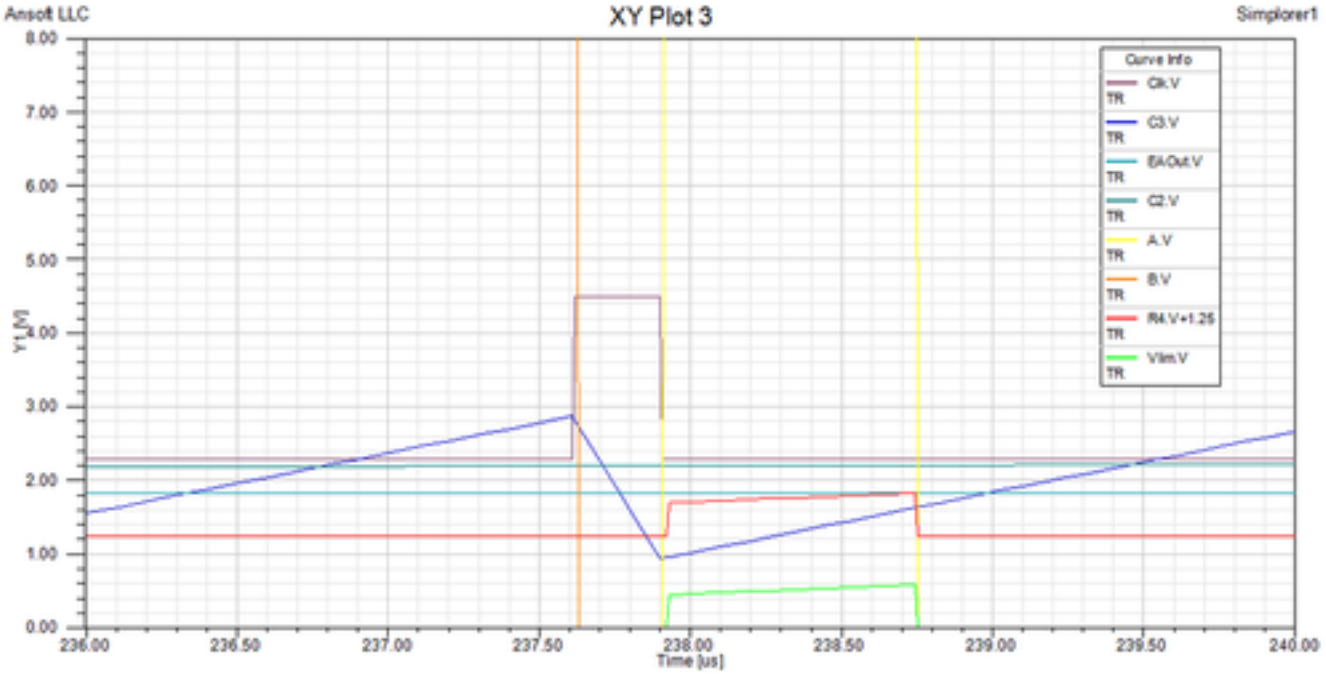

Figure 4. Simulation results(b)

Detail of the signal triggering during the normal operation of the controller. When the voltage in the Ramp pin plus the internal offset of 1.25V (red signal) reaches the value of the error amplifier output (light blue), output (A in this case, yellow) falls to zero. Normal operation is possible since the over-current protection is not activated because the Ilim pin does not reach the 1V value.

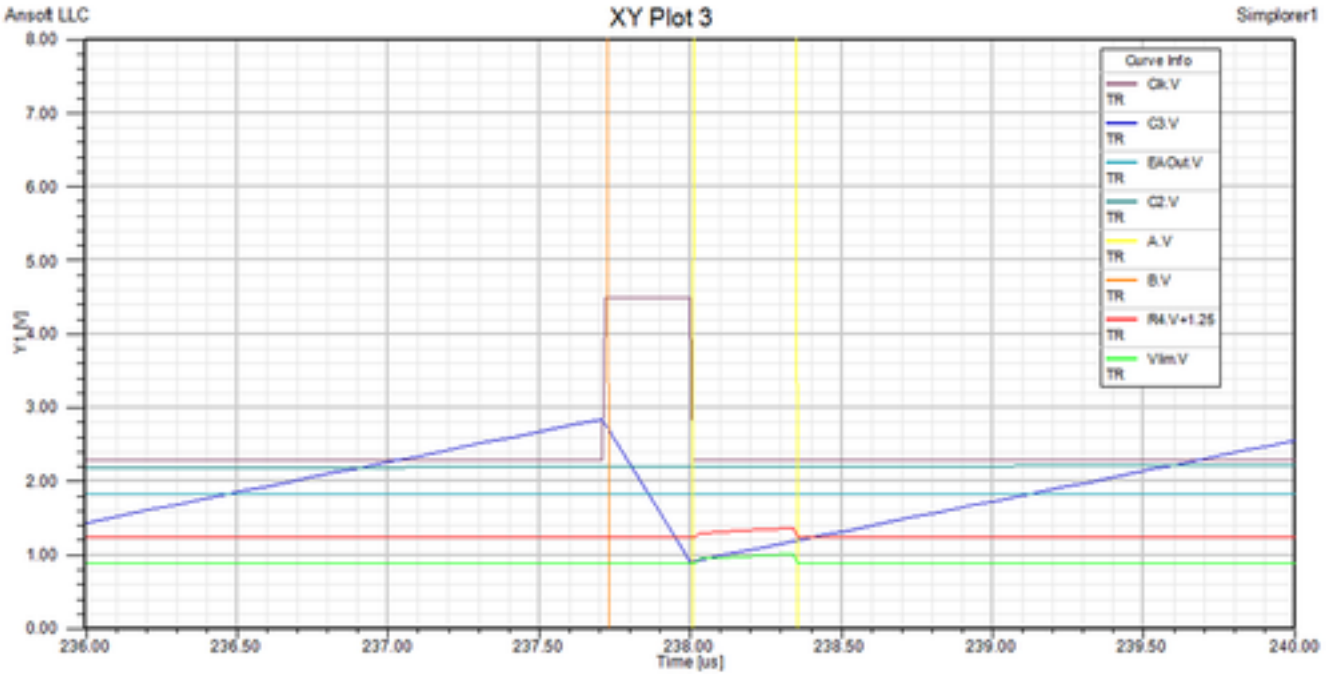

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Figure 5. Simulation results(c)

In this case, normal operation is interrupted by an over-current. When voltage in this pin (green signal) reaches 1V, output voltage (A, yellow) is set to zero, not waiting to the ramp signal to reach the value of the error amplifier output, as shown in the previous case.

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References

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UCx842: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

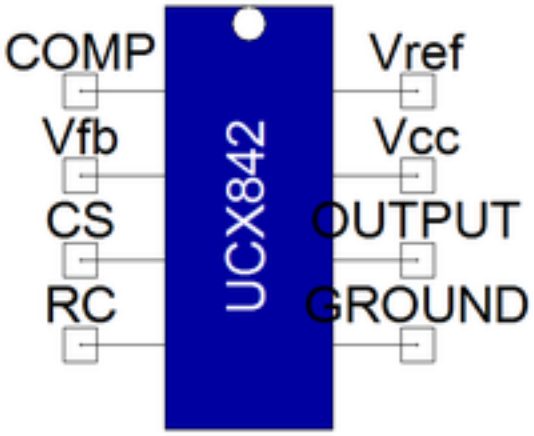

Figure 1. Component symbol

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Description

The *UCX842/3/4/5* family of control devices provides the necessary features to implement off-line or dc-to-dc fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

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Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The *UCX842* and *UCX844* have UVLO thresholds of 16 VON and 10 VOFF, ideally suited to off-line applications. The corresponding thresholds for the *UCX843* and *UCX845* are 8.4 V and 7.6 V. The *UCX842* and *UCX843* can operate to duty cycles approaching 100%. The *UCX844* and *UCX845* have a range of zero to 50%.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:

• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: voltage limited by a zener diode to 34V. Input current is modeled with a current source whose value is the sum of the output current and the voltage reference current.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 10V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Table 1

Symbol	Description
COMP	Error amplifier output
Vfb	Error amplifier inverting input
CS	Current sense comparator

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RC	Oscillator timing pin
V_{ref}	Voltage reference
V_{CC}	Power input
OUTPUT	Driver output
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, the real component specifications apply for -55°C ≤TA ≤125°C for the UC184X; -40°C ≤TA≤85°C for the UC284X; 0°C ≤TA≤70°C for the 384X; VCC = 15 V(1); RT = 10 kΩ; CT = 3.3 nF, TA = TJ.

Table 2

Parameter	Real Component Test Conditions	UCx842/3/4/5			Model	Unit
		Min	Typ	Max		
Reference Section						
Output Voltage	T_J = 25°C, IO = 1 mA	4.90	5.00	5.10	5.00	V
Line Regulation	12V ≤ V_{IN} ≤ 25 V		6	20	0	mV
Load Regulation	1 mA ≤ I_0 ≤ 20 mA		6	25	0	
Temp. Stability	See (2) (3)		0.2	0.4	0	mV/°C
Total Output Variation	Line, load, temperature (2)	4.82		5.18	0	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C (2)		50		0	µV
Long Term Stability	T_A = 125°C, 1000 Hrs (2)		5	25	0	mV
Output Short Circuit		-30	-100	-180	X	mA
Oscillator Section						
Initial Accuracy	T_J = 25°C (4)	47	52	57	52	kHz
Voltage Stability	12V ≤ V_{CC} ≤ 25 V		0.2%	1%	0%	
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (2)		5%		0%	
Amplitude	$V_{PIN\ 4}$ peak-to-peak (2)		1.7		1.7	V
Error Amp Section						
Input Voltage	$V_{PIN\ 1}$ = 2.5 V	2.42	2.50	2.58	2.50	V
Input Bias Current			-0.3	-2	0	A
A_{VOL}	2V≤V_O≤ 4 V	65	90		90	dB
Unity Gain Bandwidth	T_J = 25°C (5)	0.7	1		X	MHz

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PSRR	12V ≤ V_{CC} ≤ 25 V	60	70		70	dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7 V, $V_{PIN\ 1}$ = 1.1 V	2	6		0	mA
Output Source Current	$V_{PIN\ 2}$ = 2.3 V, $V_{PIN\ 1}$ = 5 V	-0.5	-0.8		0	
V_{OUT} High	$V_{PIN\ 2}$ = 2.3 V, R_L = 15 k to ground	5	6		6	V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7 V, R_L = 15 k to Pin 8		0.7	1.1	0.7	
Current Sense Section						
Gain	See (6) (7)	2.85	3	3.15	3	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5 V (6)	0.9	1	1.1	1	V
PSRR	12V ≤ V_{CC} ≤ 25 V (5) (6)		70		70	dB
Input Bias Current			-2	-10	0	A
Delay to Output	$V_{PIN\ 3}$ = 0 V to 2 V (5)		150	300	0	ns
Output Section						
Output Low Level	I_{SINK} = 20 mA		0.1	0.4	0.1	V
	I_{SINK} = 200 mA		1.5	2.2	0.1	
Output High Level	I_{SOURCE} = 20 mA	13	13.5		Vcc-1.5	
	I_{SOURCE} = 200 mA	12	13.5		Vcc-1.5	
Rise Time	T_J = 25°C, C_L = 1 nF (5)		50	150	X	ns
Fall Time	T_J = 25°C, C_L = 1 nF (5)		50	150	X	
Under-Voltage Lockout Section						
Start Threshold	X842	14.5	16	17.5	16	V
Min. Operating Voltage After Turn On	X842	8.5	10	11.5	10	
PWM Section						
Maximum Duty Cycle	X842	95%	97%	100%	100%	
Minimum Duty Cycle				0%	0%	
Total Standby Current						
Start-Up Current			0.5	1	0	mA
Operating Supply Current	$V_{PIN\ 2}$ = $V_{PIN\ 3}$ = 0 V		11	17	0	
V_{CC} Zener Voltager	I_{CC} = 25 mA	30	34		30 34	V

X: not implemented

(1) Adjust VCC above the start threshold before setting at 15 V.
(2) These parameters, although specified, are not 100% tested in production.
(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

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$Temp_{Stability} = (Max(V_{REF}) - Min(V_{REF})) / (Max(T_j) - Min(T_j))$

VREF(max) and VREF(min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency for the UC1842 and UC1843. Output frequency is one half oscillator frequency for the UC1844 and UC1845.
(5) These parameters, although specified, are not 100% tested in production.
(6) Parameter measured at trip point of latch with $V_{PIN2} = 0$.
(7) Gain defined as:

$A=\Delta V_{PIN1}/\Delta V_{PIN3}$; $0 \leq V_{PIN3} \leq 0.8$ V

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Example circuit :

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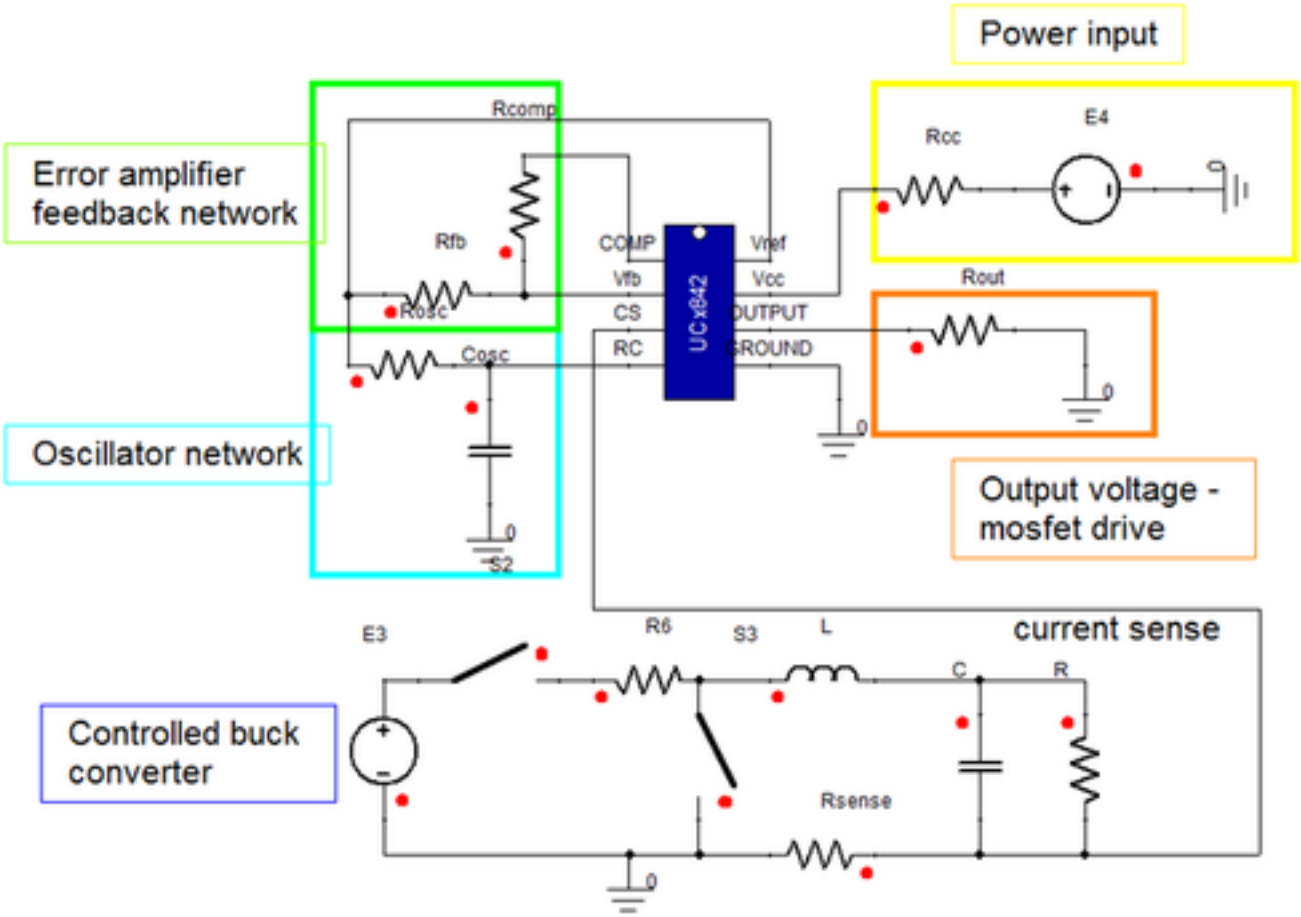

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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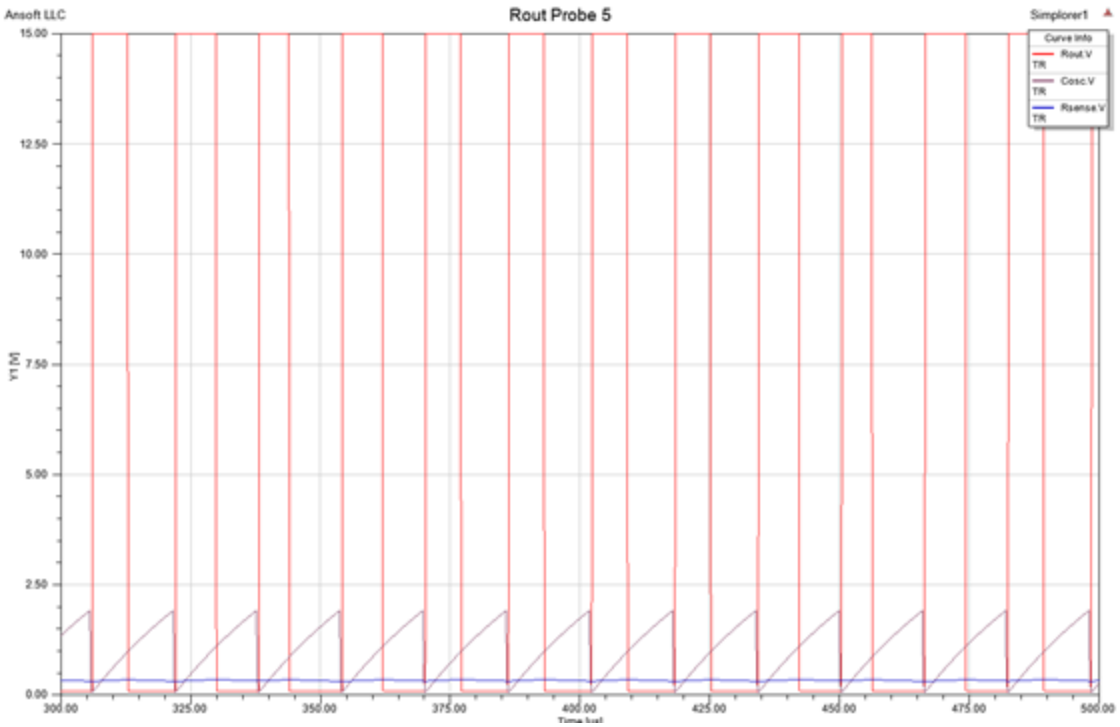

Red: output voltage

Purple: oscillator voltage

Figure 3. Simulation results

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References

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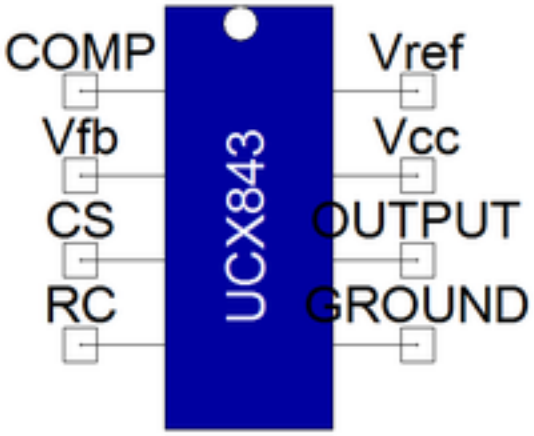
UCx843: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCX842/3/4/5* family of control devices provides the necessary features to implement off-line or dc-to-dc fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

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Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The *UCX842* and *UCX844* have UVLO thresholds of 16 VON and 10 VOFF, ideally suited to off-line applications. The corresponding thresholds for the *UCX843* and *UCX845* are 8.4 V and 7.6 V. The *UCX842* and *UCX843* can operate to duty cycles approaching 100%. The *UCX844* and *UCX845* have a range of zero to 50%.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:

• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: voltage limited by a zener diode to 34V. Input current is modeled with a current source whose value is the sum of the output current and the voltage reference current.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 7.6V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Table 1

Symbol	Description
COMP	Output of the error amplifier
Vfb	Inverting input of the error amplifier
CS	Input to the current sense comparator

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RC	Oscillator timing pin
V_{ref}	Voltage reference
V_{cc}	Power input
OUTPUT	Output of the driver
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, the real component specifications apply for -55°C ≤TA ≤125°C for the UC184X; -40°C ≤TA≤85°C for the UC284X; 0°C≤TA≤70°C for the 384X; VCC = 15 V(1); RT = 10 kΩ; CT = 3.3 nF, TA = TJ.

Table 2

Parameter	Real Component Test Conditions	UCx842/3/4/5			Model	Unit
		Min	Typ	Max		
Reference Section						
Output Voltage	T_J = 25°C, IO = 1 mA	4.90	5.00	5.10	5.00	V
Line Regulation	12V ≤ V_{IN} ≤ 25 V		6	20	0	mV
Load Regulation	1 mA ≤ I_0 ≤ 20 mA		6	25	0	
Temp. Stability	See (2) (3)		0.2	0.4	0	mV/°C
Total Output Variation	Line, load, temperature (2)	4.82		5.18	0	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C (2)		50		0	µV
Long Term Stability	T_A = 125°C, 1000 Hrs (2)		5	25	0	mV
Output Short Circuit		-30	-100	-180	X	mA
Oscillator Section						
Initial Accuracy	T_J = 25°C (4)	47	52	57	52	kHz
Voltage Stability	12V ≤ V_{CC} ≤ 25 V		0.2%	1%	0%	
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (2)		5%		0%	
Amplitude	$V_{PIN\ 4}$ peak-to-peak (2)		1.7		1.7	V
Error Amp Section						
Input Voltage	$V_{PIN\ 1}$ = 2.5 V	2.42	2.50	2.58	2.50	V
Input Bias Current			-0.3	-2	0	A
A_{VOL}	2V≤V_O≤ 4 V	65	90		90	dB

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Unity Gain Bandwidth	T_J = 25°C (5)	0.7	1		X	MHz
PSRR	12V ≤ V_{CC} ≤ 25 V	60	70		70	dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7 V, $V_{PIN\ 1}$ = 1.1 V	2	6		0	mA
Output Source Current	$V_{PIN\ 2}$ = 2.3 V, $V_{PIN\ 1}$ = 5 V	-0.5	-0.8		0	
V_{OUT} High	$V_{PIN\ 2}$ = 2.3 V, R_L = 15 k to ground	5	6		6	V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7 V, R_L = 15 k to Pin 8		0.7	1.1	0.7	
Current Sense Section						
Gain	See (6) (7)	2.85	3	3.15	3	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5 V (6)	0.9	1	1.1	1	V
PSRR	12V ≤ V_{CC} ≤ 25 V (5) (6)		70		70	dB
Input Bias Current			-2	-10	0	A
Delay to Output	$V_{PIN\ 3}$ = 0 V to 2 V (5)		150	300	0	ns
Output Section						
Output Low Level	I_{SINK} = 20 mA		0.1	0.4	0.1	V
	I_{SINK} = 200 mA		1.5	2.2	0.1	
Output High Level	I_{SOURCE} = 20 mA	13	13.5		Vcc-1.5	
	I_{SOURCE} = 200 mA	12	13.5		Vcc-1.5	
Rise Time	T_J = 25°C, C_L = 1 nF (5)		50	150	X	ns
Fall Time	T_J = 25°C, C_L = 1 nF (5)		50	150	X	
Under-Voltage Lockout Section						
Start Threshold	X842	14.5	16	17.5	16	V
Min. Operating Voltage After Turn On	X842	8.5	10	11.5	10	
PWM Section						
Maximum Duty Cycle	X842	95%	97%	100%	100%	
Minimum Duty Cycle				0%	0%	
Total Standby Current						
Start-Up Current			0.5	1	0	mA
Operating Supply Current	$V_{PIN\ 2}$ = $V_{PIN\ 3}$ = 0 V		11	17	0	
V_{CC} Zener Voltager	I_{CC} = 25 mA	30	34		30 34	V

X: not implemented

(1) Adjust VCC above the start threshold before setting at 15 V.
(2) These parameters, although specified, are not 100% tested in production.

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(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$Temp_{Stability} = (Max(V_{REF}) - Min(V_{REF})) / (Max(T_j) - Min(T_j))$

VREF(max) and VREF(min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency for the UC1842 and UC1843. Output frequency is one half oscillator frequency for the UC1844 and UC1845.
(5) These parameters, although specified, are not 100% tested in production.
(6) Parameter measured at trip point of latch with $V_{PIN2} = 0$.
(7) Gain defined as:

$A=\Delta V_{PIN1}/\Delta V_{PIN3}$; $0 \leq V_{PIN3} \leq 0.8$ V

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Example circuit :

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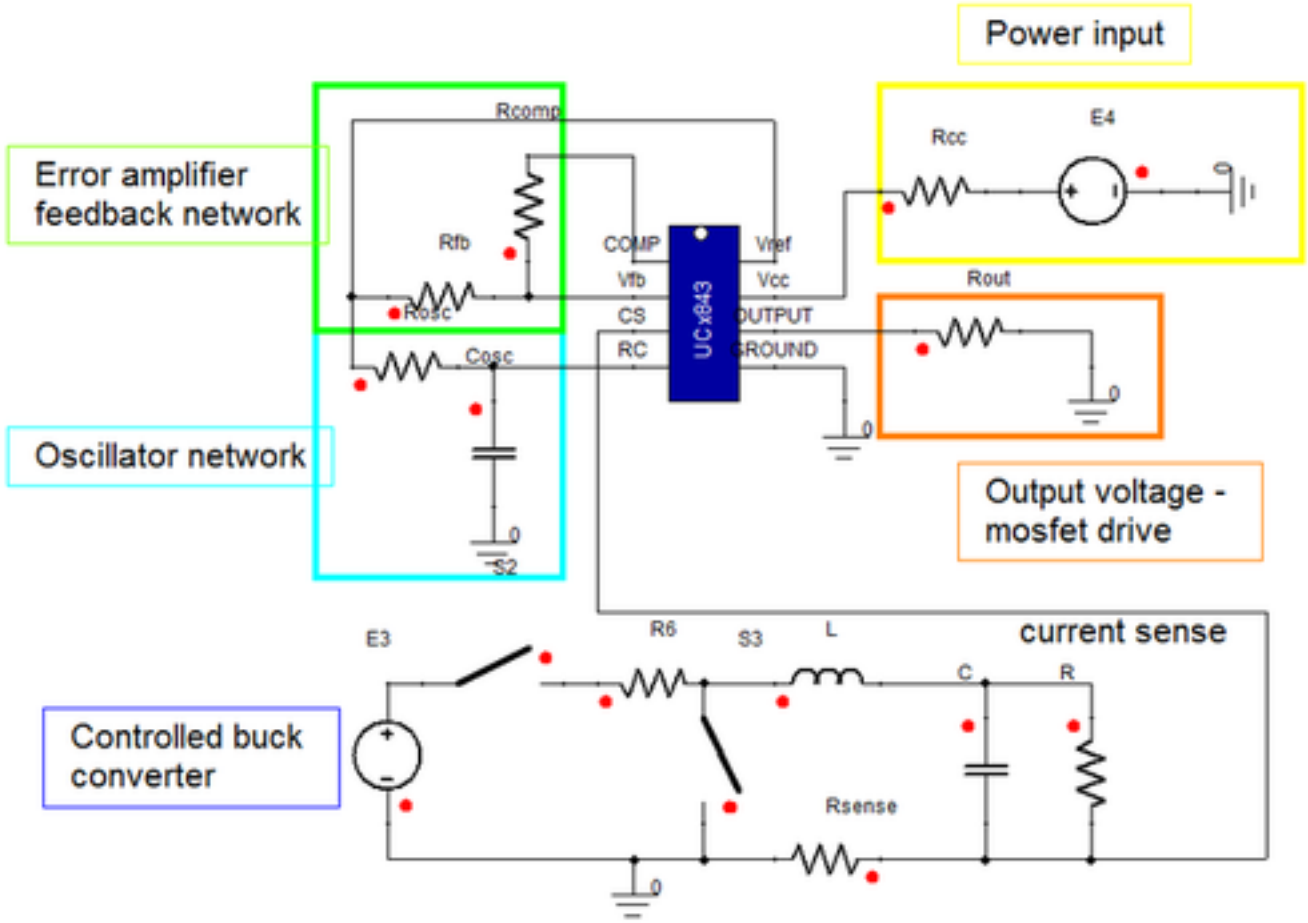

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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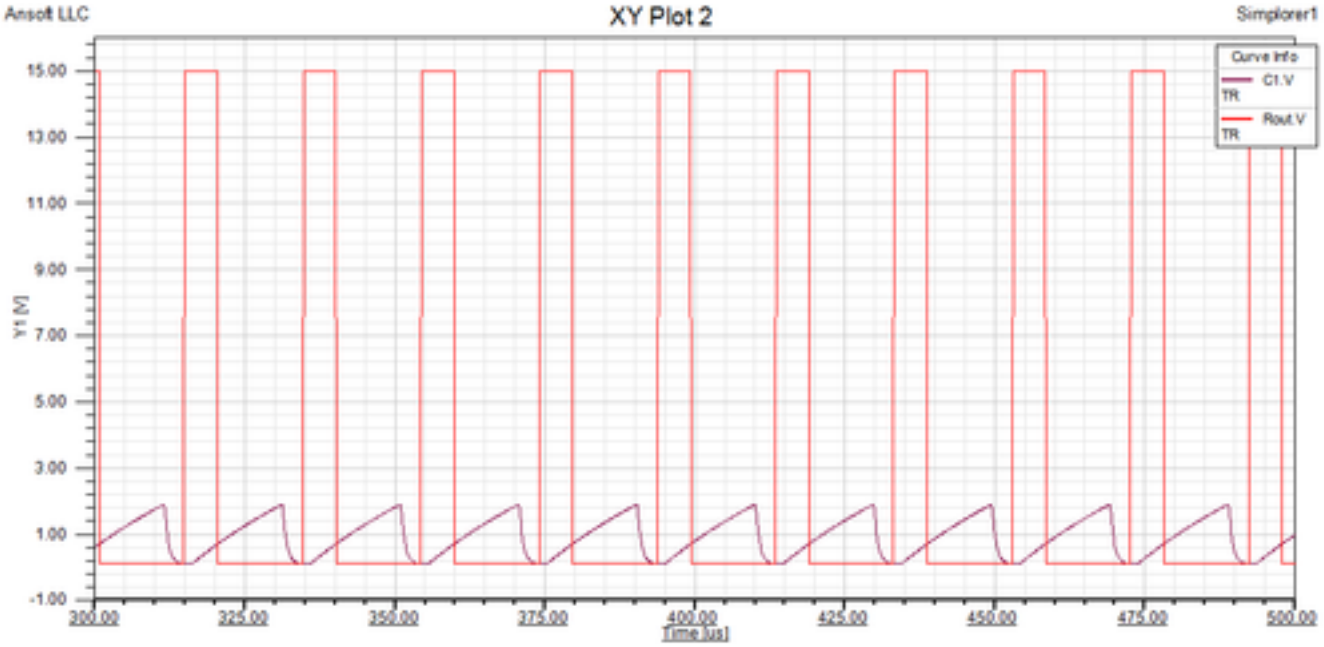

Red: output voltage

Purple: oscillator voltage

Figure 3. Simulation results

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UCx844: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

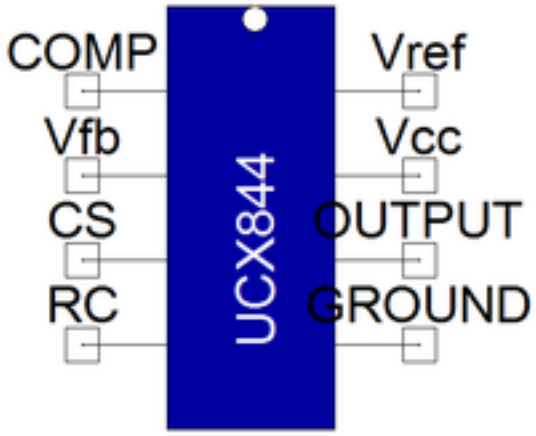

Figure 1. Component symbol

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Description

The *UCX842/3/4/5* family of control devices provides the necessary features to implement off-line or dc-to-dc fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

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Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The *UCX842* and *UCX844* have UVLO thresholds of 16 VON and 10 VOFF, ideally suited to off-line applications. The corresponding thresholds for the *UCX843* and *UCX845* are 8.4 V and 7.6 V. The *UCX842* and *UCX843* can operate to duty cycles approaching 100%. The *UCX844* and *UCX845* have a range of zero to 50%.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:

• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: voltage limited by a zener diode to 34V. Input current is modeled with a current source whose value is the sum of the output current and the voltage reference current.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 10V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Assumptions and Limitations

There is not enough information in the manufacturer datasheet to identify the behavior, so there are some limitations on this model. The oscillation condition that is managed with the state diagram ranges between 0.1V and 1.7V. The capacitor discharge (CT) is discharged through the 200 ohm resistance. The minimum value for the resistance to oscillate is 9.8 kohm. You can make the circuit work by adjusting the frequency with RT/CT (RT >10k).

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Conservative Pins

Table 1

Symbol	Description
COMP	Output of the error amplifier
Vfb	Inverting input of the error amplifier
CS	Input to the current sense comparator
RC	Oscillator timing pin
V_{ref}	Voltage reference
V_{cc}	Power input
OUTPUT	Output of the driver
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, the real component specifications apply for -55°C ≤TA ≤125°C for the UC184X; -40°C ≤TA≤85°C for the UC284X; 0°C≤TA≤70°C for the 384X; VCC = 15 V(1); RT = 10 kΩ; CT = 3.3 nF, TA = TJ.

Table 2

Parameter	Real Component Test Conditions	UCx842/3/4/5			Model	Unit
		Min	Typ	Max		
Reference Section						
Output Voltage	T_J = 25°C, IO = 1 mA	4.90	5.00	5.10	5.00	V
Line Regulation	12V ≤ V_{IN} ≤ 25 V		6	20	0	mV
Load Regulation	1 mA ≤ I_0 ≤ 20 mA		6	25	0	
Temp. Stability	See (2) (3)		0.2	0.4	0	mV/°C
Total Output Variation	Line, load, temperature (2)	4.82		5.18	0	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C (2)		50		0	µV
Long Term Stability	T_A = 125°C, 1000 Hrs (2)		5	25	0	mV
Output Short Circuit		-30	-100	-180	X	mA
Oscillator Section						
Initial Accuracy	T_J = 25°C (4)	47	52	57	52	kHz

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Voltage Stability	12V ≤ V_{CC} ≤ 25 V		0.2%	1%	0%	
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (2)		5%		0%	
Amplitude	$V_{PIN\ 4}$ peak-to-peak (2)		1.7		1.7	V
Error Amp Section						
Input Voltage	$V_{PIN\ 1}$ = 2.5 V	2.42	2.50	2.58	2.50	V
Input Bias Current			-0.3	-2	0	A
A_{VOL}	2V≤V_O≤ 4 V	65	90		90	dB
Unity Gain Bandwidth	T_J = 25°C (5)	0.7	1		X	MHz
PSRR	12V ≤ V_{CC} ≤ 25 V	60	70		70	dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7 V, $V_{PIN\ 1}$ = 1.1 V	2	6		0	mA
Output Source Current	$V_{PIN\ 2}$ = 2.3 V, $V_{PIN\ 1}$ = 5 V	-0.5	-0.8		0	
V_{OUT} High	$V_{PIN\ 2}$ = 2.3 V, R_L = 15 k to ground	5	6		6	V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7 V, R_L = 15 k to Pin 8		0.7	1.1	0.7	
Current Sense Section						
Gain	See (6) (7)	2.85	3	3.15	3	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5 V (6)	0.9	1	1.1	1	V
PSRR	12V ≤ V_{CC} ≤ 25 V (5) (6)		70		70	dB
Input Bias Current			-2	-10	0	A
Delay to Output	$V_{PIN\ 3}$ = 0 V to 2 V (5)		150	300	0	ns
Output Section						
Output Low Level	I_{SINK} = 20 mA		0.1	0.4	0.1	V
	I_{SINK} = 200 mA		1.5	2.2	0.1	
Output High Level	I_{SOURCE} = 20 mA	13	13.5		Vcc-1.5	
	I_{SOURCE} = 200 mA	12	13.5		Vcc-1.5	
Rise Time	T_J = 25°C, C_L = 1 nF (5)		50	150	X	ns
Fall Time	T_J = 25°C, C_L = 1 nF (5)		50	150	X	
Under-Voltage Lockout Section						
Start Threshold	X842	14.5	16	17.5	16	V
Min. Operating Voltage After Turn On	X842	8.5	10	11.5	10	
PWM Section						
Maximum Duty Cycle	X842	95%	97%	100%	100%	
Minimum Duty Cycle				0%	0%	
Total Standby Current						

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Start-Up Current			0.5	1	0	mA
Operating Supply Current	$V_{PIN\ 2} = V_{PIN\ 3} = 0$ V		11	17	0	
V_{CC} Zener Voltager	I_{CC} = 25 mA	30	34		30 34	V

X: not implemented

(1) Adjust VCC above the start threshold before setting at 15 V.
(2) These parameters, although specified, are not 100% tested in production.
(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$Temp_{Stability} = (Max(V_{REF}) - Min(V_{REF})) / (Max(T_j) - Min(T_j))$$

VREF(max) and VREF(min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency for the UC1842 and UC1843. Output frequency is one half oscillator frequency for the UC1844 and UC1845.
(5) These parameters, although specified, are not 100% tested in production.
(6) Parameter measured at trip point of latch with $V_{PIN2} = 0$.
(7) Gain defined as:

$$A=\Delta V_{PIN1}/\Delta V_{PIN3} ; 0 \leq V_{PIN3} \leq 0.8 \text{ V}$$

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Example circuit :

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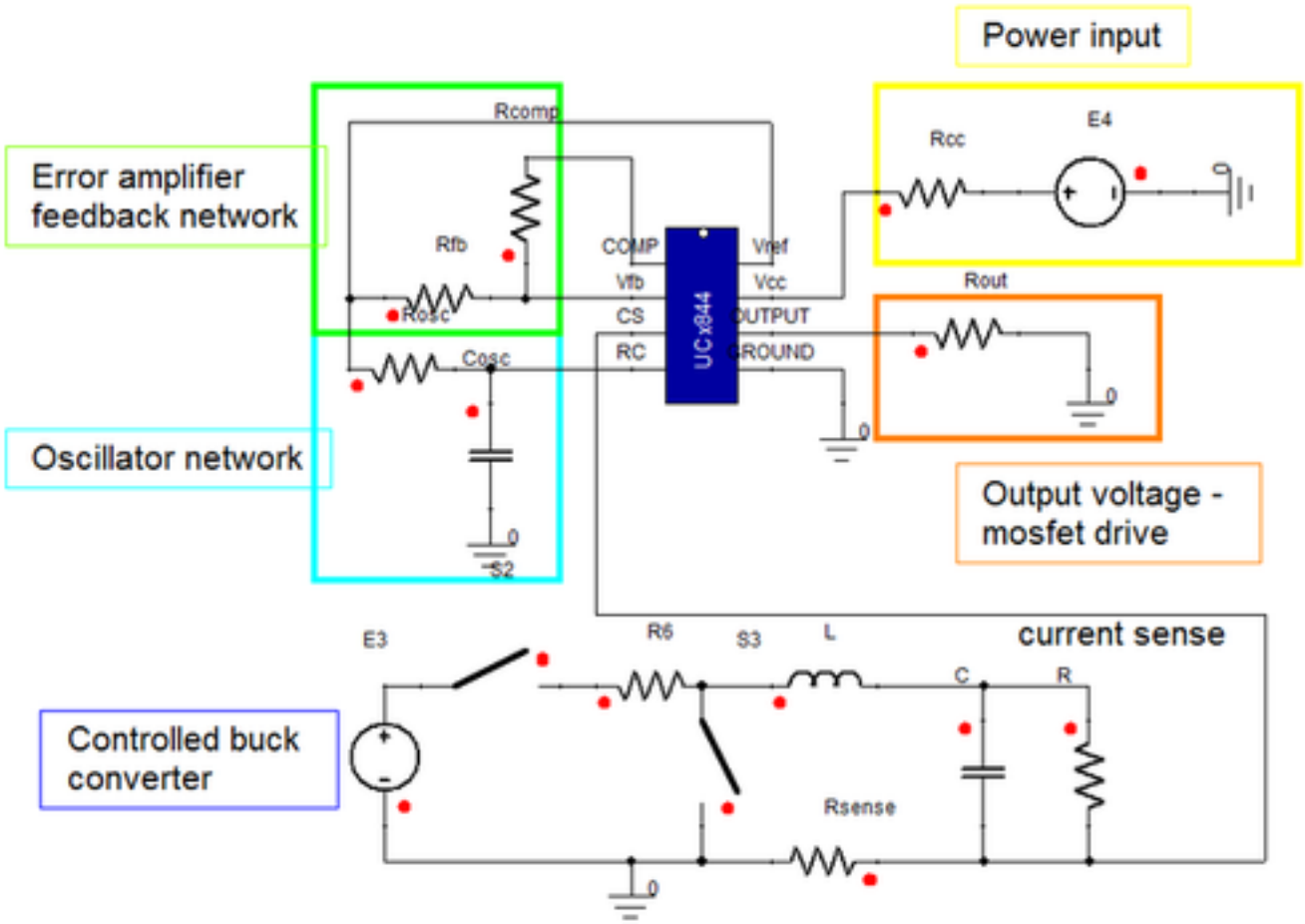

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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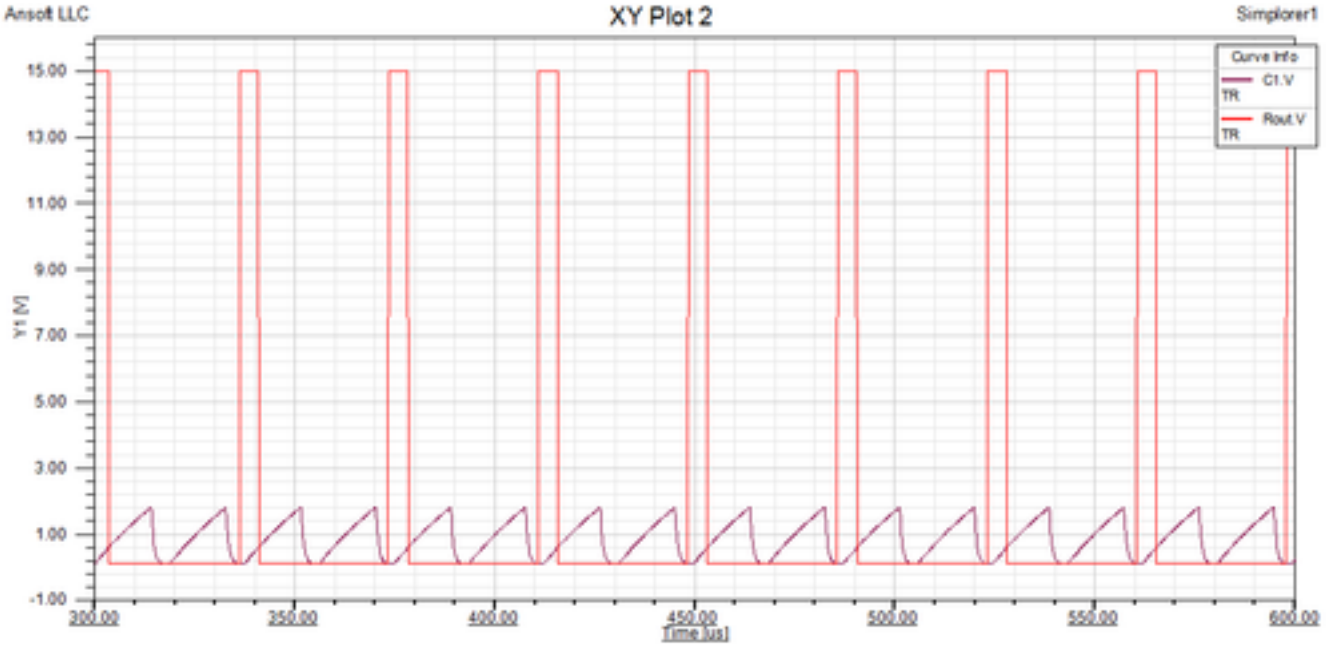

Red: output voltage

Purple: oscillator voltage

Figure 3. Simulation results

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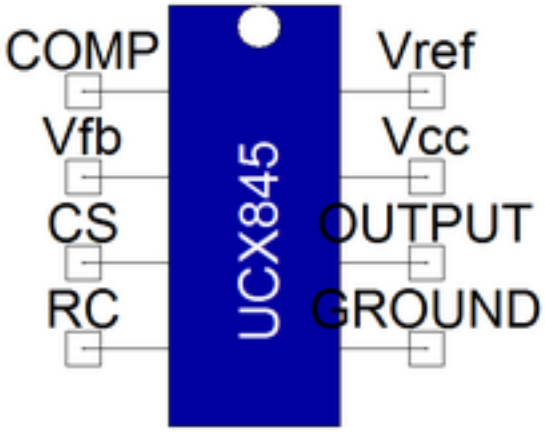
UCx845: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCX842/3/4/5* family of control devices provides the necessary features to implement off-line or dc-to-dc fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

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Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The *UCX842* and *UCX844* have UVLO thresholds of 16 VON and 10 VOFF, ideally suited to off-line applications. The corresponding thresholds for the *UCX843* and *UCX845* are 8.4 V and 7.6 V. The *UCX842* and *UCX843* can operate to duty cycles approaching 100%. The *UCX844* and *UCX845* have a range of zero to 50%.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:

• Error amplifier: COMP pin is connected to its output and Vfb pin is connected to the inverting input.
• Current sense: a voltmeter measures the voltage on CS pin. The input impedance is infinite.
• Oscillator: when a resistor and a capacitor are connected to the RC pin, an oscillator circuit is achieved. Its period depends on the resistance and capacity.
• Reference voltage: provides an ideal 5V voltage reference with zero output impedance. It sets to 0V if the power input falls below the under-voltage value.
• Power input: voltage limited by a zener diode to 34V. Input current is modeled with a current source whose value is the sum of the output current and the voltage reference current.
• Output voltage: controlled by a state machine. Its output impedance is zero.

The state machines control the under-voltage protection (when the input voltage falls below 7.6V, the protection activates and the output and the reference fall to zero), the oscillator and the output voltage.

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Conservative Pins

Table 1

Symbol	Description
COMP	Output of the error amplifier
Vfb	Inverting input of the error amplifier
CS	Input to the current sense comparator

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RC	Oscillator timing pin
V_{ref}	Voltage reference
V_{CC}	Power input
OUTPUT	Output of the driver
GROUND	Reference ground and power ground

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Parameters

Comparison between model and real component.

Unless otherwise stated, the real component specifications apply for -55°C ≤TA ≤125°C for the UC184X; -40°C ≤TA≤85°C for the UC284X; 0°C ≤TA≤70°C for the 384X; VCC = 15 V(1); RT = 10 kΩ; CT = 3.3 nF, TA = TJ.

Table 2

Parameter	Real Component Test Conditions	UCx842/3/4/5			Model	Unit
		Min	Typ	Max		
Reference Section						
Output Voltage	T_J = 25°C, IO = 1 mA	4.90	5.00	5.10	5.00	V
Line Regulation	12V ≤ V_{IN} ≤ 25 V		6	20	0	mV
Load Regulation	1 mA ≤ I_0 ≤ 20 mA		6	25	0	
Temp. Stability	See (2) (3)		0.2	0.4	0	mV/°C
Total Output Variation	Line, load, temperature (2)	4.82		5.18	0	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C (2)		50		0	µV
Long Term Stability	T_A = 125°C, 1000 Hrs (2)		5	25	0	mV
Output Short Circuit		-30	-100	-180	X	mA
Oscillator Section						
Initial Accuracy	T_J = 25°C (4)	47	52	57	52	kHz
Voltage Stability	12V ≤ V_{CC} ≤ 25 V		0.2%	1%	0%	
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (2)		5%		0%	
Amplitude	$V_{PIN\ 4}$ peak-to-peak (2)		1.7		1.7	V
Error Amp Section						
Input Voltage	$V_{PIN\ 1}$ = 2.5 V	2.42	2.50	2.58	2.50	V
Input Bias Current			-0.3	-2	0	A
A_{VOL}	2V≤V_O≤ 4 V	65	90		90	dB

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Unity Gain Bandwidth	T_J = 25°C (5)	0.7	1		X	MHz
PSRR	12V ≤ V_{CC} ≤ 25 V	60	70		70	dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7 V, $V_{PIN\ 1}$ = 1.1 V	2	6		0	mA
Output Source Current	$V_{PIN\ 2}$ = 2.3 V, $V_{PIN\ 1}$ = 5 V	-0.5	-0.8		0	
V_{OUT} High	$V_{PIN\ 2}$ = 2.3 V, R_L = 15 k to ground	5	6		6	V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7 V, R_L = 15 k to Pin 8		0.7	1.1	0.7	
Current Sense Section						
Gain	See (6) (7)	2.85	3	3.15	3	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5 V (6)	0.9	1	1.1	1	V
PSRR	12V ≤ V_{CC} ≤ 25 V (5) (6)		70		70	dB
Input Bias Current			-2	-10	0	A
Delay to Output	$V_{PIN\ 3}$ = 0 V to 2 V (5)		150	300	0	ns
Output Section						
Output Low Level	I_{SINK} = 20 mA		0.1	0.4	0.1	V
	I_{SINK} = 200 mA		1.5	2.2	0.1	
Output High Level	I_{SOURCE} = 20 mA	13	13.5		Vcc-1.5	
	I_{SOURCE} = 200 mA	12	13.5		Vcc-1.5	
Rise Time	T_J = 25°C, C_L = 1 nF (5)		50	150	X	ns
Fall Time	T_J = 25°C, C_L = 1 nF (5)		50	150	X	
Under-Voltage Lockout Section						
Start Threshold	X842	14.5	16	17.5	16	V
Min. Operating Voltage After Turn On	X842	8.5	10	11.5	10	
PWM Section						
Maximum Duty Cycle	X842	95%	97%	100%	100%	
Minimum Duty Cycle				0%	0%	
Total Standby Current						
Start-Up Current			0.5	1	0	mA
Operating Supply Current	$V_{PIN\ 2}$ = $V_{PIN\ 3}$ = 0 V		11	17	0	
V_{CC} Zener Voltager	I_{CC} = 25 mA	30	34		30 34	V

X: not implemented

(1) Adjust VCC above the start threshold before setting at 15 V.
(2) These parameters, although specified, are not 100% tested in production.

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(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$Temp_{Stability} = (Max(V_{REF}) - Min(V_{REF})) / (Max(T_j) - Min(T_j))$

VREF(max) and VREF(min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(4) Output frequency equals oscillator frequency for the UC1842 and UC1843. Output frequency is one half oscillator frequency for the UC1844 and UC1845.
(5) These parameters, although specified, are not 100% tested in production.
(6) Parameter measured at trip point of latch with $V_{PIN2} = 0$.
(7) Gain defined as:

$A=\Delta V_{PIN1}/\Delta V_{PIN3}$; $0 \leq V_{PIN3} \leq 0.8$ V

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Example circuit :

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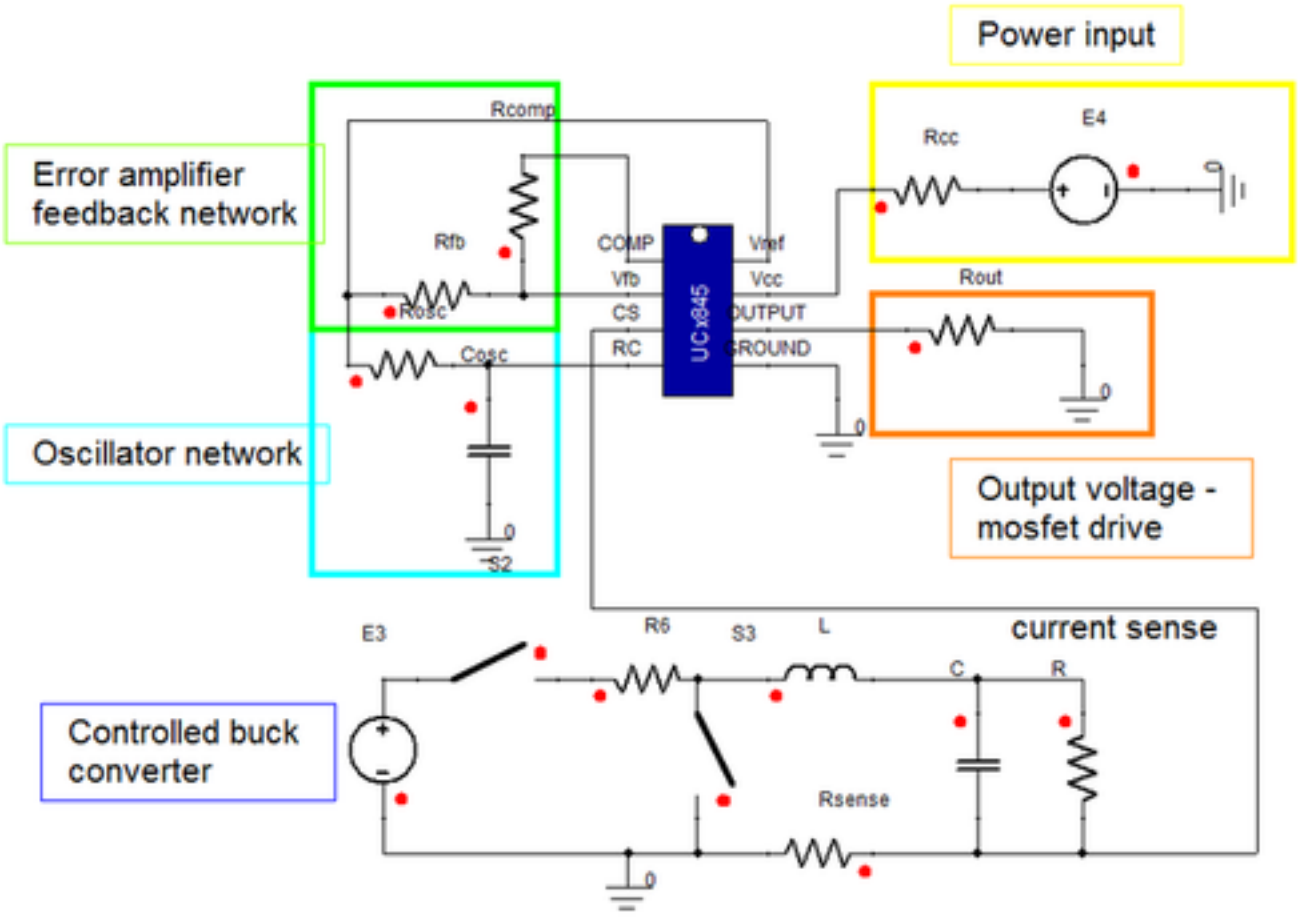

Figure 2. Example Circuit

In this example, the IC controls the switching of a buck converter with current feedback.

Simulation results :

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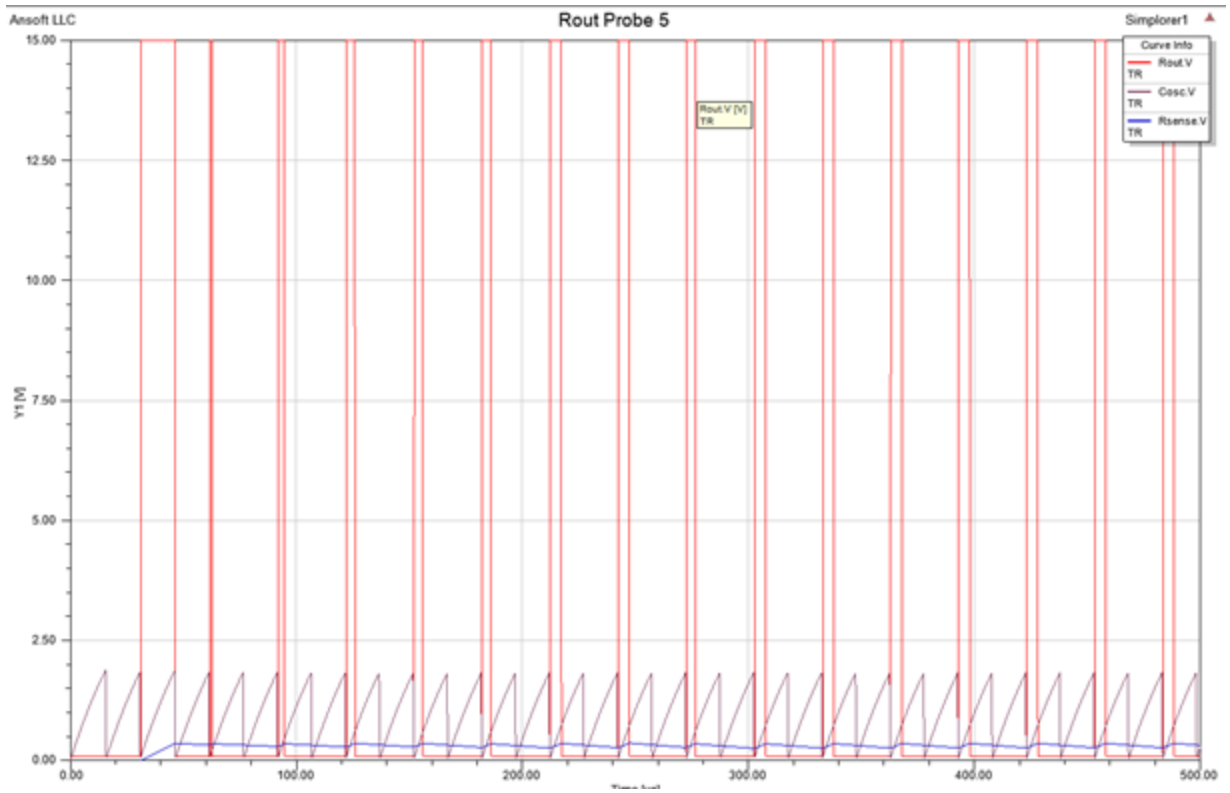

Red: output voltage

Purple: oscillator voltage

Figure 3. Simulation results

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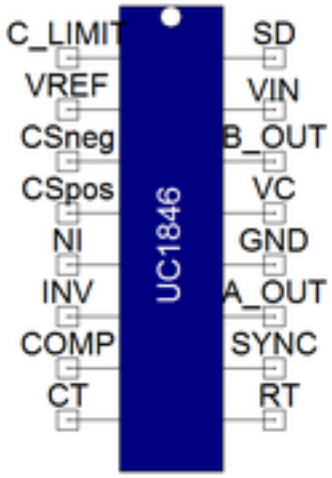
UCx846: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UC1846/7* family of control ICs provides all of the necessaryfeatures to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

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Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression,deadline adjust capability, and a ±1% trimmed bandgap reference.

This model consists of two main parts: the electrical circuit and the state machines which control it.

In the circuit we can find the following parts:

• Error amplifier: COMP pin is connected to its output, INV pin is connected to the inverting input and NI to the non-inverting one.
• Differential current sense: a voltmeter measures the voltage between CS+ and CS- pins.
• Oscillator: Its period depends on the resistance connected to Rt pin and the capacitor to Ct. Sync pin allows synchronizing two UCx846 devices.
• Current limit and soft-start: voltmeters measure the voltage on these pins to set the current peak.
• Reference voltage: provides an ideal 5.1V voltage reference with zero output impedance.
• Outputs A & B: controlled by a state machine. Their output impedance is zero.
• Shutdown: a voltmeter measures the SD pin voltage. When its value falls below 0.350V, the IC shuts down.

The state machines control the under-voltage protection (when the input voltage falls below 7.7V, the protection activates and the outputs fall to zero), the oscillator, the output voltage and the shutdown function.

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Conservative Pins

Table 1

PIN	DESCRIPTION
C_LIMIT	Current limit / Soft-start
VREF	Reference voltage

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C/S-	Differential current sense, negative pin
C/S+	Differential current sense, positive pin
NI	Non-inverting error amplifier input
INV	Inverting error amplifier input
Comp	Error amplifier output
CT	Oscillator capacitor pin
RT	Oscillator resistor pin
Sync	Clock and synchronization pin
A Out	A output
Gnd	Ground
VC	Power supply voltaje
B Out	B output
VIN	Supply voltaje
Shutdown	Shutdown input

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for TA=-55°C to +125°C for UC1846; -40°C to +85°C for the UC2846; and 0°C to +70°C for the UC3846;VIN=15V, RT=10k, CT=4.7nF, TA=TJ.

Table 2

PARAMETER	TEST CONDITIONS	UC1846			MODEL	UNITS
		MIN.	TYP.	MAX.		
Reference Section						
Output Voltage	T_J=25°C, I_O=1mA	5.05	5.10	5.15	5.10	V
Line Regulation	V_{IN}=8V to 40V		5	20	5-20	mV
Load Regulation	I_L=1mA to 10mA		3	15	0	mV
Tem-	Over Oper-		0.4		0	mV

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perature Stability	ating Range, (Note 2)					/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	5.1-5.3	V
Output Noise Voltage	10Hz ≤ f ≤10kHz, T_J=25°C (Note 2)		100		0	µV
Long TermStability	T_J=125°C, 1000 Hrs. (Note 2)		5		0	mV
Short Circuit Output Current	V_{REF}=0V	-10	-45		X	mA
Oscillator Section						
Initial Accuracy	T_J=25°C	39	43	47	45	kHz
Voltage Stability	V_{IN}=8V to 40V		-1	2	0	%
Temperature Stability	Over OperatingRange (Note 2)		-1		0	%
Sync Output High Level		3.9	4.35		4.35	V
Sync Output LowLevel			2.3	2.5	2.3	V
Sync Input High Level	Pin 8=0V	3.9			3.9	V
Sync Input LowLevel	Pin 8=0V			2.5	2.5	V
Sync Input Current	Sync Voltage=3.9V, Pin 8=0V		1.3	1.5	0	mA
Error AmpSection						
Input Offset Voltage			0.5	5	0	mV
Input BiasCurrent			-0.6	-1	0	µA
Input Offset Current			40	250	0	nA

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Common Mode Range	V_{IN}=8V to 40V	0		V_{IN}-2	X	V
Open Loop Voltage Gain	V_O=1.2 to 3V, V_{CM}=2V	80	105		100	dB
Unity GainBand-width	T_J=25°C (Note 2)	0.7	1.0		X	MHz
CMRR	V_{CM}=0V to 38V, V_{IN}=40V	75	100		100	dB
PSRR	V_{IN}=8V to 40V	80	105		105	dB
Output SinkCur-rent	V_{ID}=-15mV to -5V, $V_{PIN\ 7}$=1.2V	2	6		X	mA
Output SourceCur-rent	V_{ID}=15mV to 5V, $V_{PIN\ 7}$=2.5V	-0.4	-0.5		X	mA
High Level Output Voltage	R_L=(Pin 7) 15kΩ	4.3	4.6		4.6	V
Low Level Output Voltage			0.7	1	0	V
Current SenseAmplifierSection						
Amplifier Gain	$V_{PIN\ 3}$=0V, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	3	
Maximum Differential Input Signal ($V_{PIN\ 4}$-$V_{PIN\ 3}$)	Pin 1 Open (Note 3) R_L (Pin 7)=15kΩ	1.1	1.2		X	V
Input Offset Voltage	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		5	25	0	mV
CMRR	V_{CM}=1V to 12V	60	83		∞	dB
PSRR	V_{IN}=8V to 40V	60	84		∞	dB
Input BiasCur-rent	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		-2.5	-10	0	µA
Input Offset Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		0.08	1	0	µA

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Input Com-monMode Range		0		V_{IN}-3	X	V
Delay to Outputs	T_J=25°C, (Note 2)		200	500	0	ns
Current LimitAdjustSection						
Current Limit Offset	$V_{PIN\ 3}$=0V, $V_{PIN\ 4}$=0V, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.5	V
Input BiasCur-rent	$V_{PIN\ 5}$=V_{REF}, $V_{PIN\ 6}$=0V		-10	-30	0	µA
Shutdown Terminal Section						
Threshold Voltage		250	350	400	350	mV
Input Voltage Range		0		V_{IN}	X	V
Minimum Latching Current ($I_{PIN\ 1}$)	(Note 6)	3.0	1.5		1.5	mA
Maximum Non-Latching Current ($I_{PIN\ 1}$)	(Note 7)		1.5	0.8	1.5	mA
Delay to Outputs	T_J =25°C (Note 2)		300	600	300	ns
Output Section						
Collector-Emitter Voltage		40				V
Collector LeakageCurrent	V_C =40V (Note 5)			200	0	µA
Output LowLevel	I_{SINK} =20mA		0.1	0.4	15	V
	I_{SINK} =100m-A		0.4	2.1	15	V
Output High Level	I_{SOURCE} =20mA	13	13.5		15	V
	I_{SOURCE}	12	13.5		15	V

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	=100m-A					
Rise Time	C_L =1nF, T_J =25°C (Note 2)		50	300	X	ns
Fall Time	C_L =1nF, T_J =25°C (Note 2)		50	300	X	ns
Under-Voltage Lockout Section						
Start-Up Threshold			7.7	8.0	7.7	V
Threshold Hys-teresis			0.75		0.75	V
Total StandbyCurrent						
Supply Current			17	21	0	mA

X: not modeled

Note 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3. Parameter measured at trip point of latch with VPIN 5 = VREF, VPIN 6 = 0V.
Note 4. Amplifier gain defined as:

$G = \Delta V_{PIN7} / \Delta V_{PIN4}$; V_{PIN4} = 0 to 1.0V

Note 5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.
Note 6. Current into Pin 1 guaranteed to latch circuit in shutdown state.
Note 7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

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Input/Output Quantities

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Example circuit :

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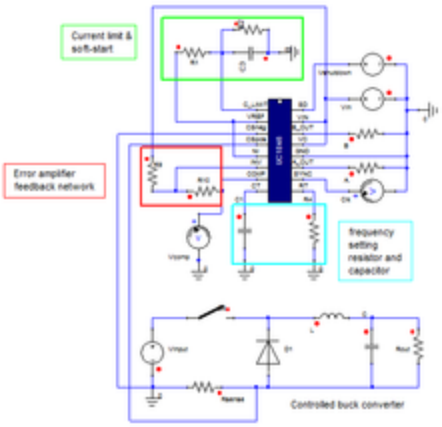
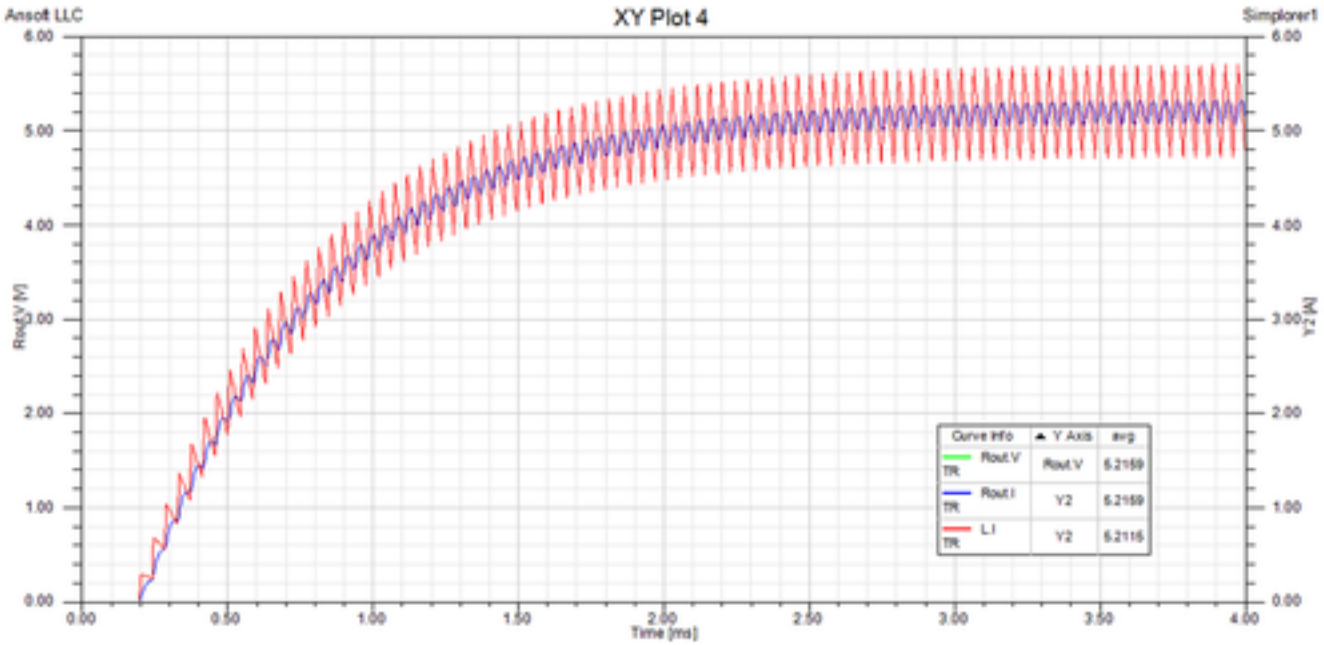


Figure 2. Example Circuit

In this application we are using a UCx846 to control a buck converter in current mode. Apart from the converter itself, the external circuit needed for a proper operation consists of: frequency setting circuit (a resistor and a capacitor), error amplifier feedback network, soft-start capacitor and input and current limit circuitry.

In a real application the output would be connected to a MOSFET gate or a driver input pin. Here we are using a simple resistor whose voltage value opens and closes the converter switch.

Simulation results :



Red: inductor current

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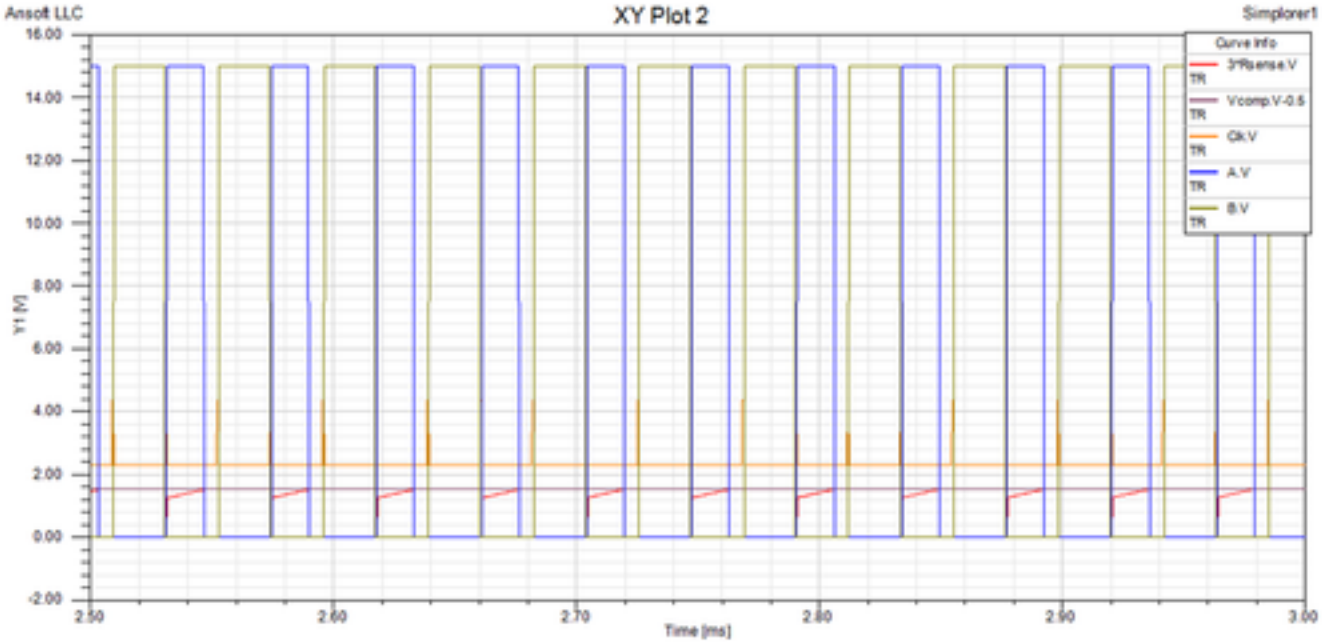
Blue: load current (right scale, in Amps), load voltage (left scale, in Volts)

Figure 3. Simulation results(a)



Red: current sense resistor voltage * 3

Blue: A output voltage

Green: B output voltage

Orange: clock

Purple: error amplifier output voltage - 0.5V

Figure 4. Simulation results(b)

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References

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UCx8741: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

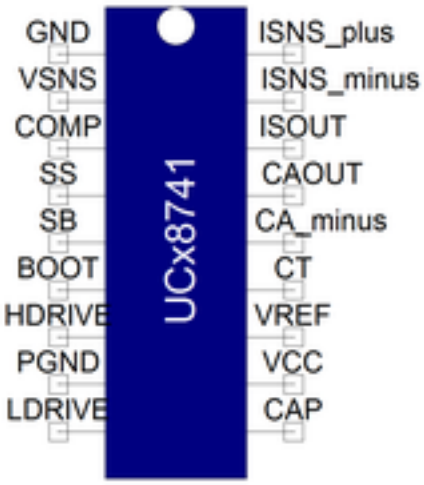

Figure 1. Component symbol

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Description

The *UC3874* family of synchronous step-down (Buck) regulators provides high efficiency power conversion from an input voltage range of 4.5 to 36 volts. The UC3874 is tailored for battery powered applications such as laptop computers, consumer products, communications systems, and aerospace which demand high performance and long battery life. The synchronous regulator replaces the catch diode in the standard buck regulator with a low Rds(on) N-channel MOSFET switch allowing for significant efficiency improvements. The high side N-channel MOSFET switch is driven out of phase from the low side N-channel MOSFET switch by an on-chip bootstrap circuit which requires only a single external capacitor to develop the regulated

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gate drive. Fixed frequency, average current mode control provides the regulator with inherent slope compensation, tight regulation of the output voltage, and superior load and line transient response. Switching frequencies up to 300kHz are possible.

Light load efficiency is improved by a fully programmable standby mode, in which the quiescent current consumption of the controller is significantly reduced. The reduction is achieved by disabling the MOSFET driver outputs and the internal oscillator when the controller has sensed that the output load current has dropped a user programmable amount from full load.

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Conservative Pins

Table 1

PIN	NAME	FUNCTION
1	GND	Ground
2	VSNS	VoltageamplifierInverting Input
3	COMP	Compensation
4	SS	SoftStart
5	SB	Standby
6	BOOT	Bootstrap
7	HDRIVE	High Side Driver Output
8	PGND	Power Ground
9	LDRIVE	LowSide Driver Output
10	CAP	Capacitor Bypass
11	VCC	SupplyVoltage
12	VREF	Voltage Reference
13	CT	Oscillator Capacitor
14	CA_minus	CurrentAmplifierInverting Input
15	CAOUT	CurrentAmplifier Output
16	ISOUT	Currentsense Output
17	ISNS_minus	Currentsense (-)
18	ISNS_plus	Currentsense (+)

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Parameters

Comparison between model and real component.

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Table 2

PARAMETER	TEST CONDITIO-NS	MIN	TY-P	MAX	MODE-L	UNIT-S
Overall Section						
Supply Cur-rent, Sleep	SOFTSTA-RT = 0V; TA=25°C		30	75	30	uA
Supply Cur-rent, Oper-ating			8.5	12	8.5	mA
Supply Cur-rent, Standby	UC2874-1, UC3874-1		2.5	3.5	2.5	mA
Supply Cur-rent, Standby	UC1874-1			5.5	2.5	mA
VCC Turn-onThreshold	UCX874-1		4.5	4.8	4.5	V
VCC Turn-off Threshold	UCX874-1	4.1	4.4		4.4	V
Voltage AmplifierSection						
Input Voltage	TA = 25°C	1.97	2	2.03	2	V
VSNS BiasCur-rent		-500	25	500	0	nA
Transcon-ductance	ICOMp = +10 A to -10 A, UC3874 -1; UC2874-1,	400	675	1000	675	uS
Transcon-ductance	ICOMp = +5 A to -5 A, UC1874-1	250	675	1250	675	uS
VOUT High		2.8	3.1	3.25	3.2	V
VOUT Low	SB = VREF			1.85	1.25	V
Output SourceCurrent	VOUT = 1V; UC3874-1; UC2874-1	10	35		-	uA
	VOUT = 1V; UC1874 -1	5	35		-	uA
Current AmplifierSection						
Input Offset Voltage	VCOMP = 2.5V	-6	0	6	0	mV
Input BiasCur-	VCM =	-500		500	0	nA

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rent (SENSE)	2.5V					
Open LoopGain	VCM = 2.5V, VOUT = 1V to 3.5V	80	110		110	dB
VOUT High	RCAOUT = 100k to GND, TA = 25°C	3.6	3.7		3.7	V
VOUT Low	RCAOUT = 100k to VREF, TA = 25°C		0.7	0.86	0.7	V
Output SourceCurrent	VOUT = 0V, TA = 25°C	80	100	120	-	uA
Common Mode REJ Ratio	VCM = 2V to 3V	70	90		90	dB
Gain Band-widthProduct	FIN = 100kHz, 10mV p-p	2	3.5		3.5	MHz
Reference Section						
Output Voltage	IREF = 0mA, TA = 25°C	2.46-2	2.5	2.53-8	2.5	V
	IREF = 0mA	2.43-7	2.5	2.56-3	2.5	V
Load Regu-lation	IREF = 0mA to 5mA		2	15	2	mV
Line Regu-lation	VCC = 12V to 24V		2	15	0	mV
Short CircuitCurrent	VREF = 0V	10	20	25	20	mA
Oscillator Section						
Initial Accur-acy	TA = 25°C	85	100	115	100	kHz
Voltage Stab-ility	VCC = 12V to 18V		1	1.5	-	%
Total Variation	Line, Tem-perature	80		120	X	kHz
Ramp Amplitude (p-p)	TA = 25°C	2.48	2.7	2.85	2.7	V
Ramp Valley Voltage	TA = 25°C	0.86	0.9-5		0.95	V

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Sleep/Soft Start/Bootstrap Section						
Sleep Threshold	Measured on SS, TA = 25°C	0.25	0.6	0.8	-	V
SS ChargeCur-rent	VSS = 2.5V	4	6	10	6	uA
SS DischargeCur-rent	VSS = 2.5V	0.5	0.8		0.8	mA
Bootstrap Regulation Voltage	UCX874-1, Low Driver ON	6	7.5	9	7.5	V
Bootstrap Refresh Voltage	UCX874-1, VCAOUT> VCTPEAK	2.7	3.5	4	-	V
High Side Driver Output Section						
Output High Voltage	IOUT = -50mA, Boot = 23V	21	22.-2		19.2	V
Output LowVoltage	IOUT = 50mA		1	2.2	0	V
	IOUT = 10mA		300	500	-	mV
Output Low (UVLO)	IOUT = 50mA, VCC = 0V		0.9	1.5	-	V
Output Rise Time	COUT = 1nF		40	160	40	ns
Output Fall Time	COUT = 1nF		30	100	30	ns
Low Side Driver Output Section						
Output High Voltage	IOUT = -50mA, Vcap = 23V	8.8	9.5		7.5	V
Output LowVoltage	IOUT = 50mA		1	2.2	0	V
	IOUT = 10mA		300	500	-	mV
Output Low (UVLO)	IOUT = 50mA, VCC = 0V		0.9	1.5	-	V
Output Rise Time	COUT = 1nF		40	160	40	ns
Output Fall Time	COUT = 1nF		30	100	30	ns
X10 AmplifierSection						
Gain	VISNS =	9.2	9.8	10.4	9.8	V/V

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	20mV to 80mV					
Slew RateRising	TA = 25°C	1	1.4		-	V/us
Slew RateFalling	TA = 25°C	2	3.5		-	V/us
Input Resist-ance	TA = 25°C	60	100	165	100	kOhm

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Examples

Example circuit :

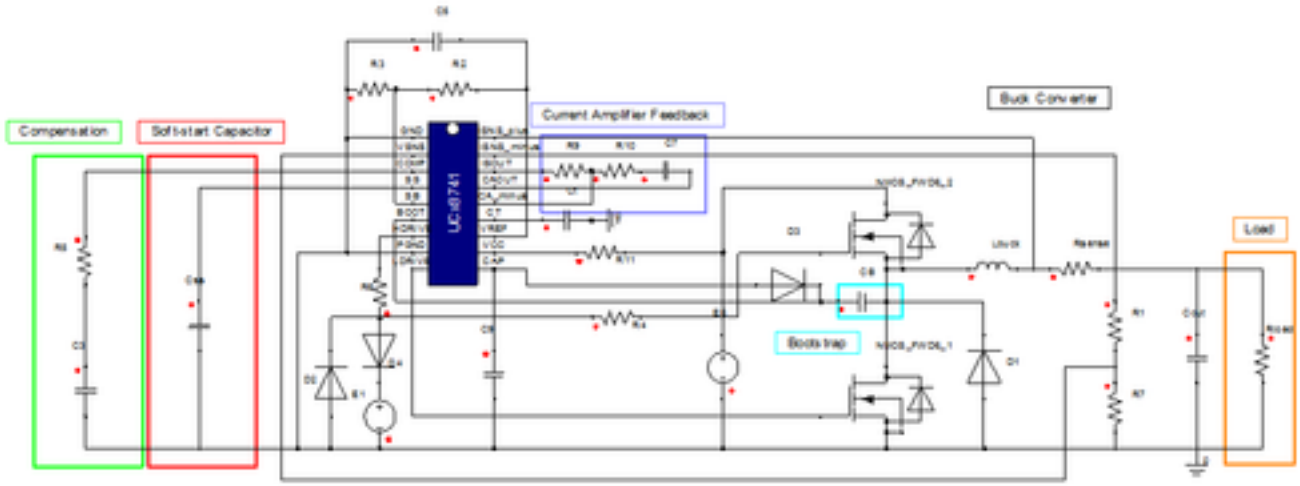

Figure 2. Example Circuit

Simulation results :

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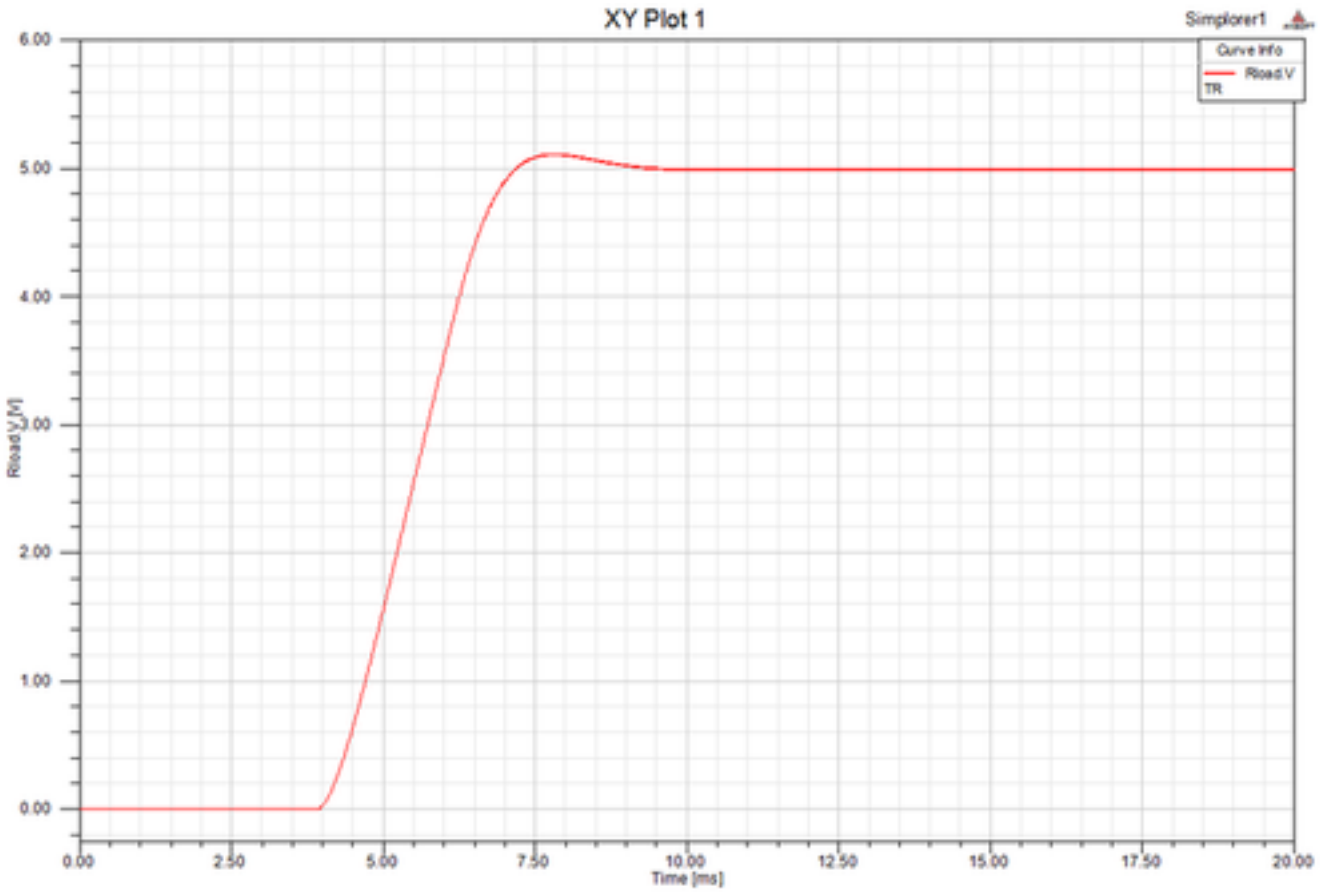

Figure 3. Simulation results

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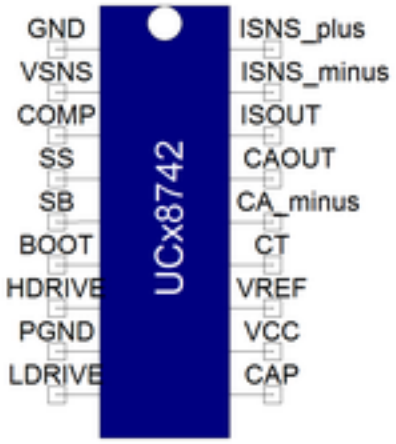
UCx8742: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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17	ISNS_minus	Currentsense (-)
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Parameters

Comparison between model and real component.

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Table 2

PARAMETER	TEST CONDITIO-NS	MIN	TY-P	MAX	MODE-L	UNIT-S
Overall Section						
Supply Cur-rent, Sleep	SOFTSTA-RT = 0V; TA=25°C		30	75	30	uA
Supply Cur-rent, Oper-ating			8.5	12	8.5	mA
Supply Cur-rent, Standby	UC2874-2, UC3874-2		2.5	3.5	2.5	mA
Supply Cur-rent, Standby	UC1874-2			5.5	2.5	mA
VCC Turn-onThreshold	UCX874-2		10	10.5	10	V
VCC Turn-off Threshold	UCX874-2	8.2	9		9	V
Voltage AmplifierSection						
Input Voltage	TA = 25°C	1.97	2	2.03	2	V
VSNS BiasCur-rent		-500	25	500	0	nA
Transcon-ductance	I_{COMP} = +10 A to -10 A, UC3874-2; UC2874-2	400	675	1000	675	uS
Transcon-ductance	I_{COMP} = +5 A to -5 A, UC1874-2	250	675	1250	675	uS
VOUT High		2.8	3.1	3.25	3.2	V
VOUT Low	SB = VREF			1.85	1.25	V
Output SourceCurrent	V_{OUT} = 1V; UC3874-1,-2; UC2874-1,-2	10	35		-	uA
	V_{OUT} = 1V; UC1874 - 1,-2	5	35		-	uA
Current AmplifierSection						
Input Offset Voltage	VCOMP = 2.5V	-6	0	6	0	mV
Input BiasCur-rent (SENSE)	VCM = 2.5V	-500		500	0	nA

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Open LoopGain	VCM = 2.5V, VOUT = 1V to 3.5V	80	110		110	dB
VOUT High	RCAOUT = 100k to GND, TA = 25°C	3.6	3.7		3.7	V
VOUT Low	RCAOUT = 100k to VREF, TA = 25°C		0.7	0.86	0.7	V
Output SourceCurrent	VOUT = 0V, TA = 25°C	80	100	120	-	uA
Common Mode REJ Ratio	VCM = 2V to 3V	70	90		90	dB
Gain Band-widthProduct	FIN = 100kHz, 10mV p-p	2	3.5		3.5	MHz
Reference Section						
Output Voltage	IREF = 0mA, TA = 25°C	2.46-2	2.5	2.53-8	2.5	V
	IREF = 0mA	2.43-7	2.5	2.56-3	2.5	V
Load Regu-lation	IREF = 0mA to 5mA		2	15	2	mV
Line Regu-lation	VCC = 12V to 24V		2	15	0	mV
Short CircuitCurrent	VREF = 0V	10	20	25	20	mA
Oscillator Section						
Initial Accur-acy	TA = 25°C	85	100	115	100	kHz
Voltage Stab-ility	VCC = 12V to 18V		1	1.5	-	%
Total Variation	Line, Tem-perature	80		120	X	kHz
Ramp Amplitude (p-p)	TA = 25°C	2.48	2.7	2.85	2.7	V
Ramp Valley Voltage	TA = 25°C	0.86	0.9-5		0.95	V

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Sleep/Soft Start/Bootstrap Section						
Sleep Threshold	Measured on SS, TA = 25°C	0.25	0.6	0.8	-	V
SS ChargeCur-rent	VSS = 2.5V	4	6	10	6	uA
SS DischargeCur-rent	VSS = 2.5V	0.5	0.8		0.8	mA
Bootstrap Regulation Voltage	UCX874-2, Low Driver ON	9.5	10.-2	12.5	11	V
Bootstrap Refresh Voltage	UCX874-2, VCAOUT> VCTPEAK	7	8	9	-	V
High Side Driver Output Section						
Output High Voltage	IOUT = -50mA, Boot = 23V	21	22.-2		22	V
Output LowVoltage	IOUT = 50mA		1	2.2	0	V
	IOUT = 10mA		300	500	-	mV
Output Low (UVLO)	IOUT = 50mA, VCC = 0V		0.9	1.5	-	V
Output Rise Time	COUT = 1nF		40	160	40	ns
Output Fall Time	COUT = 1nF		30	100	30	ns
Low Side Driver Output Section						
Output High Voltage	IOUT = -50mA, Vcap = 23V	8.8	9.5		11	V
Output LowVoltage	IOUT = 50mA		1	2.2	0	V
	IOUT = 10mA		300	500	-	mV
Output Low (UVLO)	IOUT = 50mA, VCC = 0V		0.9	1.5	-	V
Output Rise Time	COUT = 1nF		40	160	40	ns
Output Fall Time	COUT = 1nF		30	100	30	ns
X10 AmplifierSection						
Gain	VISNS =	9.2	9.8	10.4	9.8	V/V

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	20mV to 80mV					
Slew RateRising	TA = 25°C	1	1.4		-	V/us
Slew RateFalling	TA = 25°C	2	3.5		-	V/us
Input Resist-ance	TA = 25°C	60	100	165	100	kOhm

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Examples

Example circuit :

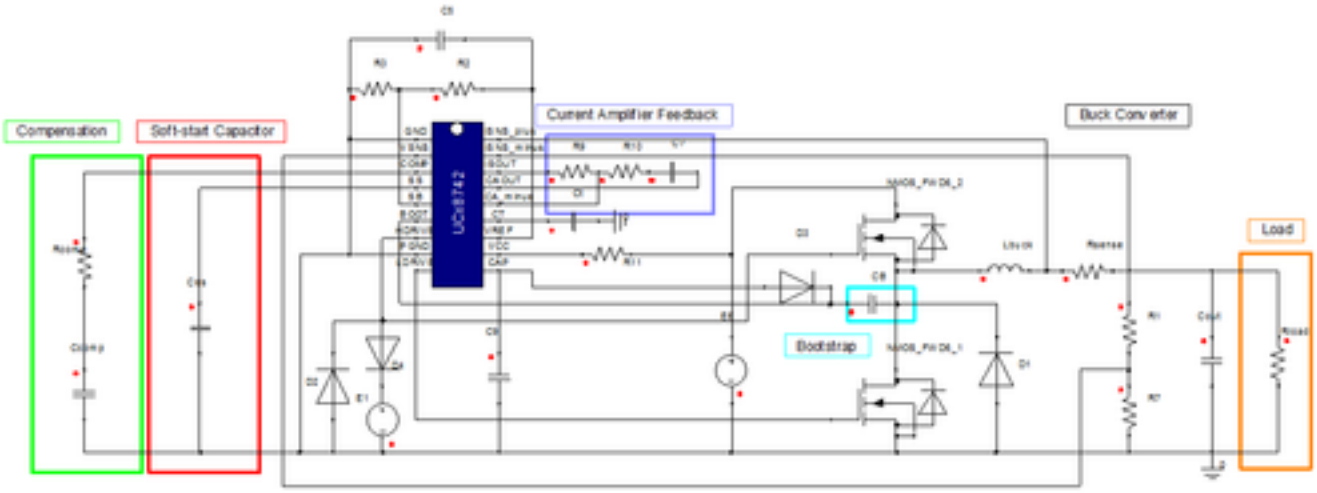

Figure 2. Example Circuit

Simulation results :

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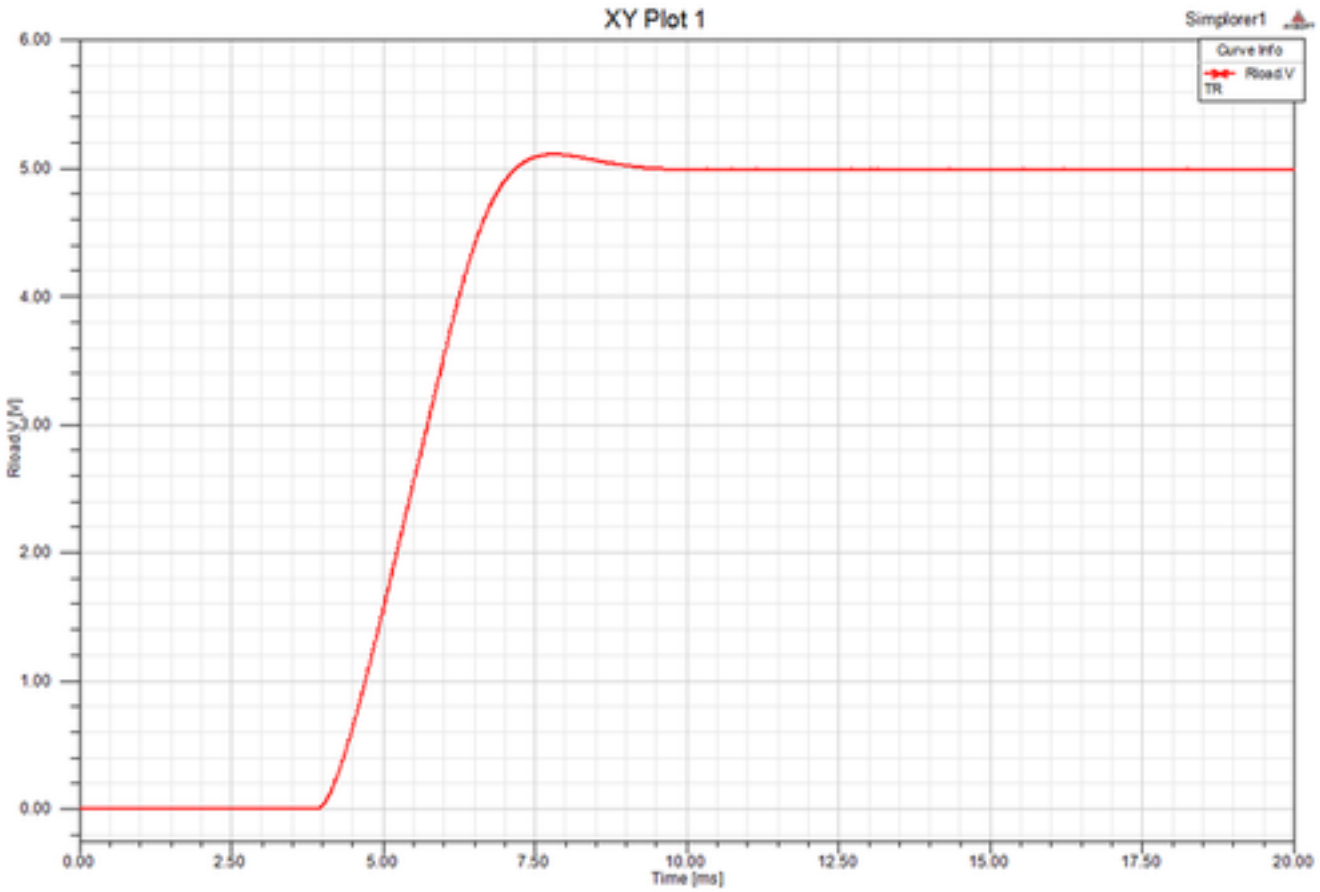

Figure 3. Simulation results

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References

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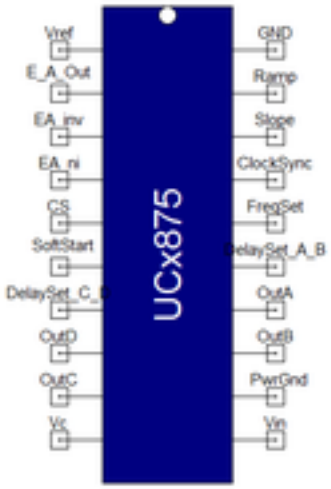
UCx875: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UCx875/6* family of integrated circuits implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This family of circuits may be configured to provide control in either voltage or current mode operation, with a separate over-current shutdown for fast fault protection.

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A programmable time delay is provided to insert a dead-time at the turn-on of each output stage. This delay, providing time to allow the resonant switching action, is independently controllable for each output pair (A-B, C-D).

With the oscillator capable of operation at frequencies in excess of 2MHz, overall switching frequencies to 1MHz are practical. In addition to the standard free running mode, with the CLOCKSYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

Protective features include an undervoltage lockout which maintains all outputs in an active-low state until the supply reaches a 10.75V threshold, 1.5V hysteresis is built in for reliable, bootstrapped chip supply. Over-current protection is provided, and will latch the outputs in the OFF state within 70nsec of a fault. The current-fault circuitry implements full-cycle restart operation.

With the oscillator capable of operation at frequencies in excess of 2MHz, overall switching frequencies to 1MHz are practical. In addition to the standard free running mode, with the CLOCKSYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

In this model we can differentiate two main parts: the electrical circuit and the logic which manages it.

The circuit consists of (from top left and counterclockwise):
- Vref pin, a 5V voltage source.
- Voltage error amplifier.
- Current sense pin, a voltmeter.
- The soft-start circuit.
- Delay measurement circuit.
- Ramp and slope compensation circuit.
- Input voltage pin, a voltmeter.
- Totem-pole outputs.
- Bidirectional clock circuit.
- Frequency setting circuit.

The logic consists of four state machines. The main state machine, the one located at the bottom, controls the main operation of the model. It opens and closes the outputs as a function of the ramp voltage and the output of the error amplifier. This machine also introduces a gap between the switching of the switches on the same leg if it has been configured in the output delay control pin.

Another auxiliary state machine controls the oscillator and the clock.

Finally, the two state machines located at the top control the undervoltage protection, the soft-start function and the overcurrent protection.

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Table 1

Symbol	Description
CLOCKSYNC	Bi-directional clock and synchronization pin
E/AOUT	Error amplifier output
CS+	Current sense
FREQSET	Oscillator frequency set pin
DELAYSET A-B	Output delay control A-B
DELAYSET C-D	Output delay control C-D
EA-	Error amplifier inverting input
EA+	Error amplifier non-inverting input
GND	Signal ground
OUT A	Output A
OUT B	Output B
OUT C	Output C
OUT D	Output D
PWRGND	Power ground
RAMP	Voltage ramp
SLOPE	Set ramp slope/slope compensation
SOFTSTART	Soft start
VC	Output switch supply voltage
VIN	Primary ship supply voltage
VREF	Reference voltage

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Parameters

Comparison between model and real component.

Unless otherwise stated, -55°C < TA < 125°C for the UC1875 V_C=V_{IN}=12V, $R_{FREQSET}$ = 12kΩ, $C_{FREQSET}$ = 330pF, R_{SLOPE}=12kΩ, C_{RAMP}=200pF, $C_{DELAYSET\ A-B}$ = $C_{DELAYSET\ C-D}$ = 0.01µF, $I_{DELAYSET\ A-B}$ = $I_{DELAYSET\ C-D}$ = -500 µA, TA=TJ.

Table 2

PARAMETERS	TEST CONDITIONS	UCx875			MODEL	UNITS
		MIN	TOP	MAX		
Under-Voltage Lockout						
Start Threshold			10.75	11.75	10.75	V
UVLO Hysteresis		0.5	1.25	2.0	1.25	V
Supply Current						
I_{IN} Startup	V_{IN} = 8V, V_C =20V, R_{SLOPE} open, I_{DELAY}=0		150	600	0	µA
I_C Startup			10	100	0	µA
I_{IN}			30	44	0	mA
I_C			15	30	0	mA
Voltage Reference						
Output Voltage	T_J = +25°C	4.92	5	5.08	5	V
Line Regulation	11V < V_{IN} < 20V		1	20	0	mV
Load Regulation	1mA < I_O < 10mA		5	20	0	mV
Total Variation*	Line, Load, Temperature	4.9		5.10	5	V
Noise Voltage*	10Hz < f < 10kHz		50		0	µVrms
Long TermStability*	T_J = 125°C, 1000hrs.		2.5		0	mV
Short CircuitCurrent	V_{REF} = 0V, T_J = +25°C		60		X	mA

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Error Amplifier						
Input Offset Voltage			5	15	0	mV
Input BiasCurrent			0.6	3	0	µA
AVOL	1V < $V_{E/AOUT}$ < 4V	60	90		90	dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		95	dB
PSRR	11V < V_{CC} < 20V	85	100		100	dB
Output SinkCurrent	$V_{E/AOUT}$ = 1V	1	2.5		0	mA
Output SourceCur-rent	$V_{E/AOUT}$ = 4V	-0.5	-1.3		0	mA
Output High Voltage	$I_{E/AOUT}$= -0.5mA	4.0	4.7	5.0	5	V
Output LowVoltage	$I_{E/AOUT}$ = 1mA	0	0 .5	1.0	0	V
Unity GainBand-width		7	11		X	MHz
Slew Rate		6	11		X	V/µsec
PWM Comparator						
Ramp Off-set Voltage	T_J = +25°C		1.3		1.3	V
Zero PhaseShift Voltage		0.-55	0.9		1	V
PWM Phase Shift	$V_{E/AOUT}$ > Ramp Peak + Ramp Off-set	98	99.5	102	100	%
	$V_{E/AOUT}$ < Zero Phase Shift Voltage	0	0.5	2	0	%
Output Skew	$V_{E/AOUT}$ < 1V		5	±20	0	nsec
Ramp to Output			65	125	0	nsec

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Delay						
Oscillator Section						
Initial Accuracy	T_J = 25°C	0.-85	1	1.15	1	MHz
Voltage Stability	11V < V_{CC} < 20V		0.2	2	0	%
Total Variation	Line, Temperature	0.8		1.20	1	MHz
Sync Pin Threshold	T_J = 25°C		3.8		3.5	V
Clock Out Peak	T_J = 25°C		4.3		4.3	V
Clock Out Low	T_J = 25°C		3.3		3.3	V
Clock Out Pulse Width	$R_{CLOCKSYNC}$ = 3.9kΩ		30	100	32	nsec
Maximum Frequency	$R_{FREQSET}$ =5 kΩ	2			2.22	MHz
Ramp Generator/Slope Compensation						
Ramp Current, Minimum	I_{SLOPE} = 10µA, $V_{FREQSET}$ =VREF		-11	-14	X	µA
Ramp Current, Maximum	I_{SLOPE} = 1mA, $V_{FREQSET}$ =VREF	-0.8	-0.95		X	mA
Ramp Valley			0		0	V
Ramp Peak - Clamping Level	$R_{FREQSET}$ =100 kΩ		3.8	4.1	3.9	V
Current Limit						
Input BiasCurrent	V_{CS+} = 0.3V		2	5	0	µA
Threshold Voltage		2.4	2.5	2.6	2.5	V
Delay to Output			85	150	0	nsec
Soft-Start Section						
Charge Current	$V_{SOFTSTART}$ = 0.5V	-20	-9	-3	-9	µA
Discharge	$V_{SOFTSTART}$	12-	230		230	mA

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Current	= 1V	0				
Restart Threshold		4.3	4.7		4.7	V
Discharge Level			300		0.3	mV
Delay Set						
Delay Set Voltage	I_{DELAY}=-500 µA	2.3	2.4	2.6	2.4	V
Delay Time	I_{DELAY}=-250 µA	150	250	600	252	nsec

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Example circuit :

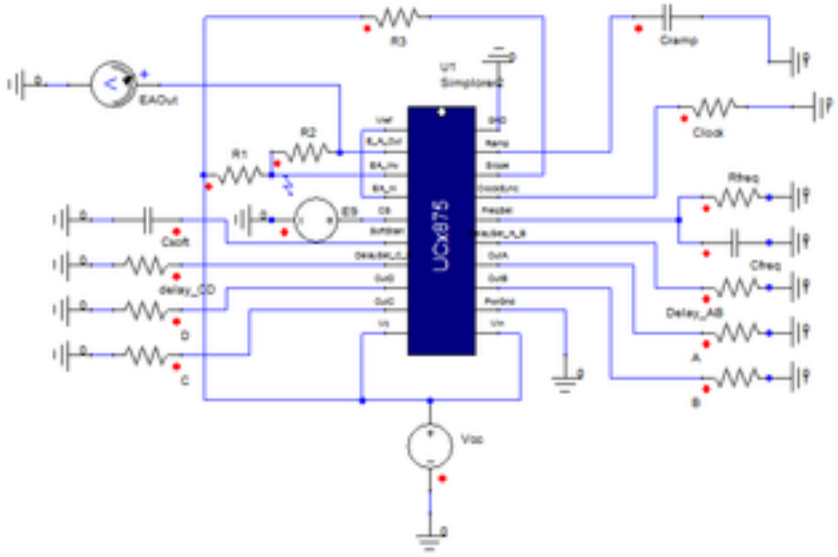

Figure 2. Example Circuit

In a real application, the output pins would be connected to MOSFET gates or to a transformer. Here, they had been replaced with resistors. Using a simpler external circuit allows us to focus in the IC operation.

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Another components connected to the IC are the resistor and the capacitor used to set the oscillator frequency, the feedback network of the error amplifier and the capacitors that set the behavior of the soft-start and the ramp.

We can use the output resistors voltage to control the four switches of a full-bridge inverter:

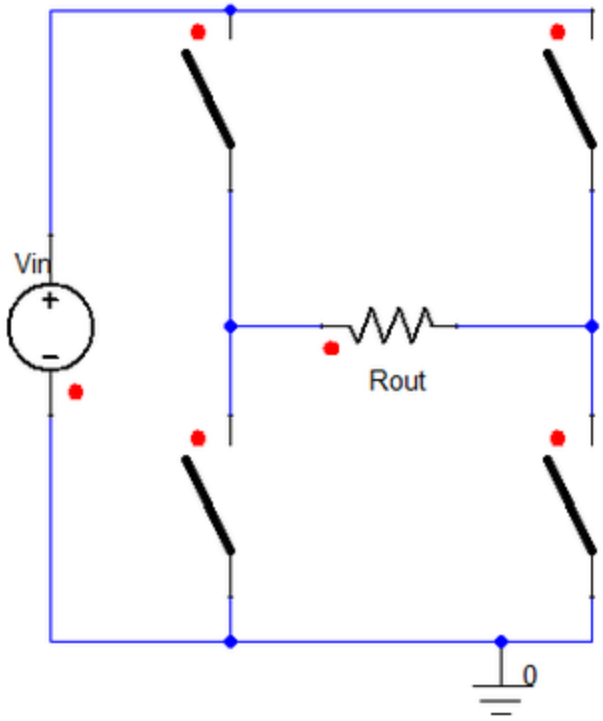

Figure 3. Four Switches Full-bridge Inverter

Simulation results :

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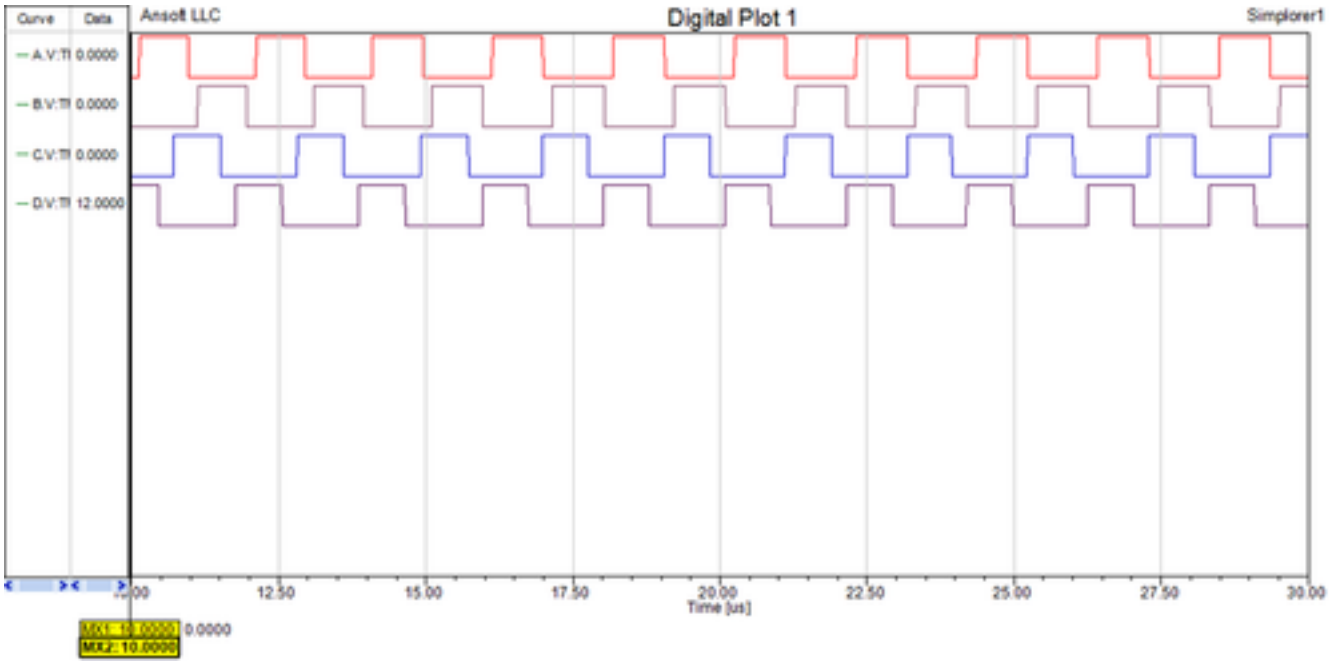

Figure 4. Simulation results(a)

In this figure we can see the four output waveforms. The comparison between the ramp voltage and the error amplifier output voltage sets the AB-CD shift. The shift value is changing in the figure because of the increasing error amplifier output voltage, as shown in the next diagram. The gap between the falling of C and the rising of D, as well as the one between A and B, is fixed by user by connecting a resistor in the delay control pin.

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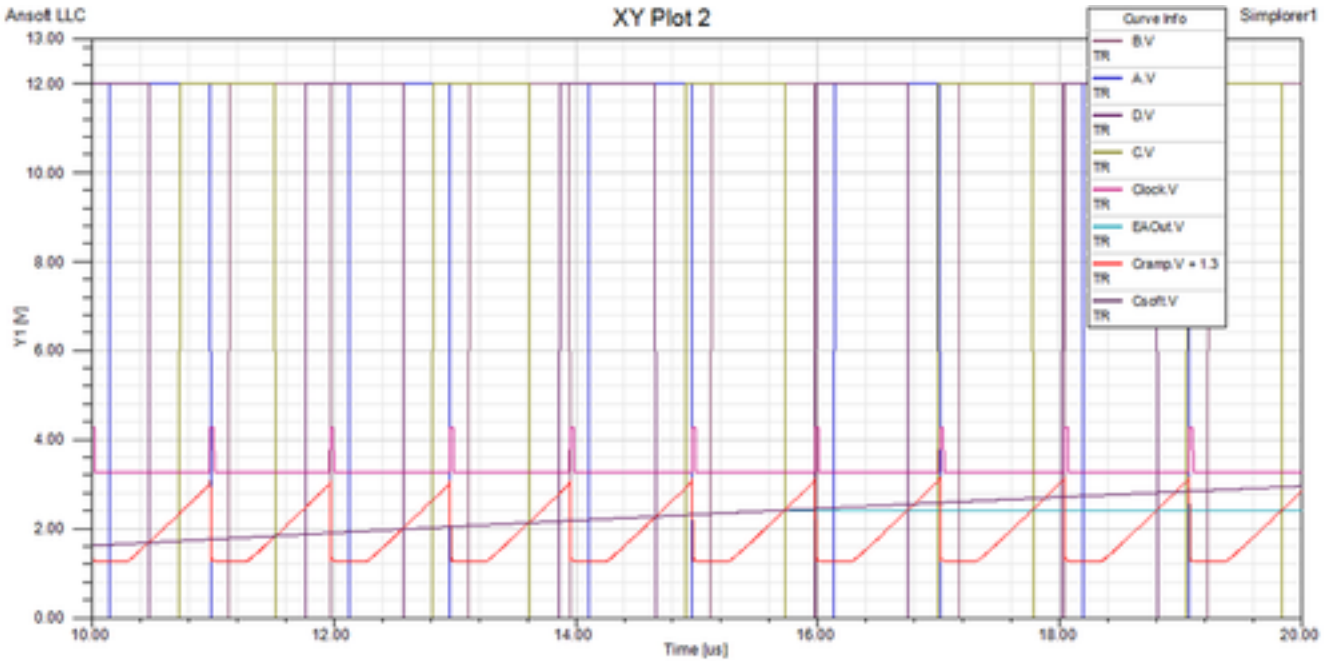

Figure 5. Simulation results(b)

When the error amplifier output voltage (light blue) reaches the ramp voltage (red), C output voltage -or D, depending on the period number- falls. The phase of the A and B outputs is constant and is the C and D the one which shifts.

In the following diagram we can see a detail of the oscillator voltage (red) and the synchronization signal (clock, in purple).

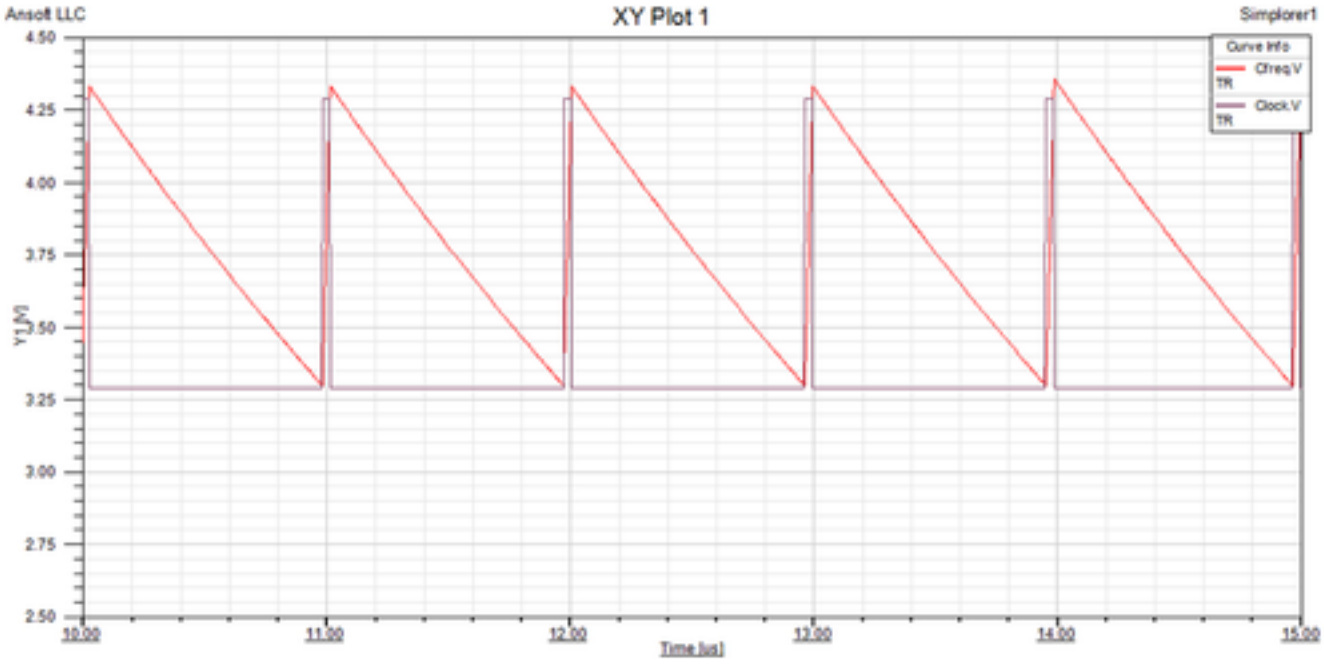

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Figure 6. Simulation results(c)

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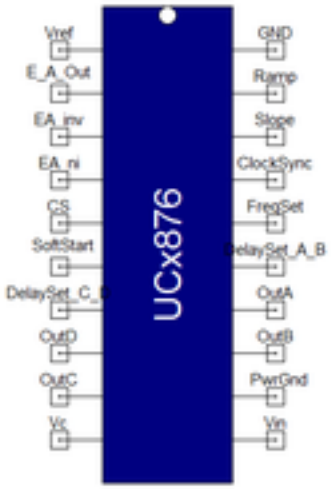
UCx876: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

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With the oscillator capable of operation at frequencies in excess of 2MHz, overall switching frequencies to 1MHz are practical. In addition to the standard free running mode, with the CLOCKSYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

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- Ramp and slope compensation circuit.
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- Totem-pole outputs.
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Table 1

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CS+	Current sense
FREQSET	Oscillator frequency set pin
DELAYSET A-B	Output delay control A-B
DELAYSET C-D	Output delay control C-D
EA-	Error amplifier inverting input
EA+	Error amplifier non-inverting input
GND	Signal ground
OUT A	Output A
OUT B	Output B
OUT C	Output C
OUT D	Output D
PWRGND	Power ground
RAMP	Voltage ramp
SLOPE	Set ramp slope/slope compensation
SOFTSTART	Soft start
VC	Output switch supply voltage
VIN	Primary ship supply voltage
VREF	Reference voltage

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Parameters

Comparison between model and real component.

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Table 2

PARAMETERS	TEST CONDITIONS	UCx876			MODEL	UNITS
		MIN	TOP	MAX		
Under-Voltage Lockout						
Start Threshold			15.25	11.75	15.25	V
UVLO Hysteresis			6.0		6.0	V
Supply Current						
I_{IN} Startup	V_{IN} = 8V, V_C =20V, R_{SLOPE} open, I_{DELAY}=0		150	600	0	µA
I_C Startup			10	100	0	µA
I_{IN}			30	44	0	mA
I_C			15	30	0	mA
Voltage Reference						
Output Voltage	T_J = +25°C	4.92	5	5.08	5	V
Line Regulation	11V < V_{IN} < 20V		1	20	0	mV
Load Regulation	1mA < I_O < 10mA		5	20	0	mV
Total Variation*	Line, Load, Temperature	4.9		5.10	5	V
Noise Voltage*	10Hz < f < 10kHz		50		0	µVrms
Long TermStability*	T_J = 125°C, 1000hrs.		2.5		0	mV
Short CircuitCurrent	V_{REF} = 0V, T_J = +25°C		60		X	mA

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Error Amplifier						
Input Offset Voltage			5	15	0	mV
Input BiasCurrent			0.6	3	0	µA
AVOL	1V < $V_{E/AOUT}$ < 4V	60	90		90	dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		95	dB
PSRR	11V < V_{CC} < 20V	85	100		100	dB
Output SinkCurrent	$V_{E/AOUT}$ = 1V	1	2.5		0	mA
Output SourceCur-rent	$V_{E/AOUT}$ = 4V	-0.5	-1.3		0	mA
Output High Voltage	$I_{E/AOUT}$= -0.5mA	4.0	4.7	5.0	5	V
Output LowVoltage	$I_{E/AOUT}$ = 1mA	0	0 .5	1.0	0	V
Unity GainBand-width		7	11		X	MHz
Slew Rate		6	11		X	V/µsec
PWM Comparator						
Ramp Off-set Voltage	T_J = +25°C		1.3		1.3	V
Zero PhaseShift Voltage		0.-55	0.9		1	V
PWM Phase Shift	$V_{E/AOUT}$ > Ramp Peak + Ramp Off-set	98	99.5	102	100	%
	$V_{E/AOUT}$ < Zero Phase Shift Voltage	0	0.5	2	0	%
Output Skew	$V_{E/AOUT}$ < 1V		5	±20	0	nsec
Ramp to Output			65	125	0	nsec

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Delay						
Oscillator Section						
Initial Accuracy	T_J = 25°C	0.-85	1	1.15	1	MHz
Voltage Stability	11V < V_{CC} < 20V		0.2	2	0	%
Total Variation	Line, Temperature	0.8		1.20	1	MHz
Sync Pin Threshold	T_J = 25°C		3.8		3.5	V
Clock Out Peak	T_J = 25°C		4.3		4.3	V
Clock Out Low	T_J = 25°C		3.3		3.3	V
Clock Out Pulse Width	$R_{CLOCKSYNC}$ = 3.9kΩ		30	100	32	nsec
Maximum Frequency	$R_{FREQSET}$ =5 kΩ	2			2.22	MHz
Ramp Generator/Slope Compensation						
Ramp Current, Minimum	I_{SLOPE} = 10µA, $V_{FREQSET}$ =VREF		-11	-14	X	µA
Ramp Current, Maximum	I_{SLOPE} = 1mA, $V_{FREQSET}$ =VREF	-0.8	-0.95		X	mA
Ramp Valley			0		0	V
Ramp Peak - Clamping Level	$R_{FREQSET}$ =100 kΩ		3.8	4.1	3.9	V
Current Limit						
Input BiasCurrent	V_{CS+} = 0.3V		2	5	0	µA
Threshold Voltage		2.4	2.5	2.6	2.5	V
Delay to Output			85	150	0	nsec
Soft-Start Section						
Charge Current	$V_{SOFTSTART}$ = 0.5V	-20	-9	-3	-9	µA
Discharge	$V_{SOFTSTART}$	12-	230		230	mA

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Current	= 1V	0				
Restart Threshold		4.3	4.7		4.7	V
Discharge Level			300		0.3	mV
Delay Set						
Delay Set Voltage	I_{DELAY}=-500 µA	2.3	2.4	2.6	2.4	V
Delay Time	I_{DELAY}=-250 µA	150	250	600	252	nsec

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Example circuit :

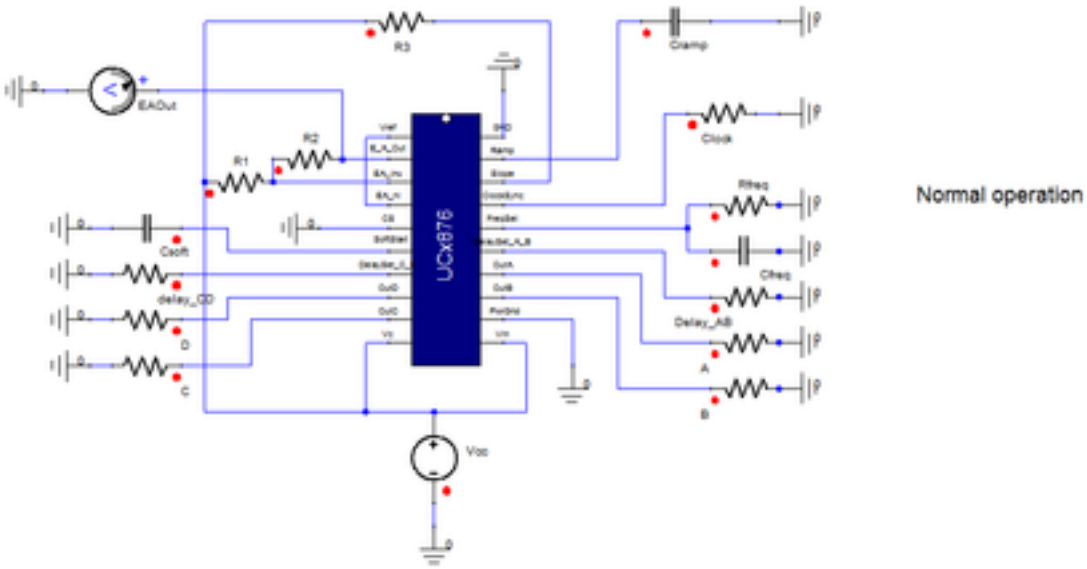

Figure 2. Example Circuit

In a real application, the output pins would be connected to MOSFET gates or to a transformer. Here, they had been replaced with resistors. Using a simpler external circuit allows us to focus in the IC operation.

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Another components connected to the IC are the resistor and the capacitor used to set the oscillator frequency, the feedback network of the error amplifier and the capacitors that set the behavior of the soft-start and the ramp.

We can use the output resistors voltage to control the four switches of a full-bridge inverter:

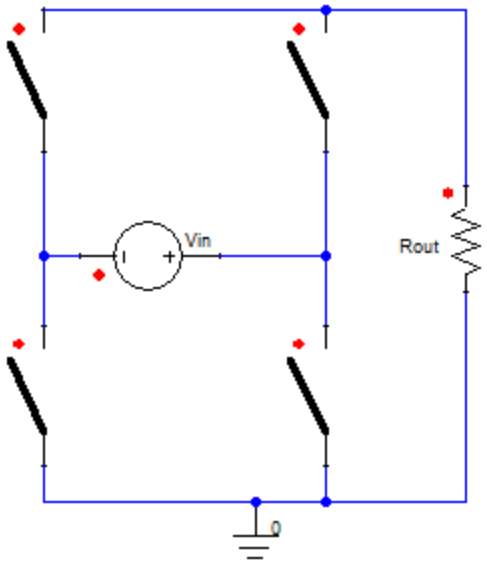

Figure 3. Four Switches Full-bridge Inverter

Simulation results :

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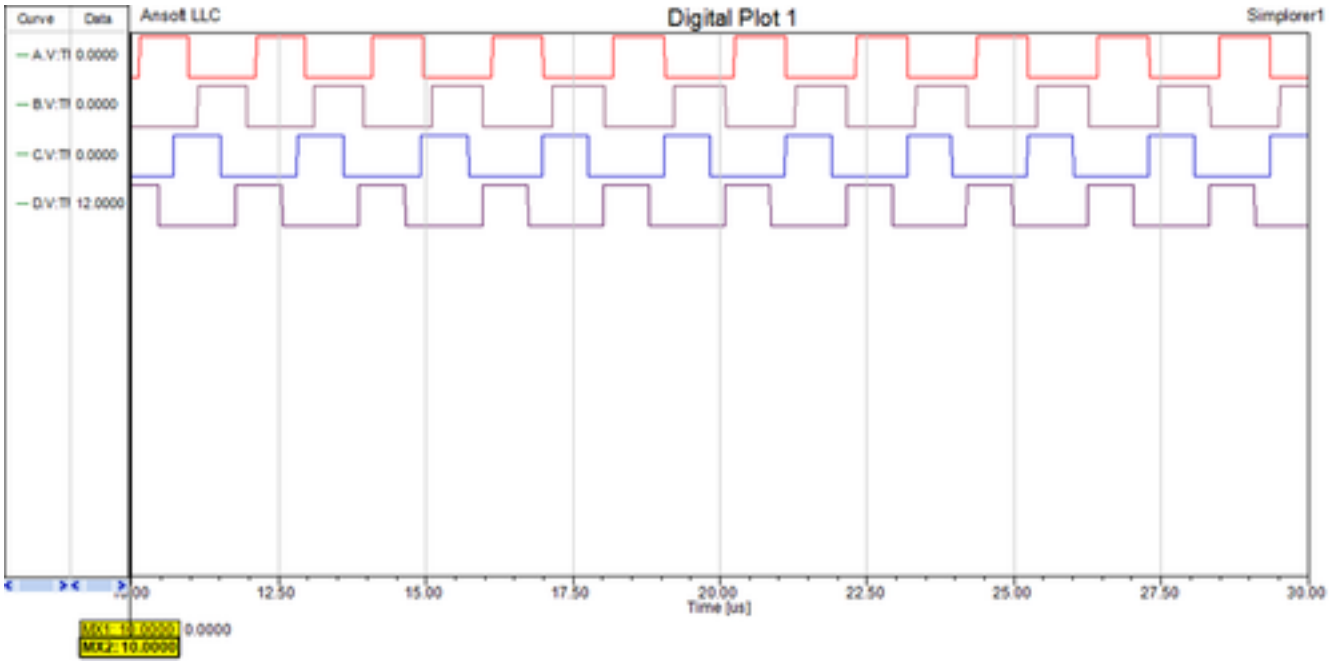

Figure 4. Simulation results(a)

In this figure we can see the four output waveforms. The comparison between the ramp voltage and the error amplifier output voltage set the AB-CD shift. The shift value is changing in the figure because of the increasing error amplifier output voltage, as shown in the next diagram. The gap between the fall of C and the rise of D, as well as the one between A and B, is fixed by user by connecting a resistor in the delay control pin.

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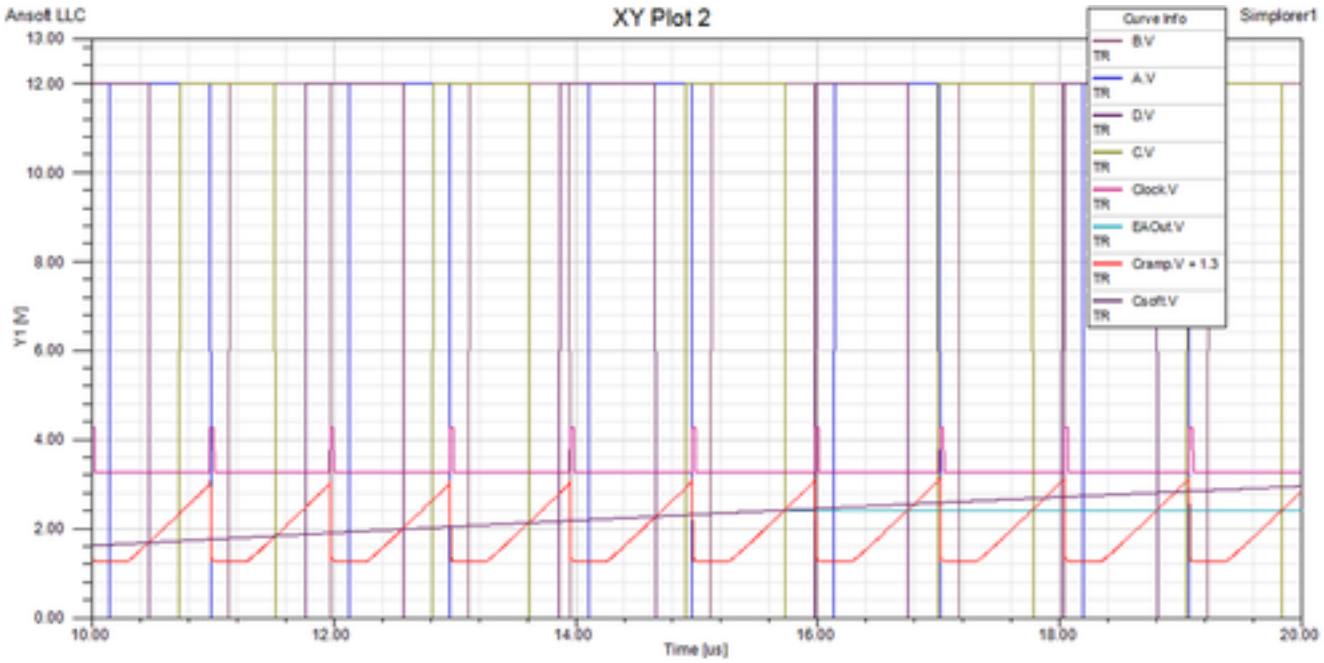

Figure 5. Simulation results(b)

When the error amplifier output voltage (light blue) reaches the ramp voltage (red), C output voltage -or D, depending on the period number- falls. The phase of the A and B outputs is constant and is the C and D the one which shifts.

In the following diagram we can see a detail of the oscillator voltage (red) and the synchronization signal (clock, in purple).

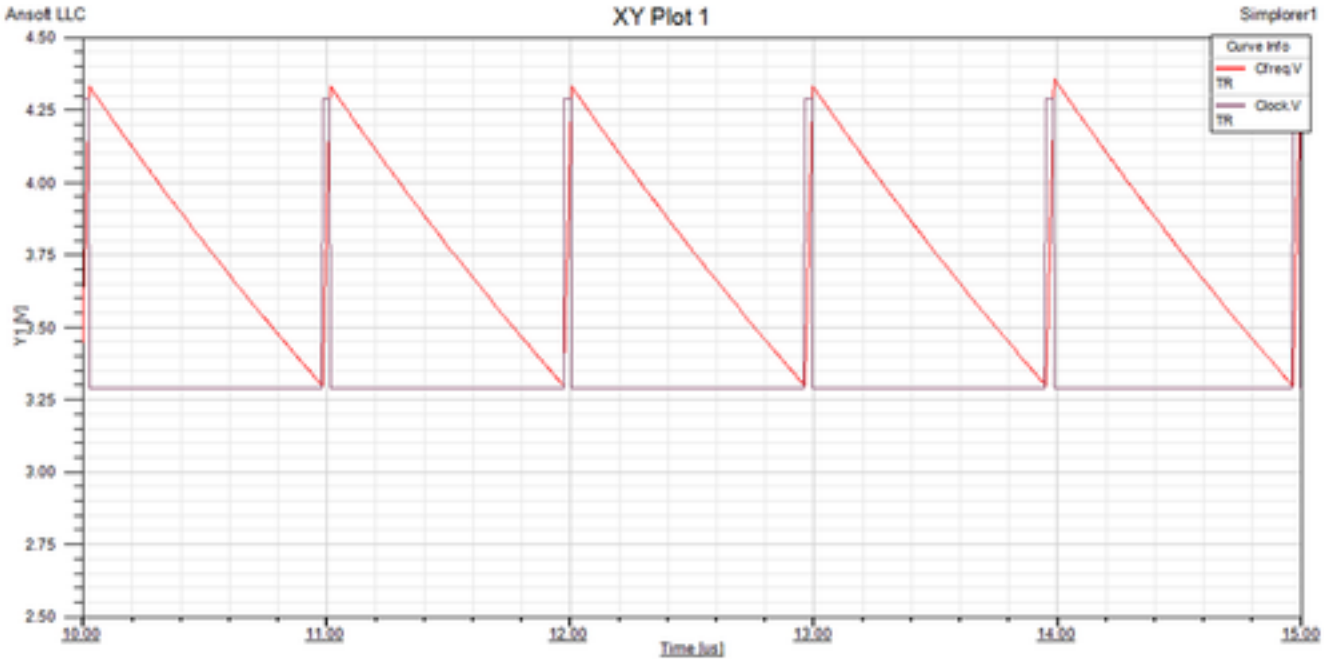

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Figure 6. Simulation results(c)

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References

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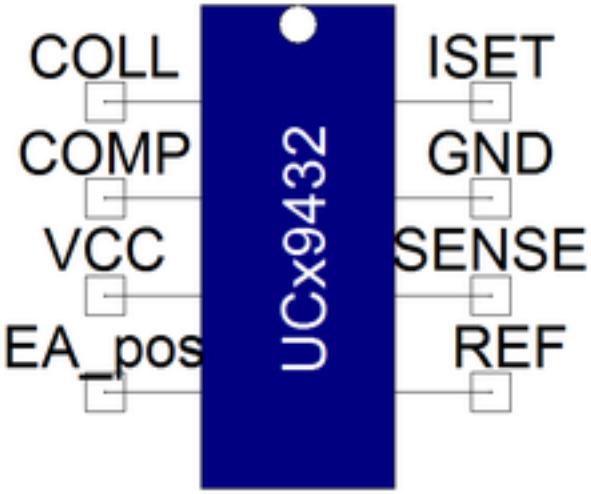
UCx9432: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *UC39432* is an adjustable precision analog controller with 100mA sink capability if the ISET pin is grounded. A resistor between ISET and ground will modify the transconductance while decreasing the maximum current sink. This will add further control in the optocoupler configuration. The trimmed precision reference along with the non-inverting error amplifier inputs are accessible for custom configuration.

This analog controller is based on two ideal operational amplifiers. The rest of the components within the model are used to limit voltage or current in different parts.

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Conservative Pins

Table 1

Pin	Description
COLL	Collector of the output transistor
COMP	Output of the error amplifier
EA_pos	Non-inverting input to the error amplifier
GND	Reference and power ground
ISET	Current set pin for the transconductance amplifier
REF	Output of the trimmed precision reference
SENSE	Inverting input to the error amplifier
VCC	Power connection

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Parameters

Comparison between model and real component.

Unless otherwise stated, these specifications apply for TA = -55°C to +125°C and COLL Output = 2.4V to 36.0V for the UC19432, TA = -25°C to +85°C and COLL Output = 2.3V to 36.0V for the UC29432, and TA= 0°C to +70°C and COLL Output = 2.3V to 36.0V for the UC39432, VCC = 15V, ICOLL = 10mA, TA = TJ.

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Table 2

PARAMETER	REAL COMPONENT TEST CONDITIONS	UCx9432			MODEL	UNITS
		MIN	TYP	MAX		
Reference VoltageTolerance	T_A = 25°C	1.295	1.3	1.305	1.3	V
Reference Temperature Tolerance	V_{COLL} = 5.0V	1.291	1.3	1.309	1.3	V
Reference Line Regulation	VCC = 2.4V to 36.0V, V_{COLL} = 5V		10	38	0	mV
Reference Load Regulation	I_{COLL} = 10mA to 50mA, V_{COLL} = 5V		10	38	0	mV
Reference SinkCurrent				10	10	µA
Reference SourceCurrent				-10	-10	µA
EA Input BiasCurrent		-0.5	-0.2		0	µA
EA Input Offset Voltage				4.0	0	mV
EA Output Current Sink (Internally Limited)				16	16	µA
EA Output CurrentSource				-1	-1	mA
Minimum OperatingCurrent	VCCÂ = 36.0V, V_{COLL} = 5V		0.5	0.8	X	mA
Collector CurrentLimit (Note)	V_{COLL} = VCC = 36.0V, Ref = 1.35V ISET = GND		130	145	X	mA
Collector Saturation	I_{COLL} = 20mA	0.7	1.1	1.5	1.1	V
Transconductance (gm)	VCCÂ = 2.4V to	-170	-140	-110	-140	mS

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(Note)	36.0V, V_{COL} = 3V, I_{COLL} = 20mA ISET = GND					
Error Amplifier AVOL		60	90		90	dB
Error Amplifier GBW	(Note 1)	30	5		X	MHz
Transcon-ductance Amplifier GBW			3		X	MHz

***Note 1**: Guaranteed by design. Not 100% tested in production.*

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Example circuit :

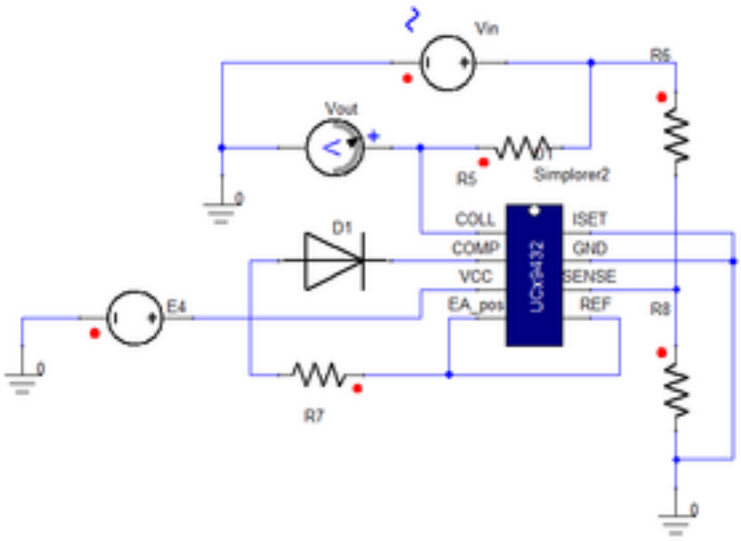

Figure 2. Example Circuit

In this application, the UCx9432 is used to achieve an overvoltage comparator with hysteresis, as shown in the datasheet.

Simulation results :

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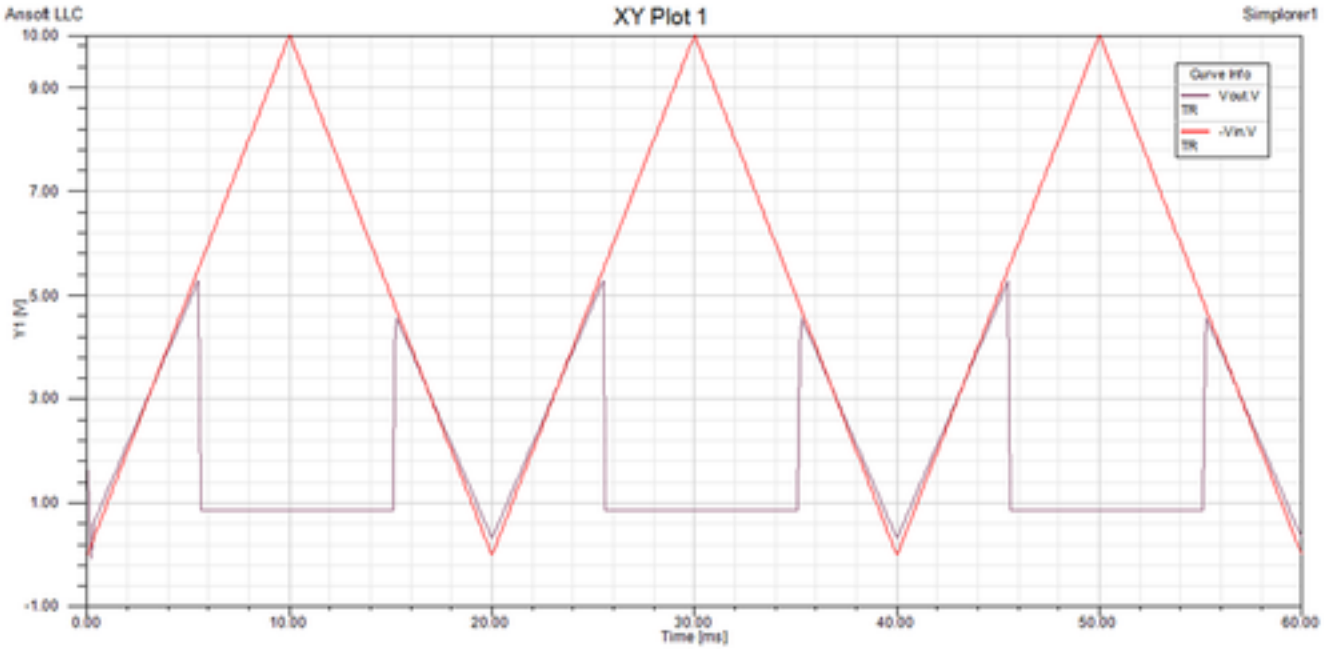

Red: input voltage

Purple: output voltage

Figure 3. Simulation results

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Switching Regulators

Switching Regulators consist of the following types of models:

- LM3150
- LM5116
- LT1533
- LT1931
- LT3690
- LTC3810_5

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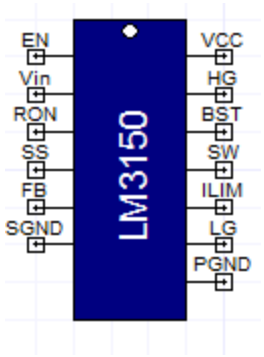
LM3150: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The LM3150 SIMPLE SWITCHER® controller is an easy-to-use and simplified step-down power controller capable of providing up to 12 A of output current in a typical application. Operating with an input voltage range of 6 V to 42 V, the LM3150 controller features an adjustable output voltage down to 0.6 V. The switching frequency is adjustable up to 1 MHz and the synchronous architecture provides for highly efficient designs. The LM3150 controller employs a constant on-time (COT) architecture with a proprietary emulated ripple mode (ERM) control that allows for the use of low ESR output capacitors, which reduces overall solution size and output voltage ripple. The COT regulation architecture allows for fast transient response and requires no loop compensation, which reduces external component count and reduces design complexity.

Fault protection features such as thermal shutdown, undervoltage lockout, overvoltage protection, short-circuit protection, current limit, and output voltage prebias start-up allow for a reliable and robust solution.

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Conservative Pins

Table 1

Name	Description
VCC	Supply Voltage for FET Nominally regulated to 5.95 V. Connect a 1.0-µF to 4.7-µF decoupling Drivers capacitor from this pin to ground.
VIN	Input Supply Voltage Supply pin to the device. Nominal input range is 6 V to 42 V.
EN	To enable the IC, apply a logic high signal to this pin greater than 1.26-V typical or leave floating. To disable the part, ground the EN pin. Internally connected to the regulation, overvoltage, and short-circuit.
FB	Feedback comparators. The regulation setting is 0.6 V at this pin. Connect to feedback resistor divider between the output and ground to set the output voltage.
SGND	Signal Ground for all internal bias and reference circuitry. Should be connected to PGND at a single point.
SS	Soft-Start. An internal 7.7-µA current source charges an external capacitor to provide the soft-start function.
RON	On-time Control. An external resistor from VIN to this pin sets the high-side switch on-time. Monitors current through the low-side switch and triggers current limit
ILIM	Current Limit operation if the inductor valley current exceeds a user defined value that is set by RLIM and the Sense current, ILIM-TH, sourced out of this pin during operation.
SW	Switch Node Switch pin of controller and high-gate driver lower supply rail. A boost capacitor is also connected between this pin and BST pin Gate drive signal to the high-side NMOS switch.
HG	High-Side Gate Drive voltage is supplied by the differential voltage between the BST pin and SW pin. Connection for Bootstrap High-gate driver upper supply rail. Connect a 0.33 to 0.47-µF capacitor from
BST	Connection for Bootstrap High-gate driver upper supply rail. Connect a 0.33 to 0.47-µF capacitor from capacitor SW pin to this pin. An internal diode charges the capacitor during the high-side switch off-time. Do not connect to an external supply rail.
LG	Low-Side Gate Drive Gate drive signal to the low-side NMOS switch. The low-side gate driver voltage is supplied by VCC.
PGND	Power Ground Synchronous rectifier MOSFET source connection. Tie to power ground plane. Should be tied to SGND at a single point.

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Examples

Figure 2 shows an example of connection of the LM3150. This is an example of a 12V to 3,3V buck type converter with output voltage feedback.

Inductor current and output voltage of the converter are shown in Figure 3 and Figure 4, respectively.

Example :

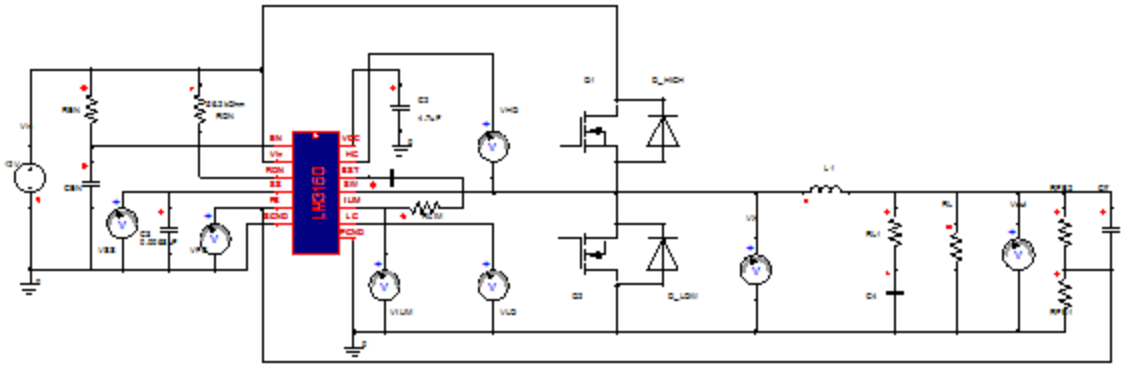

Figure 2. Twin Builder Schematic Example of use of the LM3150

Simulation results :

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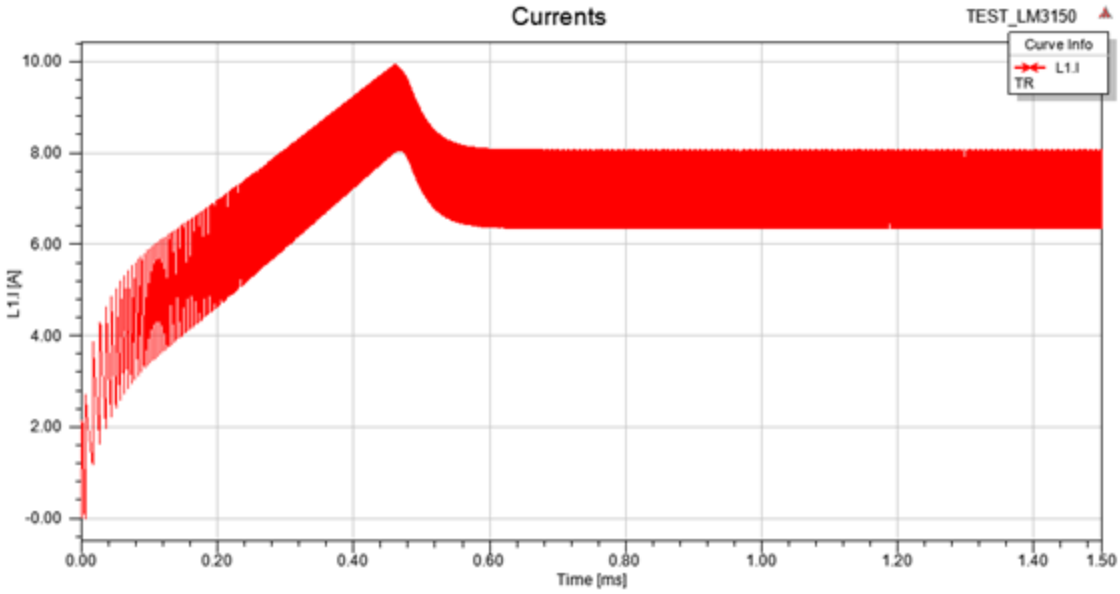

Figure 3. Inductor Current

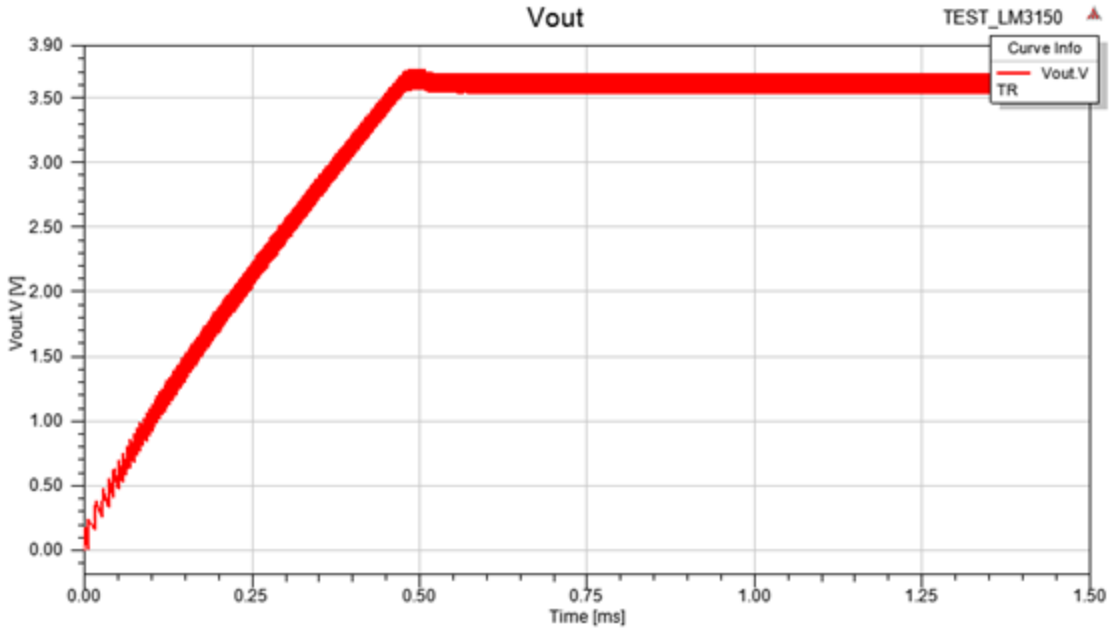

Figure 4: Output Voltage

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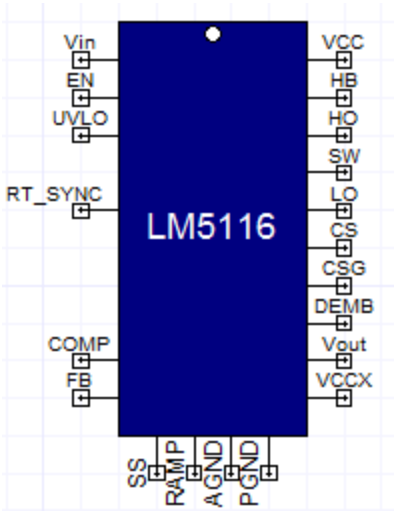
LM5116: Texas Instruments

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The LM5116 is a synchronous buck controller intended for step-down regulator applications from a high-voltage or widely varying input supply. The control method is based upon current mode control utilizing an emulated current ramp. Current mode control provides inherent line feed-fonvard, cycle-by-cycle current limiting, and compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable control of very small duty cycles necessary in high-input voltage applications.

The operating frequency is programmable from 50 kHz to 1 MHz. The LM5116 drives external high-side and low-side NMOS power switches with adaptive dead-time control. A user-

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selectable diode emulation mode enables discontinuous mode operation, for improved efficiency at light load conditions. A low quiescent current shutdown disables the controller and consumes less than 10 µA of total input current. Additional features include a high-voltage bias regulator, automatic switch-over to external bias for improved efficiency, thermal shutdown, frequency synchronization, cycle-by-cycle current limit, and adjustable line undervoltage lockout.

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Conservative Pins

Table 1

Name	Description
AGND	Analog ground. Connect to PGND through the exposed pad ground connection under the LM5116.
COMP	Output of the internal error amplifier. The loop compensation network should be connected between this pin and the FB pin.
CS	Current sense amplifier input. Connect to the top of the current sense resistor or the drain of the low-sided MOSFET if RDS(ON) current sensing is used.
CSG	Current sense amplifier input. Connect to the bottom of the sense resistor or the source of the low-side MOSFET if RDS(ON) current sensing is used.
DEMB	Low-side MOSFET source voltage monitor for diode emulation. For start-up into a pre-biased load, tie this pin to ground at the CSG connection. For fully synchronous operation, use an external series resistor between DEMB and ground to raise the diode emulation threshold above the low-side SW on-voltage.
EN	If the EN pin is below 0.5 V, the regulator is in a low-power state, drawing less than 10 µA from VIN. EN must be pulled above 3.3 V for normal operation. The maximum EN transition time for proper operation is one switching period.
FB	Feedback signal from the regulated output. This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.215 V.
HB	High-side driver supply for bootstrap gate drive. Connect to the cathode of the bootstrap diode and the positive terminal of the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high-side MOSFET gate and should be placed as close to the controller as possible.
HO	Connect to the gate of the high-side synchronous MOSFET through a short, low inductance path.
LO	Connect to the gate of the low-side synchronous MOSFET through a short, low inductance path.

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PGND	Power ground. Connect to AGND.
RAMP	Ramp control signal. An external capacitor connected between this pin and the AGND pin sets the ramp slope used for current mode control.
RT/SYNC	The internal oscillator is set with a single resistor between this pin and the AGND pin. The recommended frequency range is 50 kHz to 1 MHz. The internal oscillator can be synchronized to an external clock by AC coupling a positive edge onto this node.
SS	An external capacitor and an internal 10-µA current source set the soft start time constant for the rise of the error amp reference. The SS pin is held low during VCC < 4.5 V, UVLO < 1.215 V, EN input low, or thermal shutdown.
SW	Switch node. Connect to the negative terminal of the bootstrap capacitor and the source terminal of the high-side MOSFET.
VIN	Chip supply voltage, input voltage monitor, and input to the VCC regulator.
UVLO	If the UVLO pin is below 1.215 V, the regulator is in standby mode (VCC regulator running, switching regulator disabled). If the UVLO pin voltage is above 1.215 V, the regulator is UVLO 2 I operational. An external voltage divider can set an undervoltage shutdown threshold. There is a fixed 5-µA pullup current on this pin when EN is high. UVLO is pulled to ground when a current limit condition exists for 256 clock cycles.
VCC	Locally decouple to PGND using a low ESR/ESL capacitor located as close to the controller as possible. Optional input for an externally supplied VCC.
VCCX	If VCCX > 4.5 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. If VCCX is unused, it should be connected to ground.
VOUT	Output monitor. Connect directly to the output voltage.

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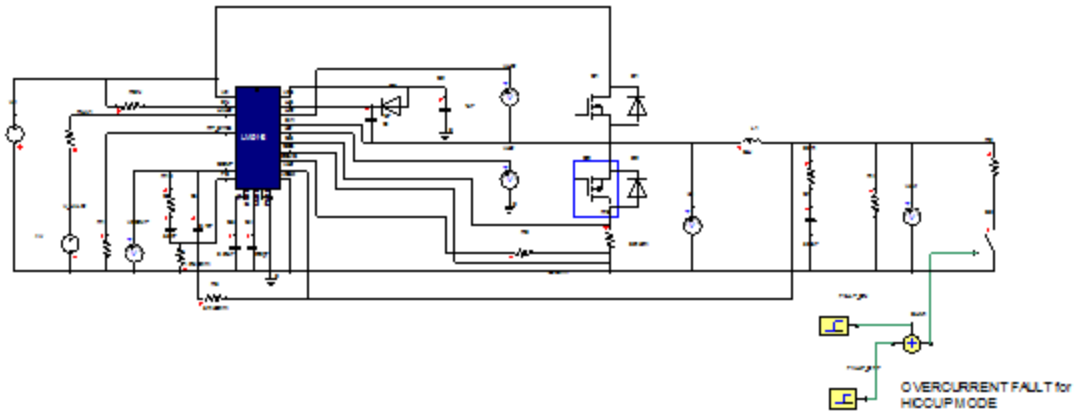

Figure 2. Buck Converter. 5V 7-A Typical Application

Simulation – signal diagrams

Figure 3 and Figure 4 show the transient waveforms of the output voltage and the inductor current of the Buck converter controlled with the LM5116.

The first part of the transient corresponds to the soft-start process. The output voltage increases almost linearly up to the reference voltage of 5V. The inductor current provides both the current to charge the output capacitor and the load. When the soft-start is finished, and the output voltage reaches the steady-state value, the averaged current through the inductor will be equal to the output current.

At t=2ms, there is an overload fault created by closing the switch that controls the overcurrent load. The current through the inductor is limited to the maximum inductor current, and the HICCUP protection counts 256 consecutive clock cycles of overcurrent, the regulator is shutdown by pulling down the UVLO pin. The regulator is started with a full soft-start cycle.

The regulator starts the new soft-start cycle at 3.3ms, and since the fault is still present, is tries to provide the maximum current. At t=3.5ms the fault is cleared, and the soft-start process continues until the converter reaches the steady-state value.

Simulation results :

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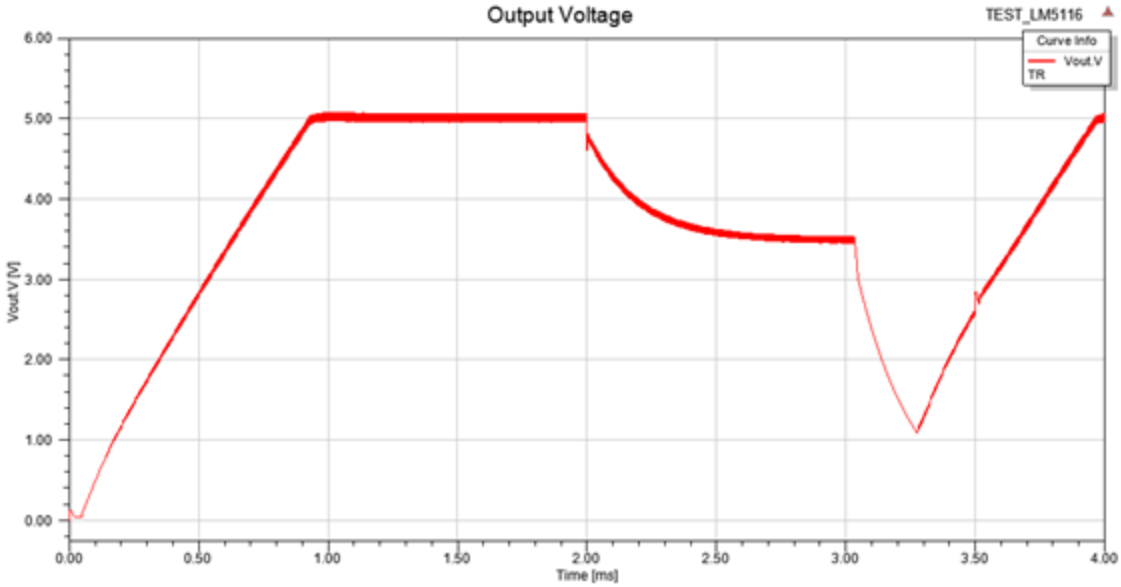

Figure 3. Output Voltage

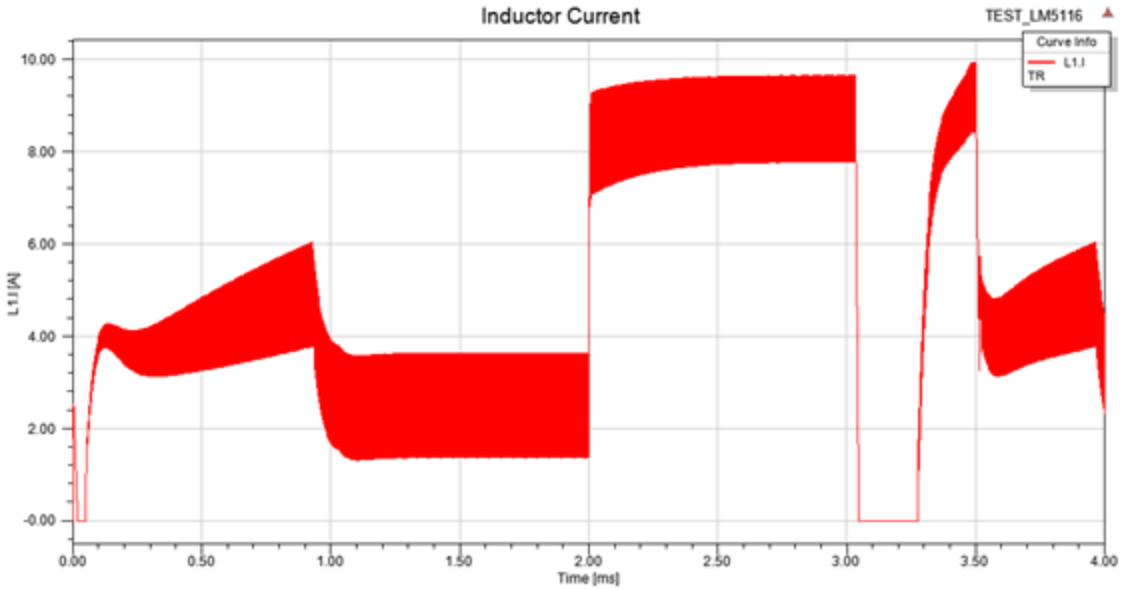

Figure 4: Inductor Current

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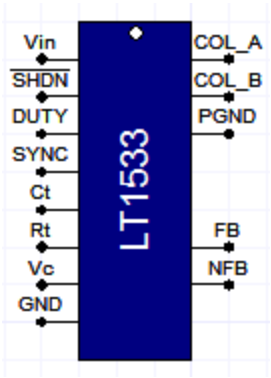
LT1533: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The LT1533 is a new class of switching regulator designed to reduce conducted and radiated electromagnetic interference (EMI). Ultralow noise and EMI are achieved by providing

user control of the output switch slew rates. Voltage and current slew rates can be independently programmed to optimize switcher harmonic content versus efficiency. The LT1533 can reduce high frequency harmonic power by as much as 40dB with only minor losses in efficiency.

The LT1533 utilizes a dual output switch current mode architecture optimized for low noise topologies. The IC includes two 1A power switches along with all necessary oscillator, control and protection circuitry. Unique error amp circuitry can regulate both positive and negative voltages. The internal oscillator may be synchronized to an external clock for more accurate placement of switching harmonics. Protection features include cycle by cycle current limit protection, undervoltage lockout and thermal shutdown.

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Low minimum supply voltage and low supply current during shutdown make the LT1533 well suited for portable applications. The part may also be forced into a 50% duty cycle mode for unregulated applications.

Assumptions and Limitations

Slew control is not implemented in the model of LT1533, due to lack of information and simulation speed consideration. The output drivers behind pin COL_A and COL_B are directly controlled by pulse signal generated by the internal PWM state machine. As a result, the model has no reduction effect on noise or EMI as the actual device does. Pin R_VLS and R_CSL for slew rate programming is not included in this model.

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Conservative Pins

Table 1

Name	Description
COLA, COLB	These are the output collectors of the power switches. Their emitters return to PGND through a common sense resistor. COL A and COL B are alternately turned on out of phase. Large currents flow into these pins so it is desirable to keep external trace lengths short to minimize radiation. The collectors can be tied together for simple boost applications.
DUTY	Tying the DUTY pin to ground will force the outputs to switch with a 50% duty cycle. The DUTY pin must float if not used.
SYNC	The SYNC pin can be used to synchronize the oscillator to an external clock (see Oscillator Sync in Applications Information section for more details). The SYNC pin may either be floated or tied to ground if not used.
Ct	The oscillator capacitor pin is used in conjunction with RT to set the oscillator frequency
Rt	The oscillator resistor pin is used to set the charge and discharge currents of the oscillator capacitor. The nominal value is 16.9k. It is possible to adjust this resistance ±25% to get a more accurate oscillator frequency.
FB	The feedback pin is used for positive voltage sensing and oscillator frequency shifting during start-up and short-circuit conditions. It is the inverting input to the error amplifier. The noninverting input of this amplifier connects internally to a 1.25V reference. This pin should be left open if not used.
NFB	The negative voltage feedback pin is used for sensing a negative output voltage. The pin is connected to the inverting input of the negative feedback amplifier through a 100k source resistor. The negative feedback amplifier provides a gain of – 0.5 to the feedback amplifier. The nominal regulation point would be –2.5V on NFB. This pin should be left open if not used.

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GND	Signal Ground. The internal error amplifier, negative feedback amplifier, oscillator, slew control circuitry and the bandgap reference are referred to this ground. Keep the connection to the feedback divider and VC compensation network free of large ground currents.
VC	The compensation pin is used for frequency compensation and current limiting. It is the output of the error amplifier and the input of the current comparator. Loop frequency compensation can be performed with an RC network connected from the VC pin to ground.
SHDN	The shutdown pin is used for disabling the switcher. Grounding this pin will disable all internal circuitry. Normally this output can be tied high (to VIN) or may be left floating.
Rcsl	A resistor to ground sets the current slew rate for the collectors A and B.
Rvsl	A resistor to ground sets the voltage slew rate for the collectors A and B.
Vin	Input Supply Pin. Bypass this pin with a ≥ 4.7mF low ESR capacitor. When VIN is below 2.55V the part will go into undervoltage lockout where it will stop output switching and pull the VC pin low.
PGND	Power Switch Ground. This ground comes from the emitters of the power switches.

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Example:

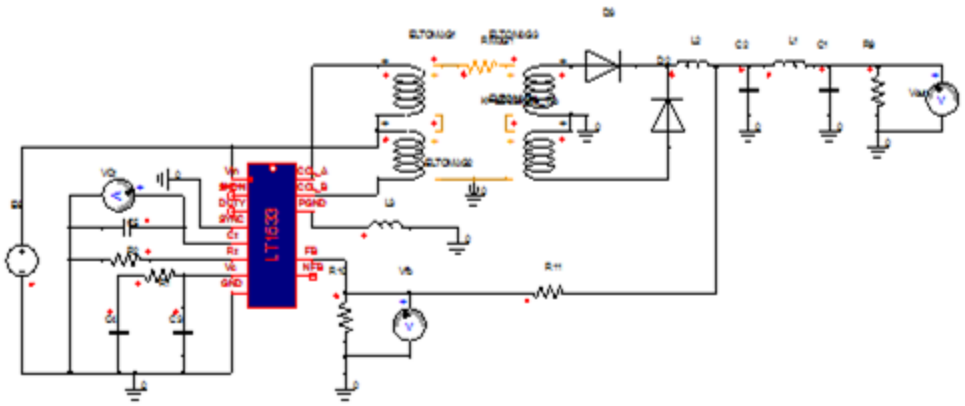

Figure 2. 5V to 12V Forward Push-Pull DC/DC Converter. Typical application

Simulation – signal diagrams

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Figure 3 shows the transient waveform of the output voltage and the inductor current of the push-pull converter controlled with the LT1533. The output voltage reaches the steady-state value at t=3.0ms.

Figure 4 shows how the switching frequency changes as a function of the voltage at the feedback pin. The initial switching frequency is 7 times slower than the selected value adjusted with the Rt resistor and Ct capacitor. The switching frequency increases proportional to the voltage at the feedback pin until it reaches the nominal value at Vfb = 0.4V.

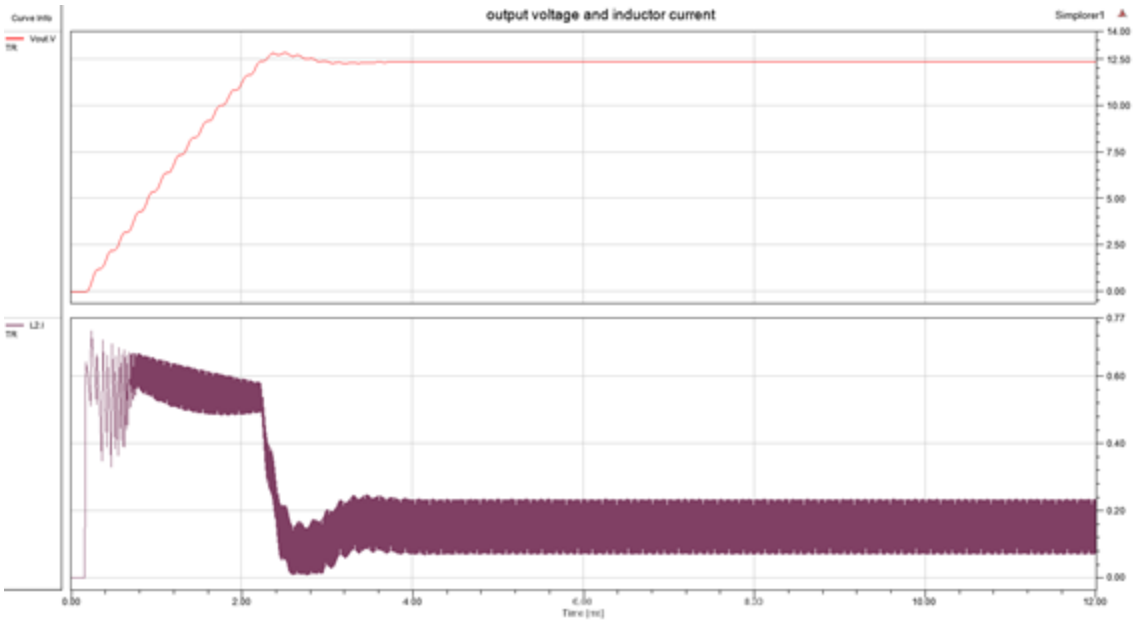

Figure 3. Output voltage and inductor current

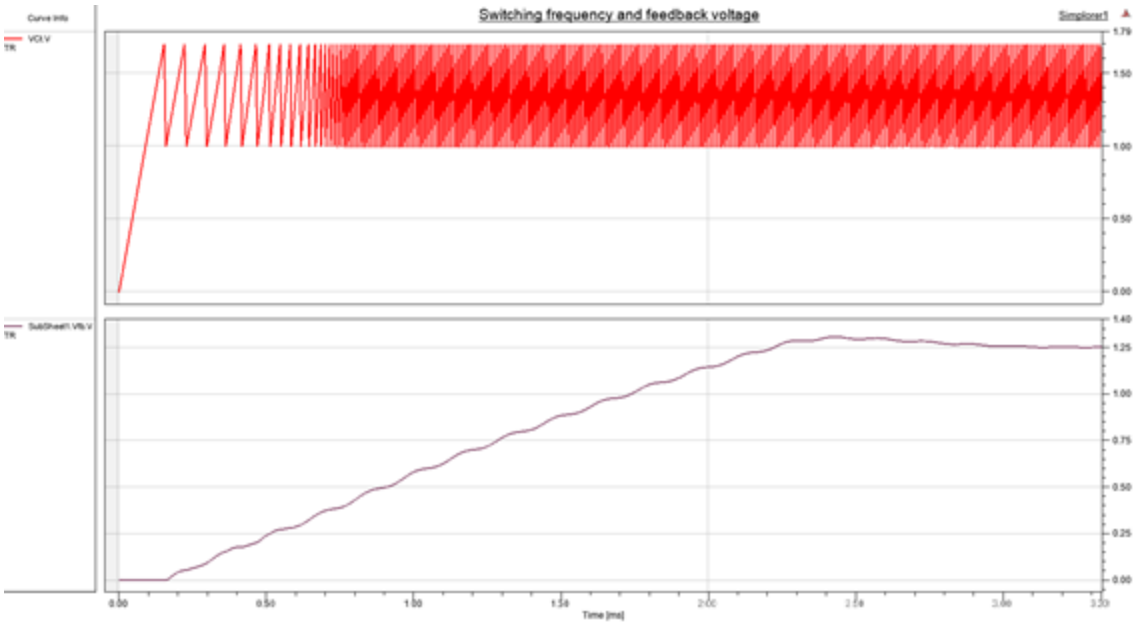

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Figure 4. Switching frequency and feedback voltage

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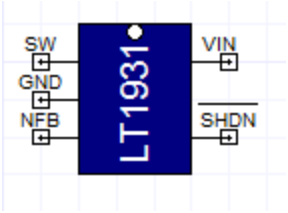
LT1931: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The LT1931/LT1931A are the industry's highest power inverting SOT-23 current mode DC/DC converters. Both parts include a 1A integrated switch allowing high current outputs to be generated in a small footprint. The LT1931 switches at 1.2MHz while the LT1931A switches at 2.2MHz. These high speeds enable the use of tiny, low cost capacitors and inductors 2mm or less in height. The LT1931 is capable of generating – 5V at 350mA or –12V at 150mA from a 5V supply, while the LT1931A can generate –5V at 300mA using significantly smaller inductors. Both parts are easy pin-for-pin upgrades for higher power LT1611 applications.

The LT1931/LT1931A operate in a dual inductor inverting topology that filters both the input side and output side current. Very low output voltage ripple approaching 1mVP-P can be achieved when ceramic output capacitors are used. Fixed frequency switching ensures a clean output free from low frequency noise typically present with charge pump solutions. The low impedance output remains within 1% of nominal during large load steps. The 36V switch allows VIN to VOUT differential of up to 34V.

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Conservative Pins

Table 1

Name	Description
SW	Switch Pin. Connect inductor/diode here. Minimize trace area at this pin to keep EMI down.
GND	Ground. Tie directly to local ground plane.
NFB	Feedback Pin. Reference voltage is –1.255V. Connect resistive divider tap here. Minimize trace area. The NFB bias current flows out of the pin. Set R1 and R2 according to: For LT1931: $R_1 = \frac{\lvert V_{OUT}\rvert - 1.255}{\frac{1.255}{R_2} + (4 \times 10^{-6})}$ For LT1931A: $R_1 = \frac{\lvert V_{OUT}\rvert - 1.255}{\frac{1.255}{R_2} + (8 \times 10^{-6})}$
SHDN	Shutdown Pin. Tie to 2.4V or more to enable device. Ground to shut down.
VIN	Input Supply Pin. Must be locally bypassed.

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Example:

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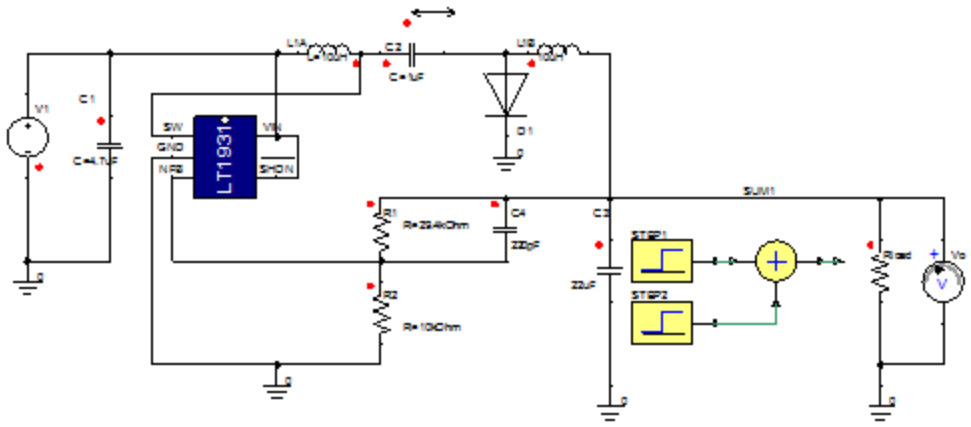

Figure 2. Example of Connection

*Mutual inductance must have a coupling value close to 1

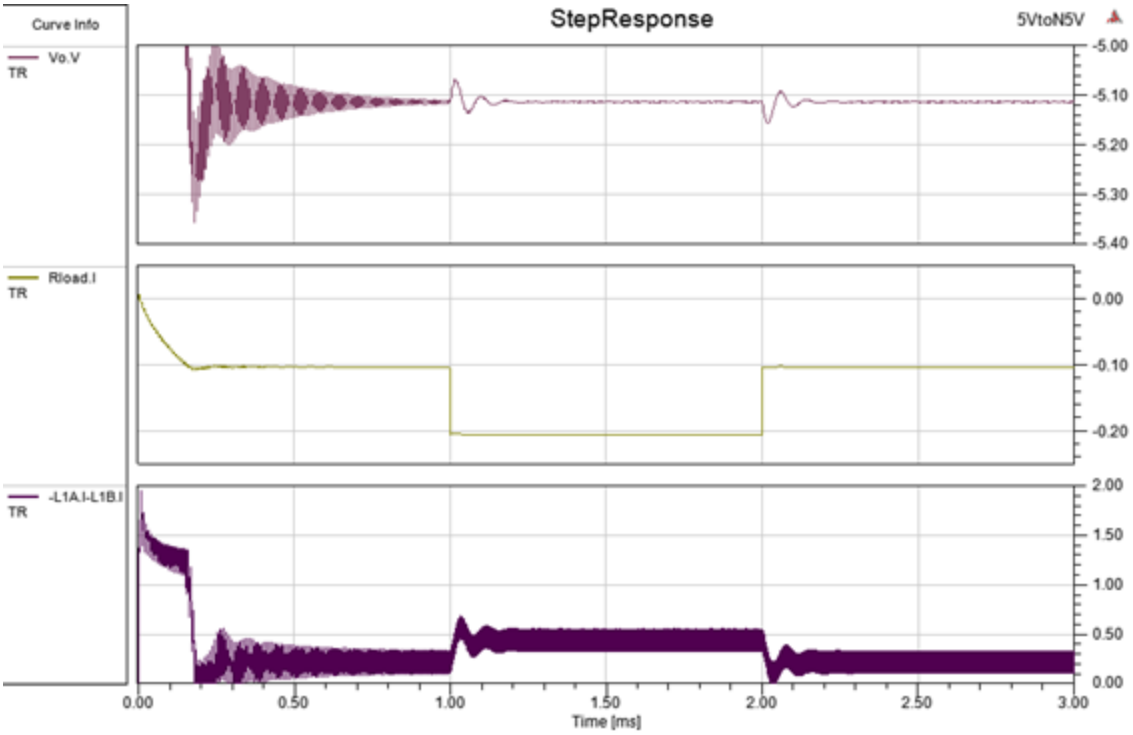

Figure 3. Step Response

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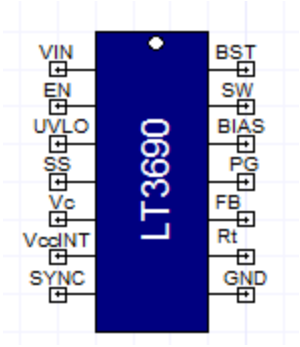
LT3690: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The LT3690 is an adjustable frequency monolithic buck switching regulator that accepts input voltages up to 36V. A high efficiency 90mΩ switch is included on the device along with the boost diode and the necessary oscillator, control, and logic circuitry. The internal synchronous power switch of 30mΩ increases efficiency and eliminates the need for an external Schottky catch diode. Current mode topology is used for fast transient response and good loop stability. Shut-down reduces input supply current to less than 1µA. The low ripple Burst Mode maintains high efficiency at low output currents while keeping output ripple below 15mV in typical applications. The LT3690 features robust operation and is easily configurable. Using a resistor divider on the UVLO pin provides a programmable under voltage lockout. A power good flag signals when VOUT reaches 90% of the programmed out- put voltage. Protection circuitry senses the current in the power switches to protect the LT3690 against short-circuit conditions. Frequency fold back and thermal shutdown provide additional protection.

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Conservative Pins

Table 1

Name	Description
SW	The SW pin is the emitter output of the internal highside NPN power switch (HS) and the drain output of the internal lowside power N-channel switch (LS). Connect this pin to the inductor and boost capacitor. This pin is driven up to the VIN voltage by the HS switch during the on-time of the PWM duty cycle. The inductor current drives the SW pin negative during the off-time. The on-resistance of the LS switch and the internal Schottky diode fixes the negative voltage. The exposed pad is connected internally with SW pins 1-4, 23-26 and should be soldered to a large copper area to reduce thermal resistance.
SYNC	The SYNC pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 20% and 80% duty cycle. The synchronizing range is from 170kHz to 1.5MHz. When not used for synchronization, the SYNC pin can be tied to ground to select low ripple Burst Mode operation or tied to the output voltage to select standard PWM mode.
RT	Oscillator Resistor Input. Connecting a resistor to ground (Pin 10) from this pin sets the switching frequency.
VC	The VC pin is the output of the internal error amplifier. The voltage on this pin controls the peak switch current. Tie an RC network from this pin to ground to compensate the control loop.
FB	The LT3690 regulates the FB pin to 0.8V. Connect the feedback resistor divider tap to this pin. The adjacent ground pin (Pin 10) is recommended for the resistor divider.
SS	The SS pin is used to provide a soft-start or tracking function. The internal 2µA pull-up current ISS in combination with an external capacitor tied to this pin creates a voltage ramp. The output voltage tracks to this voltage. For tracking, tie a resistor divider to this pin from the tracked output. In undervoltage, overvoltage and thermal shutdown, the SS pin pulls low if the output voltage is below the power good threshold to restart the output voltage with soft-start behavior. If driving this pin from a digital output, use at least 10k in series. Leave this pin disconnected if unused.
UVLO	Tie a resistor divider between VIN, UVLO, and GND to program an undervoltage lockout threshold. The UVLO pin has an accurate 1.25V threshold. Above the threshold, the part operates normally. Below the threshold, the part drops into a low quiescent current state.
VIN	The VIN pin supplies current to the LT3690's internal regulator and to the internal

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	power switch. This pin must be locally bypassed.
EN	The EN input is used to put the LT3690 in shutdown mode. Pull to GND to shut down the LT3690. Tie to 1.5V or more for normal operation.
PG	The PG pin is the open collector output of an internal comparator. PG remains low until the FB pin is within 10% of the final regulation voltage. The PG output is valid when VIN is above 3.9V, the UVLO pin is high and EN is high.
BIAS	This pin connects to the anode of the internal boost Schottky diode. BIAS also supplies the current to the LT3690's internal regulator. Tie this pin to the lowest available voltage source above 3V (typically VOUT). This pin must be locally bypassed with 10nF.
VCCINT	VCCINT is an output of the internally generated supply voltage for the synchronous power DMOS transistor driver. An external capacitor CVCC must be connected between this pin and ground (Pin 21) to buffer the internal supply voltage of the LS switch.
BST	This pin is used to provide, with the external boost capacitor, a drive voltage higher than the input voltage VIN to the internal bipolar NPN power switch.
GND	Ground. The exposed pad is connected internally to GND Pins 6, 10, 16 and 21, and should be soldered to a large copper area to reduce thermal resistance.

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Example:

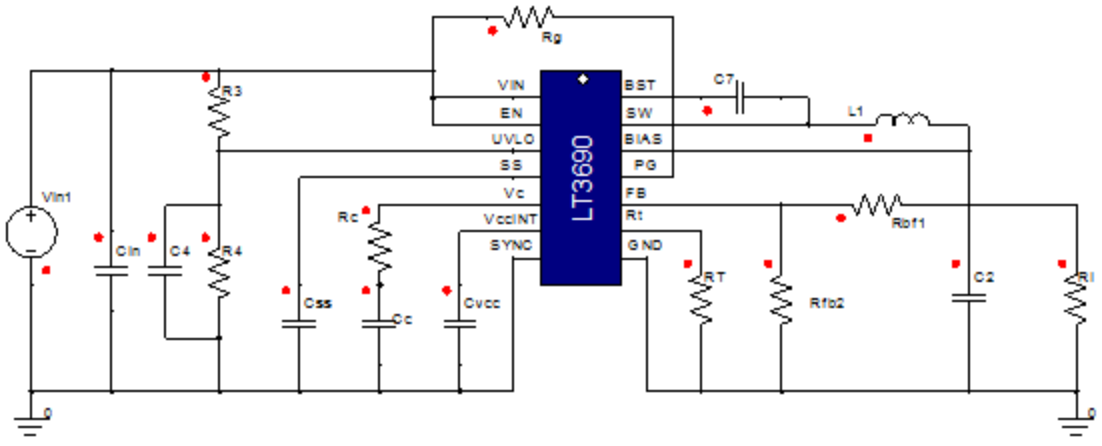

Figure 2. Example of Connection

*Connect AGND to circuit reference

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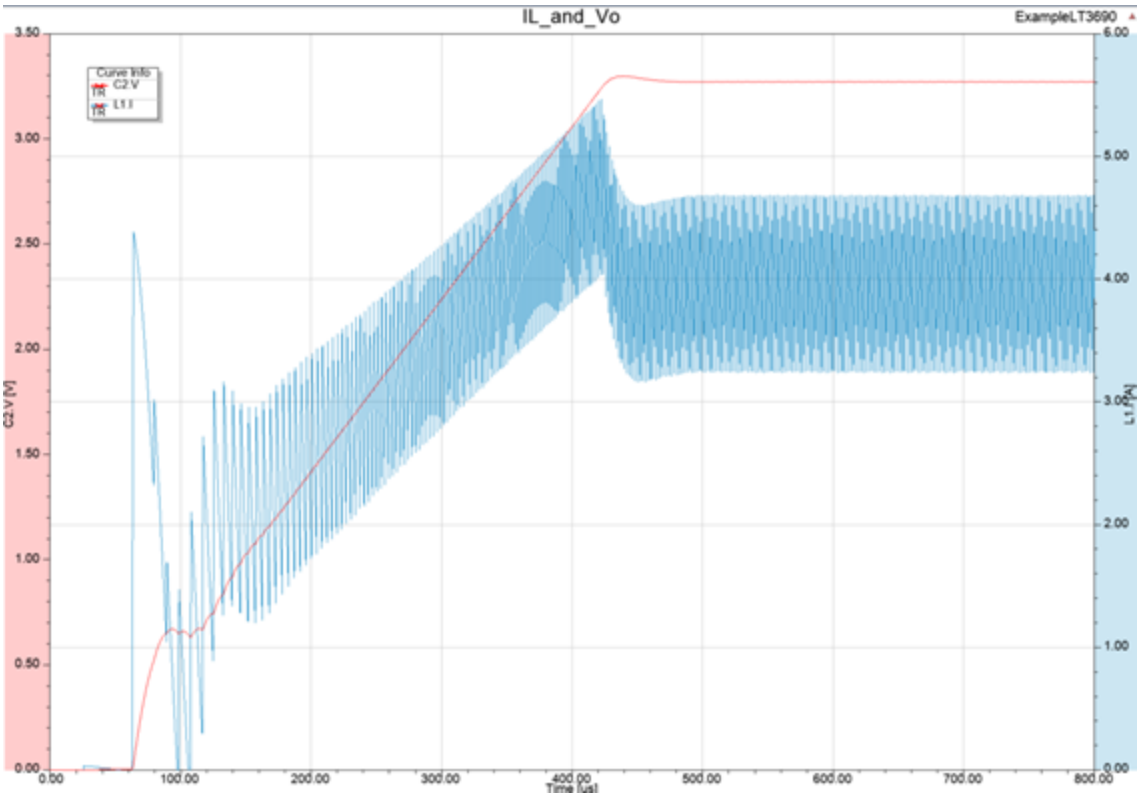

Figure 3. Waveforms

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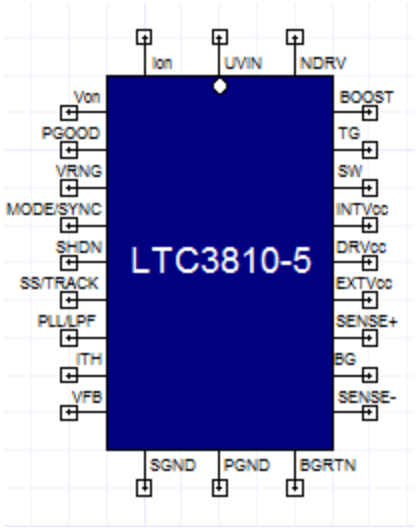
LTC3810_5: Linear Technology

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The LTC 3810-5 is a synchronous step-down switching regulator controller that can directly step-down voltages from up to 60V, making it ideal for telecom and automotive applications. The LTC3810-5 uses a constant on-time valley current control architecture to deliver very low duty cycles with accurate cycle-by-cycle current limit, without requiring a sense resistor.

A precise internal reference provides 0.5% DC accuracy. A high bandwidth (25MHz) error amplifier provides very fast line and load transient response. Large 1Ω gate drivers allow the LTC3810-5 to drive multiple MOSFETs for higher current applications. The operating frequency is selected by an external resistor and is compensated for variations in VIN and can also be

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synchronized to an external clock for switching-noise sensitive applications. A shutdown pin allows the LTC3810-5 to be turned off, reducing the supply current to 240µA.

Integrated bias control generates gate drive power from the input supply during start-up or when an output short- circuit occurs, with the addition of a small external SOT23 MOSFET. When in regulation, power is derived from the output for higher efficiency.

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Name	Description
VON	On-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to the output voltage or to an external resistive divider from the output makes the on-time proportional to VOUT. The comparator defaults to 0.7V when the pin is grounded and defaults to 2.4V when the pin is connected to INTVCC. Tie this pin to INTVCC in high VOUT applications to use a lower RON value.
VRNG	Sense Voltage Limit Set. The voltage at this pin sets the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from INTVCC. The nominal sense voltage defaults to 95mV when this pin is tied to ground, and 215mV when tied to INTVCC.
PGOOD	Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not between ±10% of the regulation point. The output voltage must be out of regulation for at least 120µs before the power good output is pulled to ground.
MODE/SYNC	Pulse Skip Mode Enable/Sync Pin. This multifunction pin provides pulse skip mode enable/ disable control and an external clock input to the phase detector. Pulling this pin below 0.8V or to an external logic-level synchronization signal disables pulse skip mode operation and forces continuous operation. Pulling this pin above 0.8V enables pulse skip mode operation. For a clock input, the phase-locked loop will force the rising top gate signal to be synchronized with the rising edge of the clock signal. This pin can also be connected to a feedback resistor divider from a secondary winding on the inductor to regulate a second output voltage.
ITH	Error Amplifier Compensation Point and Cur- rent Control Threshold. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.6V with 1.2V corresponding to zero sense voltage (zero current).
VFB	Feedback Input. Connect VFB through a resistor divider network to VOUT to set

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	the output voltage.
PLL/LPF	The phase-locked loop's low-pass filter is tied to this pin. The voltage at this pin defaults to 1.2V when the IC is not synchronized with an external clock at the MODE/SYNC pin.
SS/TRACK	Soft-Start/Tracking Input. For soft-start, a capacitor to ground at this pin sets the ramp rate of the output voltage (approximately 0.6s/µF). For coincident or ratiometric tracking, connect this pin to a resistive divider between the voltage to be tracked and ground.
SHDN	Shutdown Pin. Pulling this pin below 1.5V will shut down the LTC3810-5, turn off both of the external MOSFET switches and reduce the quiescent sup- ply current to 240µA.
UVIN	UVLO Input. This pin is input to the internal UVLO and is compared to an internal 0.8V reference. An external resistor divider is connected to this pin and the input supply to program the undervoltage lockout voltage. When UVIN is less than 0.8V, the LTC3810-5 is shut down.
NDRV	Drive Output for External Pass Device of the Linear Regulator for INTVCC. Con- nect to the gate of an external NMOS pass device and a pull-up resistor to the input voltage VIN.
EXTVCC	External Driver Supply Voltage. When this voltage exceeds 4.7V, an internal switch connects this pin to INTVCC through an LDO and turns off the external MOSFET connected to NDRV, so that controller and gate drive are drawn from EXTVCC.
INTVCC	Main Supply Pin. All internal circuits except the output drivers are powered from this pin. INTVCC should be bypassed to ground (Pin 10) with at least a 0.1µF capacitor in close proximity to the LTC3810-5.
DRVCC	Driver Supply Pin. DRVCC supplies power to the BG output driver. This pin is nor- mally connected to INTVCC. DRVCC should be bypassed to BGRTN (Pin 20) with a low ESR (X5R or better) 1µF-10µF capacitor in close proximity to the LTC3810-5.
BG	Bottom Gate Drive. The BG pin drives the gate of the bottom N-channel syn- chronous switch MOSFET. This pin swings from BGRTN to DRVCC.
BGRTN	Bottom Gate Return. This pin connects to the source of the pulldown MOSFET in the BG driver and is normally connected to ground. Connecting a negative sup- ply to this pin allows the synchronous MOSFET 's gate to be pulled below ground to help prevent false turn-on during high dV/dt transitions on the SW node.
SENSE+, SENSE–	Current Sense Comparator Input. The (+) input to the current comparator is nor- mally connected to SW unless using a sense resistor. The (–) input is used to accurately kelvin sense the bottom side of the sense resistor or MOSFET.
SW	Switch Node Connection to Inductor and Bootstrap Capacitor. The voltage swing at this pin is –0.7V (a Schottky diode (external) voltage drop) to VIN.
TG	Top Gate Drive. The TG pin drives the gate of the top N-channel synchronous switch MOSFET. The TG driver draws power from the BOOST pin and returns to the SW pin, providing true floating drive to the top MOSFET.
BOOST	Top Gate Driver Supply. The BOOST pin supplies power to the floating TG driver. BOOST should be bypassed to SW with a low ESR (X5R or better) 0.1µF capacitor. An additional fast recovery Schottky diode from DRVCC to the BOOST pin will create a complete floating charge-pumped supply at BOOST.
ION	On-Time Current Input. Tie a resistor from VIN to this pin to set the one-shot

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	timer current and thereby set the switching frequency.
SGND	Signal Ground. All small signal components should connect to this ground and eventually connect to PGND at one point

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Example:

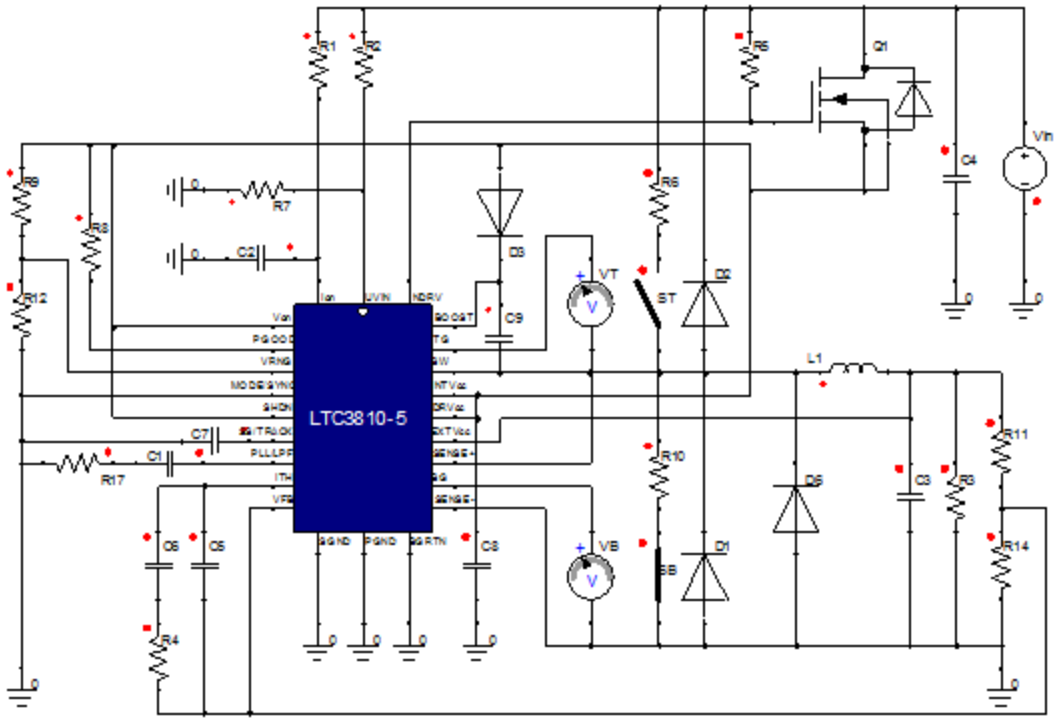

Figure 2. Example of Connection - 24V to 5V@6A

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Three Phase Bridge Drivers

The Three Phase Bridge Drivers consist of the following types of models:

- IR2136

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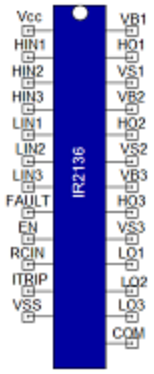
IR2136: International Rectifier

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2



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Description

The *IR213x* are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

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Conservative Pins

Table 1

V_{CC}	Low side and logic fixed supply
V_{SS}	Logic ground
HIN1,2,3 HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase [IR213(6,63,65,66,67,68)] Logic inputs for high side gate driver outputs (HO1,2,3), in phase (IR21362)
LIN1,2,3	Logic input for low side gate driver outputs (LO1,2,3), out of phase
FAULT	Indicates over-current (ITRIP) or low-side under-voltage lockout has occurred. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. I/O logic functions when ENABLE is high (i.e., positive logic) No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance)
RCIN	External RC network input used to define FAULT CLEAR delay, T_{FLTCLR}, approximately equal to R*C. When RCIN > 8 V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate drivers return
$V_{B1,2,3}$	High side floating supply

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HO1,2,3	High side gate driver outputs
$V_{S1,2,3}$	High voltage floating supply return
LO1,2,3	Low side gate driver outputs

Note: All input pins and the ITRIP pin are internally clamped with a 5.2 V zener diode.

Table 2

Part	**IR2136**
Input Logic	HIN, LIN
Ton (typ.)	400 ns
Toff (typ.)	380 ns
V_{IH} (typ.)	2.7 V
V_{IL} (typ.)	1.7 V
Vitrip+	0.46 V
UVCC/BS+	8.9 V
UVCC/BS-	8.2 V

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Parameters

Comparison between model and real component.

VBIAS (VCC,VBS1,2,3) = 15 V unless otherwise specified. The VIN, VTH, and IIN parameters are referenced to VSS and are applicable to all six channels (HIN1,2,3 and LIN1,2,3). The VO and IO parameters are referenced to COM and VS1,2,3 and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Table 3

Symbol	**Definition**	**IR213-6**	**MODEL**	**Units**	**Test Conditions**
VIH	Logic "0" input voltage LIN1,2,3,HIN1,-2,3 (min.) Logic "1" input voltage	3.0	3.0	V	

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	HIN1,2,3 IR21362 (min.)				
VIL	Logic "1" input Voltage LIN1,2,3, HIN1,2,3 (max.) Logic "0" input voltage HIN1,2,3 IR21362 (max.)	0.8	0.8		
VEN,TH+	Enable positive going threshold (max.)	3	3		
VEN,TH-	Enable negative going threshold (min.)	0.8	0.8		
VIT,TH+	ITRIP positive goingthreshold	0.46	0.46		
VIT,HYS	ITRIP input hysteresis	0.07	0.07		
VRCIN, TH+	RCIN positive goingthreshold	8	8		
VRCIN, HYS	RCIN input hysteresis	3			
VOH	High level output voltage, VBIAS - VO	0.9	X		
VOL	Low level output voltage, VO	0.4	X		Io = 20 mA
V VBSUV+	VCC and VBS supply undervoltage positive going threshold	8.9	8.9		
V VBSUV-	VCC and VBS supply undervoltage negative going threshold	8.2	8.2	V	
VCCUVH VBSUVH	VCC and VBS supply undervoltage lockout hysteresis	0.7	X		
ILK	Offset supply	50	X	µA	VB1,2,3 =

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	leakage current (max.)				VS1,2,3 = 600 V
IQBS	Quiescent VBS supplycurrent	70	X		
IQCC	Quiescent VCC supplycurrent	1.6	X	mA	VIN = 0 V or 5 V
VIN,CLAMP	Input clamp voltage (HIN, LIN, ITRIP and EN)	5.2	5.2	V	IIN =100 µA
ILIN+	Input bias current (LOUT = HI)	200	X		VLIN = 5 V
ILIN-	Input bias current (LOUT = LO)	100	X		VLIN = 0 V
IHIN+	Input bias current (HOUT = HI)	200	X		VHIN = 5 V
IHIN-	Input bias current (HOUT = LO)	100	X		VHIN = 0 V
IITRIP+	"High" ITRIP input bias current	30	X	µA	VITRIP = 5 V
IITRIP-	"Low" ITRIP input bias current	0	X		VITRIP = 0 V
IEN+	"High" ENABLE input bias current	30	X		VENABLE = 5 V
IEN-	"Low" ENABLE input bias current	0	X		VENABLE =0 V
IRCIN	RCIN input biascurrent	0	X		Vrcin= 0 V or 15 V
IO+	Output high short circuit pulsed current	200	X	mA	Vo =0 V, PW ≤10 µs
IO-	Output low short circuit pulsed current	350	X		Vo =15 V, PW ≤10 µs
Ron_RCIN	RCIN lowonresistance	50	50	Ω	
Ron_FAULT	FAULT lowonres-	50	50		

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	istance				

X: not implemented

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Input/Output Quantities

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Examples

Example circuit :

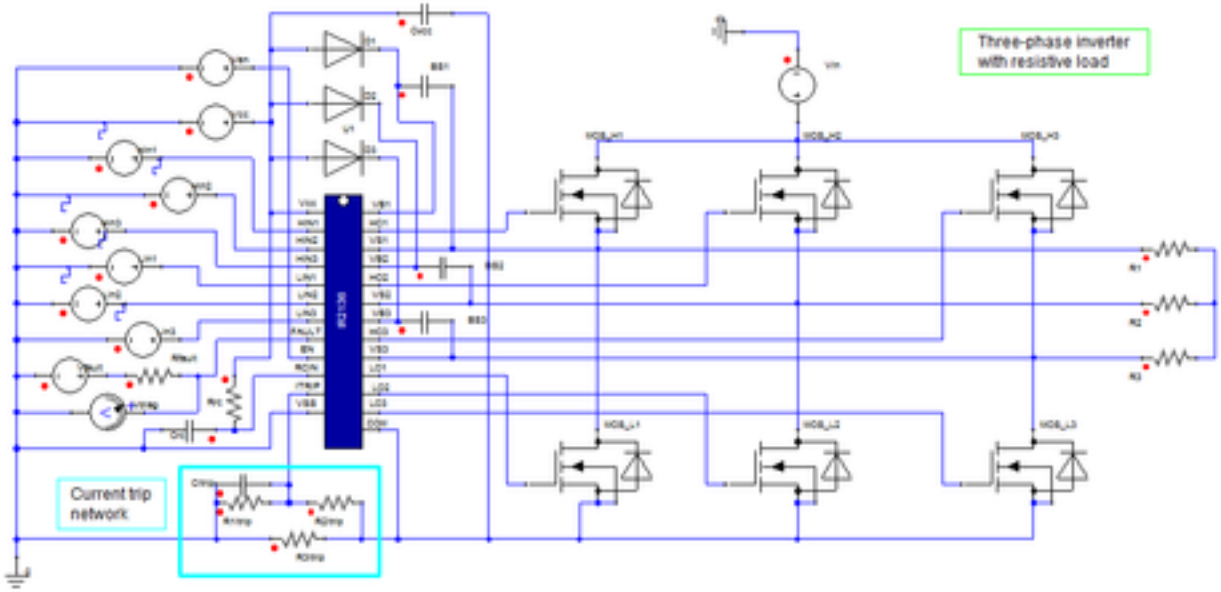

Figure 2. Example Circuit

Simulation results :

Main operation :

Three-phase resistive load output voltages :

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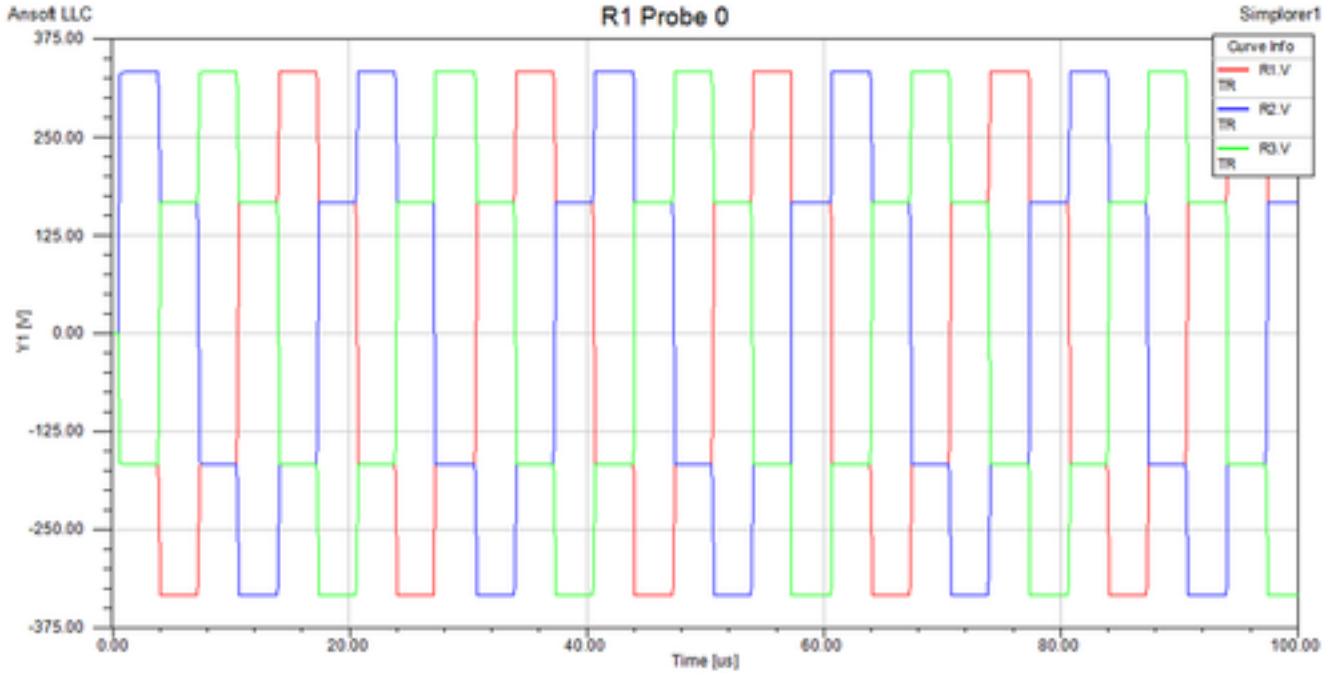

Figure 3. Main Operation results(a)

Input voltages:

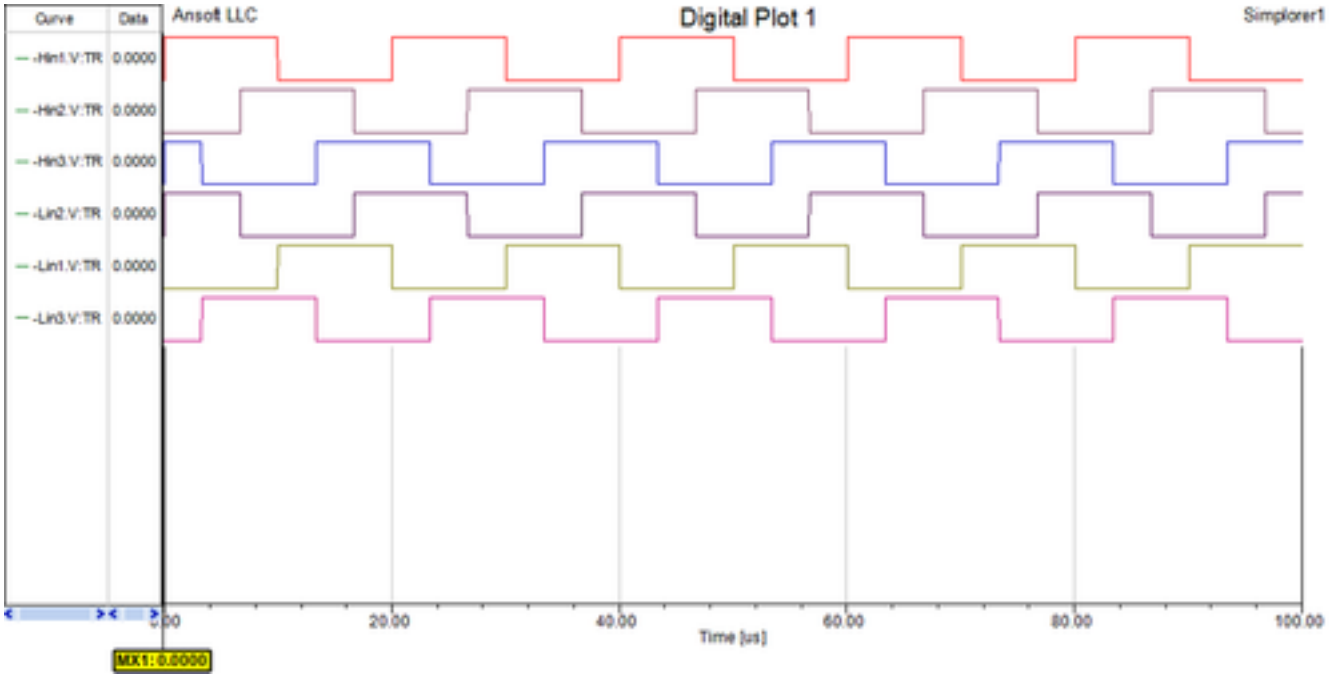

Figure 4. Main Operation results(b)

Enable, fault and current trip protection :

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To test the correct operation of the enable circuit, the fault signal and the current trip protection circuit we connect a square voltage source to the enable pin and a triangular voltage source to the ITRIP pin. When enable voltage falls below 0.8V, the outputs are disabled. Moreover, when the ITRIP voltage exceeds 0.46V, the outputs are disabled and the open drain FAULT pin is connected to ground. These overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. This voltage is represented by the green wave. When the voltage reaches 8V, FAULT rises and the outputs are enabled.

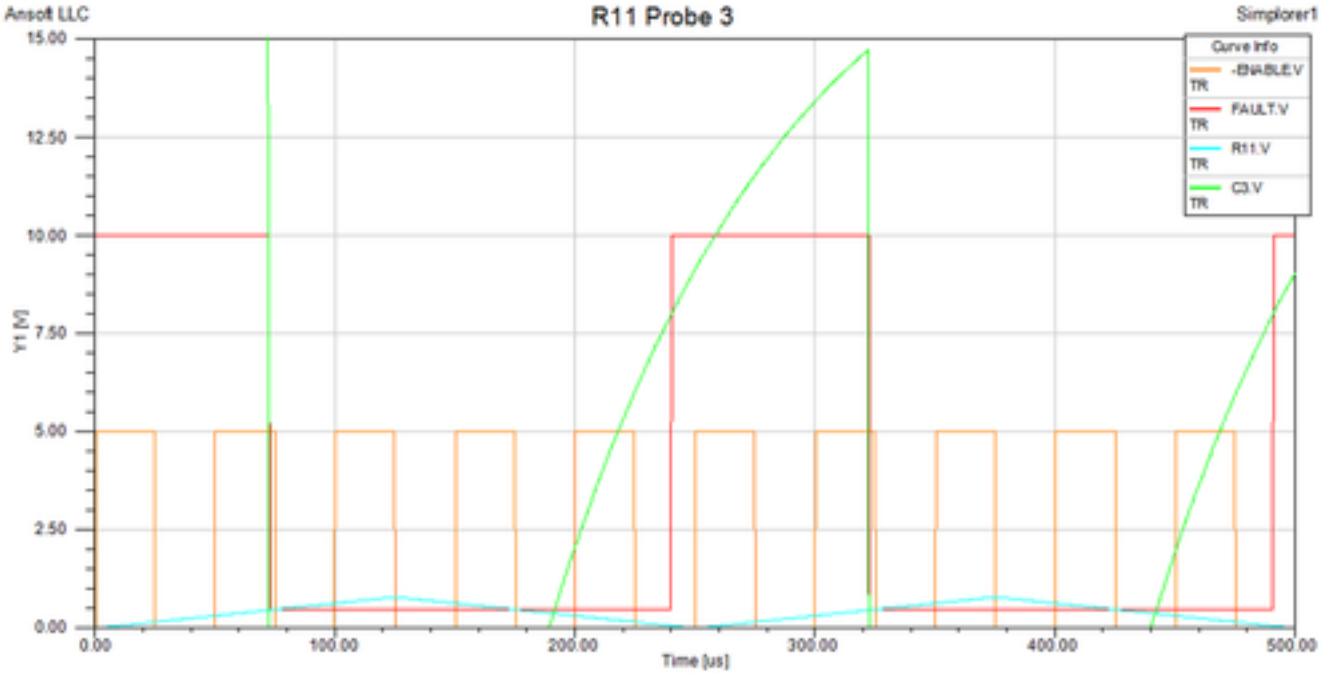

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Figure 5. Protect Operation results(a)

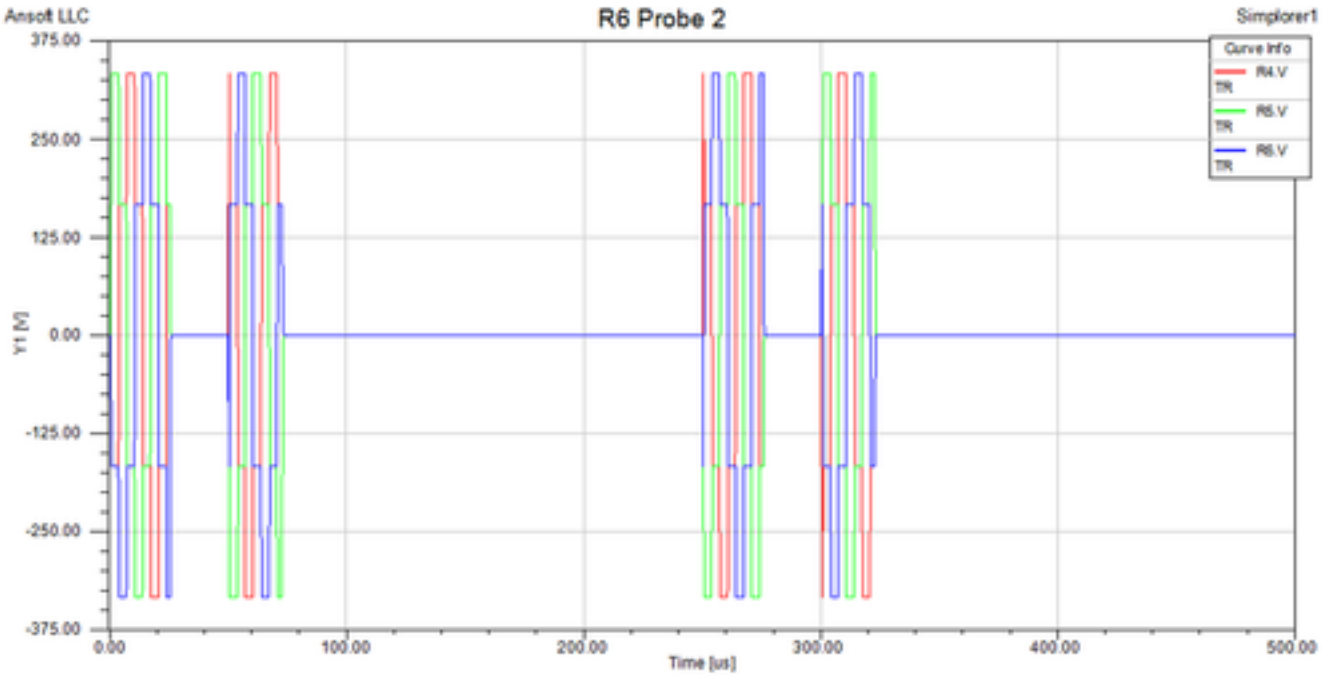
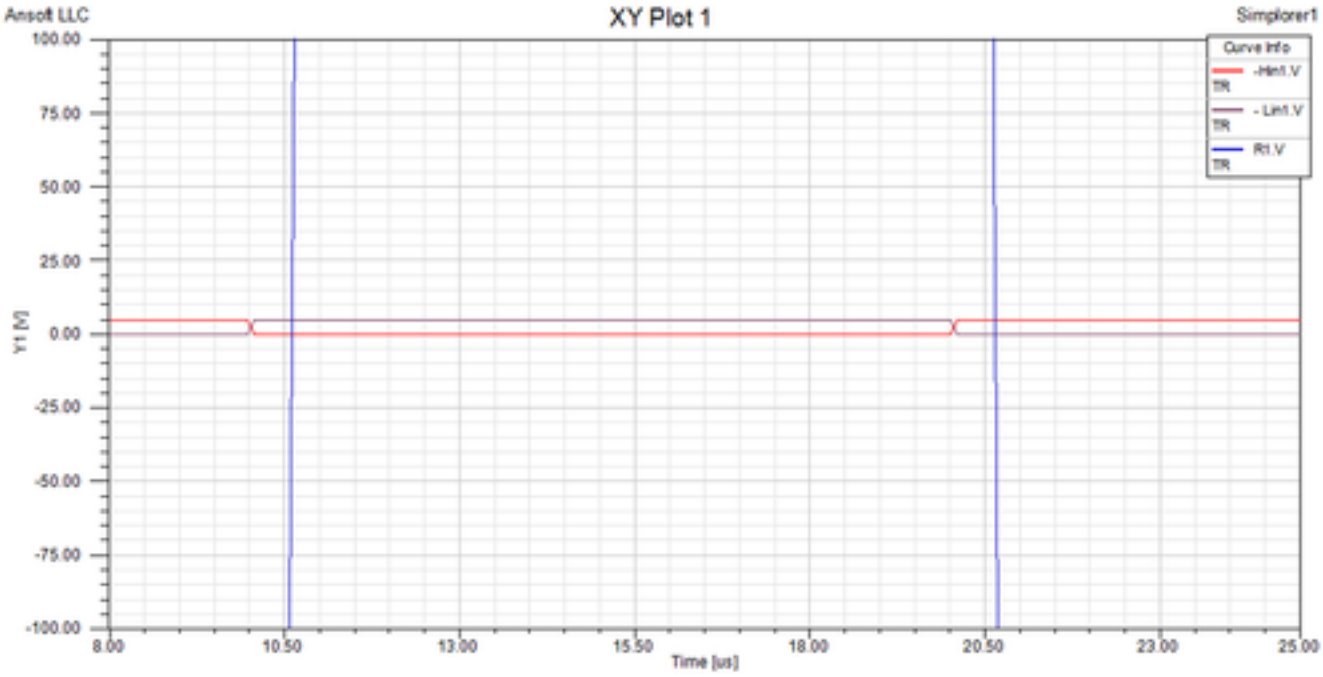


Figure 6. Protect Operation results(b)

Detail of delays:



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Red: high side input voltage

Brown: low side input voltage

Blue: phase 1 output voltage

Figure 7. Protect Operation results(c)

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References

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Zener models

The Zener models consist of the following diode:

• Zener

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Zener Diode

Library: Power Management ICs	Modeling Language: SML	Version Number: Twin Builder 2025.2

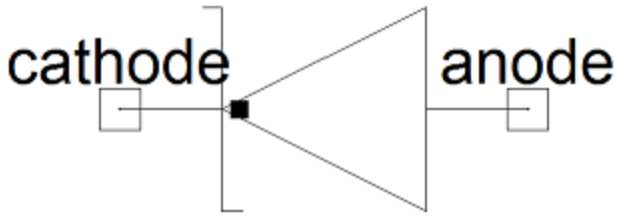

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Conservative Pins

• Parameters

• Input/Output Quantities

• Example

• References

Description

Zener diodes are a special kind of diode, which not only allows current to flow in the forward direction, but also conducts in reverse direction when the reverse voltage is above a certain value called the Zener voltage.

The Zener diode model is a system-level model that simulates the static voltage-current-relation using equivalent line model.

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Assumptions and Limitations

This component models a static voltage-current-relation of Zener diode; therefore, the dynamic behaviors are not taken into account.

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Mathematical Description

A static equivalent line model is used for the voltage-current-relation of this component. Bulk resistance during conducting is RB, reverse resistance during blocking is RR, forward voltage is VF, and the reverse breakdown voltage, or Zener Voltage, is configurable by input Vzener.

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Netlist Syntax

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Conservative Pins

Table 1

Name	Port/Terminal Description	Nature/Data Type
anode	Anode	electrical
cathode	Cathode	electrical

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Parameters

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Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
Vzener	Zener Voltage [V]	input	real
VF	Forward Voltage [V]	input	real
RB	Bulk Resistance [ohm]	input	real
RR	Reverse Resistance [ohm]	input	real

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Examples

This example includes two Zener diode clipping circuits to demonstrate its voltage limiting and waveform shaping applications. The schematic of the example is shown in Figure 2, and system parameters are listed in Table 3 :

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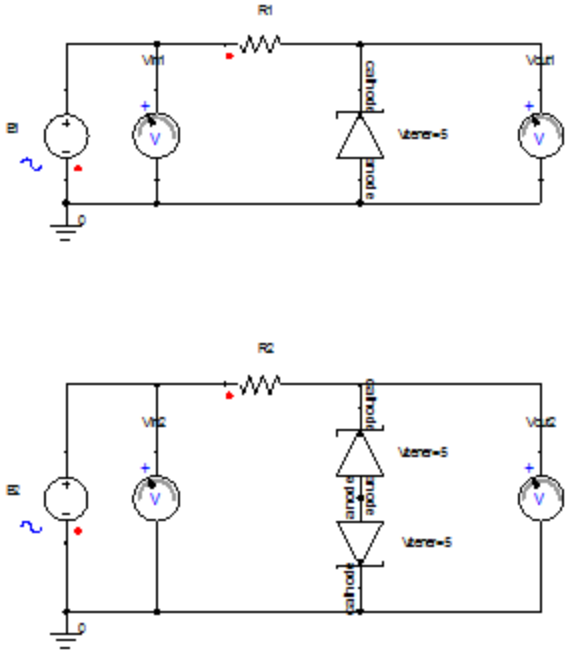

Figure 2. Application example of the System-Level Diode model

Table 3

Component	Parameter	Value [unit]
Voltage Source (sinusoidal) E1 and E2	AMPL	10 [V]
	FREQ	50 [Hz]
	TDELAY	0 [s]
	PHASE	0 [degree]
	OFF	0 [V]
Resistor R1, R2	R	1k [Ohm]
Zener Diode Zener1, Zener2 and Zener3	Vzener	5[V]
	VF	0.7 [V]
	RB	1m [Ohm]
	RR	100k [Ohm]

Simulation result of the single Zener diode circuit is shown in Figure 3. When Input Voltage goes above the 5V Zener voltage, it starts conducting and clips the output voltage at Zener voltage.

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On the other hand, its forward conducting is the same as a regular diode, when input signal goes negative, output is clipped at -0.7V since forward voltage VF is set to 0.7V.

Simulation result of the double Zener diode circuit is shown in Figure 4. Output is clipped at Vzener + VF in both directions due to the combined effect of the two Zener diodes.

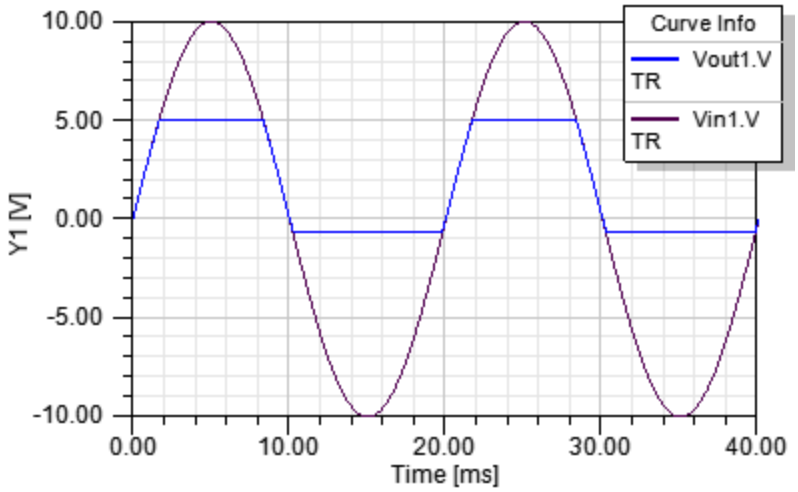

Figure 3. Simulation results for single Zener diode circuit

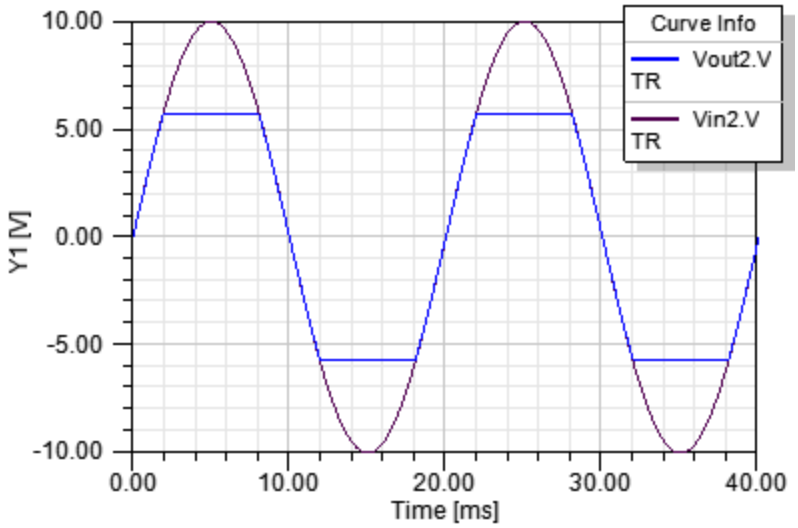

Figure 4. Simulation results for double Zener diode circuit

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References

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